World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:13, No:7, 2019

Digital Encoder Based Power Frequency Deviation Measurement

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***Abstract*—**In this paper, a simple method is presented for measurement of power frequency deviations. A phase locked loop (PLL) is used to multiply the signal under test by a factor of 100. The number of pulses in this pulse train signal is counted over a stable known period, using decade driving assemblies (DDAs) and flip-flops. These signals are combined using logic gates and then passed through decade counters to give a unique combination of pulses or levels, which are further encoded. These pulses are equally suitable for both control applications and display units. The experimental circuit developed gives a resolution of 1 Hz within the measurement period of 20 ms. The proposed circuit is also simulated in Verilog Hardware Description Language (VHDL) and implemented using Field Programing Gate Arrays (FPGAs). A Mixed signal Oscilloscope (MSO) is used to observe the results of FPGA implementation. These results are compared with the results of the proposed circuit of discrete components. The proposed system is useful for frequency deviation measurement and control in power systems.

***Keywords*—**Frequency measurement, digital control, phase locked loop, encoding, Verilog HDL.

I. Introduction

FREQUENCY is one the most important parameter for proper operation and performance in various systems such as alternators, induction motors, Universal Testing Machine (UTM) and Particle Image Velocimetry (PIV) systems. The deviation of frequency from its nominal value lowers the efficiency of the systems and also effects the performance of computers and servers.

A number of circuits are presented in the literature which can accurately measure the frequency deviations [1]-[5]. It can be done by using a BCD up/down counter too [6]. In this case, a pulse train representing the reference frequency is compared with the actual signal (which is also taken in the form of a pulse train). The difference in the frequency between the pulse numbers over a known period is counted using the up/down counter. The frequency deviation measurement can also be done using an electronic bridge [7], or a mono-stable multi-vibrator [8]. Some of these methods [6]-[8] require a stable high frequency signal and give the final output in the form of a number (counter's output) which represents the frequency deviation from its nominal value. In this paper, one simple technique is being presented which is found quite useful for providing control signals in the case of power system frequency deviations.

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II. Realization

In the proposed method, the sinusoidal signal whose frequency deviation measurement is required, is reduced to a low voltage level (2 V). This signal is then multiplied by a factor of 100 using PLL to get a pulse train A as shown in Fig. 1. The stable signal B (25 Hz) is obtained from the output Q of the flip-flop (FF-2). Q of FF-2 is used to clear the three decade counters by the trailing edge of B (i.e. the leading edge of Q). These decade counters (DC-1 to DC-3) are cascaded together. Signals A and B are ANDed together by gate G-0 and then applied to the first decade counter DC-1. For a 50 Hz sinusoidal signal, 100 pulses are passed through the counters whenever signal B is high (20 ms. duration) as shown in Fig. 2. Least significant bit (LSB) of DC-3 will be high, whereas all the other outputs of all the three counters will be zero (as shown in Table I).

At the output corresponding to 50 Hz signal (DC-3, pin number 12/3), one pulse appears in every 20 ms. duration (whenever signal B is high) which remains present above 50 Hz and disappears below 50 Hz as shown in Table II. If the frequency of unknown signal (signal under test) is deviated from its nominal value (increases), its duration decreases, more than 100 pulses are passed through the AND gate G-0 and counted by counters, whereas if the frequency of unknown signal decreases, its duration increases. Less than 100 pulses will be passed through G-0 and counted by counters. The outputs of the three counters become high (1) or low (0) accordingly. If all the high state outputs of the three counters are ANDed together on gates (G-46 to G-54), a unique combination of pulses is obtained at the outputs of these AND gates for each 1 Hz deviation as shown in Table II.

Table I shows the output of three counters for deviation of 4 Hz above and below the nominal value (50 Hz). Table II shows the output of different AND gates G-46 to G-54. Inputs of these gates are numbered according to connection of pin number of three-decade counters, corresponding to a frequency deviation from 46 Hz to 54 Hz. In the proposed method, the outputs are taken from the counters through AND gates so that unique combination of pulses is obtained. When the outputs are taken through latches, then stable high or low levels are obtained at the output of the AND gates. These voltages are directly applicable to drive display units for deviation conditions. The same voltages can also be used for control applications.

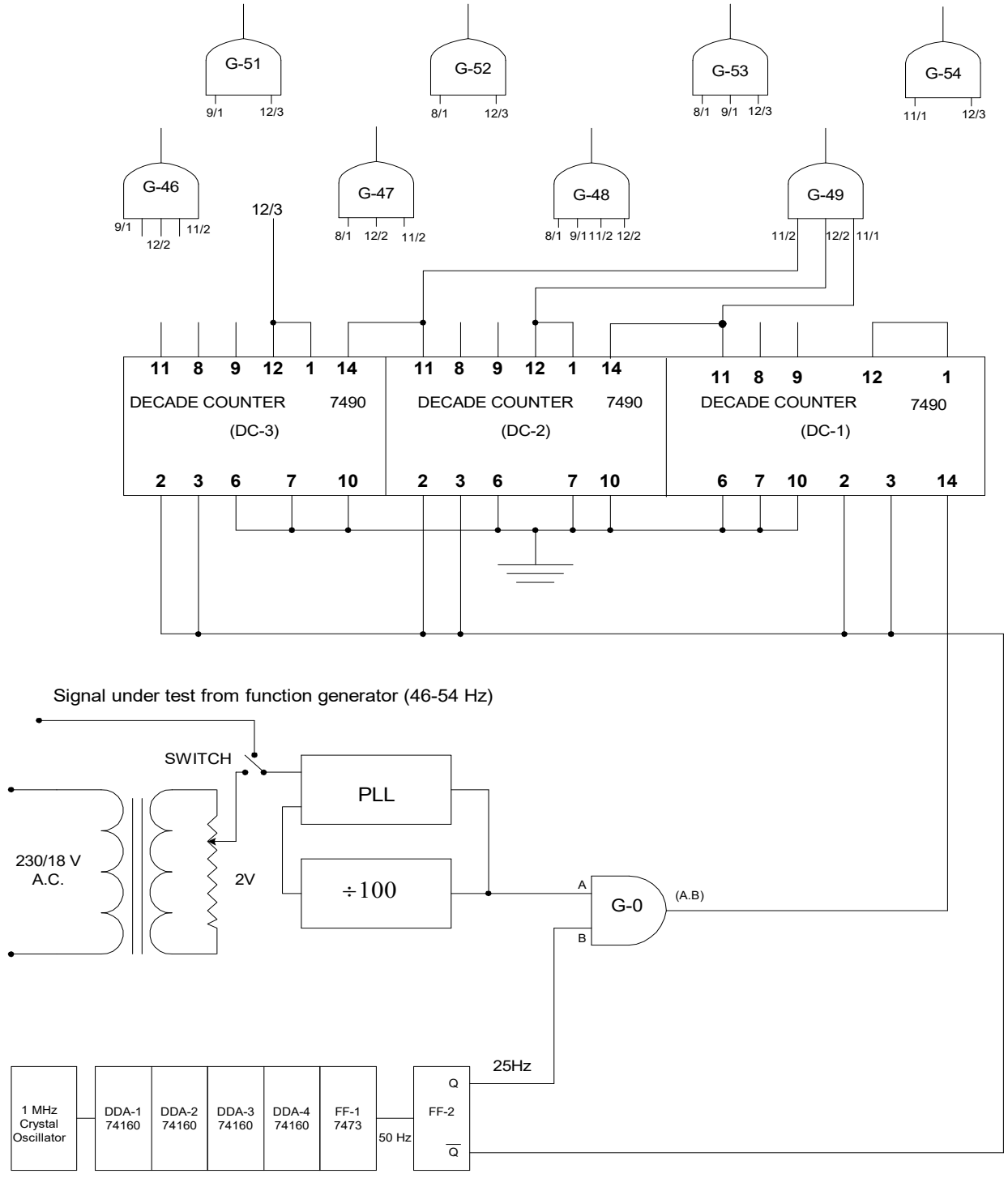

Fig. 1 A setup for frequency deviation measurement

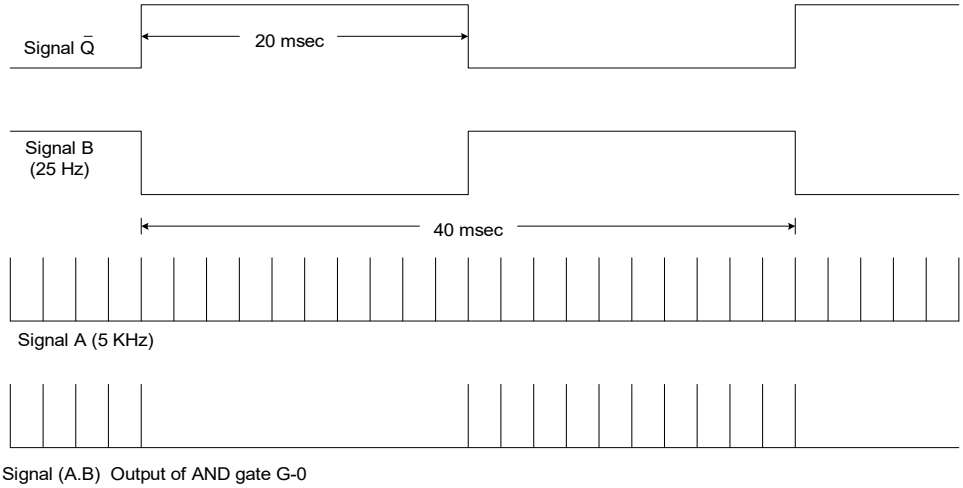

Fig. 2 Wave shapes of signals for frequency deviation measurement

TABLE I
OUTPUTS OF DECADE COUNTERS (DC-1 TO DC-3)

Frequency of signal under test in Hz	Decade counter DC-3 Pin Nos. 11	8	9	12	Decade counter DC-2 Pin Nos. 11	8	9	12	Decade counter DC-1 Pin Nos. 11	8	9	12	Number of pulses passed through AND gate G-0 when signal B is high
46	0	0	0	0	1	0	0	1	0	0	1	0	92
47	0	0	0	0	1	0	0	1	0	1	0	0	94
48	0	0	0	0	1	0	0	1	0	1	1	0	96
49	0	0	0	0	1	0	0	1	1	0	0	0	98
50	0	0	0	1	0	0	0	0	0	0	0	0	100
51	0	0	0	1	0	0	0	0	0	0	1	0	102
52	0	0	0	1	0	0	0	0	0	1	0	0	104
53	0	0	0	1	0	0	0	0	0	1	1	0	106
54	0	0	0	1	0	0	0	0	1	0	0	0	108

TABLE II
NUMBER OF PULSES AT THE OUTPUTS OF AND GATES (G-46 TO G-54)

Frequency of signal under test in Hz	G-46	G-47	G-48	G-49	DC-3 Pin No. 12/3	G-51	G-52	G-53	G-54
46	1	0	0	0	0	0	0	0	0
47	1	1	0	0	0	0	0	0	0
48	2	1	1	0	0	0	0	0	0
49	2	1	1	1	0	0	0	0	0
50	2	1	1	1	1	0	0	0	0
51	2	1	1	1	1	1	0	0	0
52	2	1	1	1	1	1	1	0	0
53	2	1	1	1	1	2	2	1	0
54	2	1	1	1	1	2	2	1	1

The Verilog HDL Simulation using Xilinx ISE tools is used to verify the functionality of the developed circuit. Fig. 3 shows the simulation results of digital encoder with encoded bit stream. The simulation results match with the hardware implementation results of the circuit with discrete components (Table II). The Verilog model is synthesized into gate level netlist and the bit stream is generated and transferred to an FPGA kit. The FPGA kit implemented the circuit of Fig. 1. The results of implementation by FPGA kit are recorded on a Mixed Signal Oscilloscope as shown in Fig. 4. The results of implemented circuit match with the results of simulation, as shown in Fig. 3. These results also match with circuit, which is realized with discrete components, as shown in Table II.

III. CONCLUSION

The developed circuit is tested experimentally with a resolution of 1 Hz within 20 ms of the measurement period (Table I). The same scheme may be extended to provide a resolution of 0.5 Hz within 20 ms measurement period with slight modifications. The resolution can further be increased by simply increasing the measurement period of stable low frequency pulse. However, this requires additional counters and gates at the output stage. The behavioral model of Verilog HDL is used to simulate and synthesize the circuit of digital encoder which is also implemented by FPGA. The results of implementation of the circuit on FPGA, match with the results simulation. Moreover, these results also match with the results

of hardware, realized by discrete components. The main feature of the proposed scheme is that a unique combination of the pulses (or levels) are obtained, which may be directly used for control applications as well as to drive a display unit.

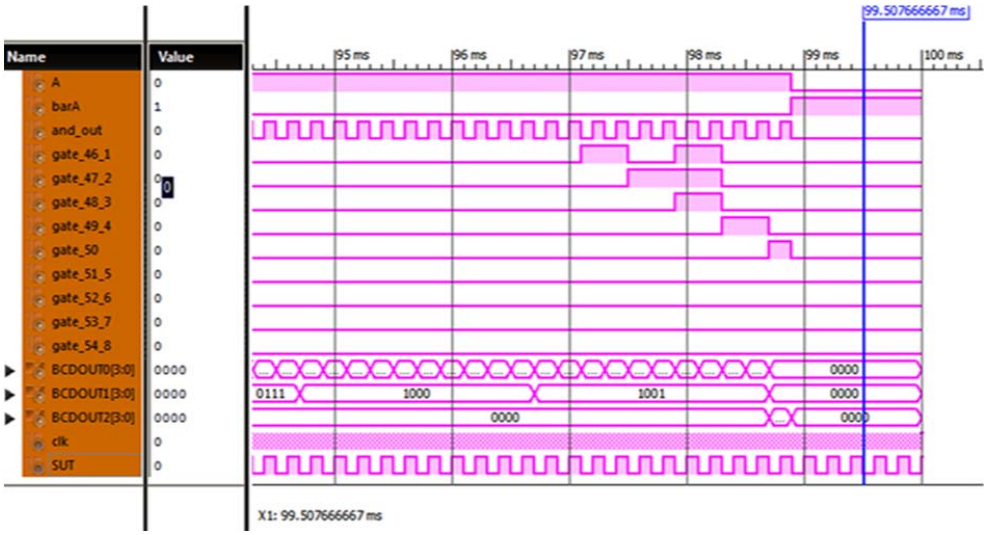

Fig. 3 (a) Simulation results of digital encoder at the output of AND gate at 50 Hz.

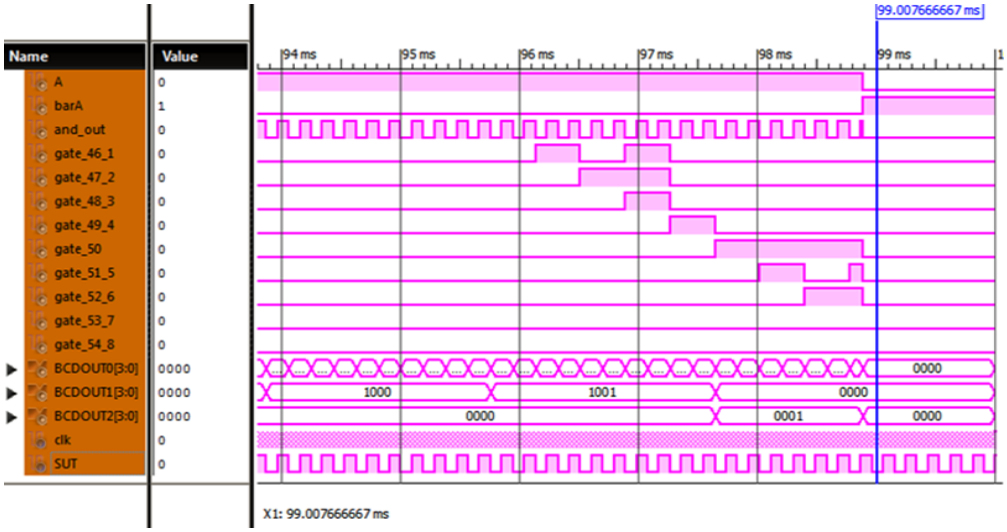

Fig. 3 (b) Simulation results of digital encoder at the output of AND gates at 52 Hz

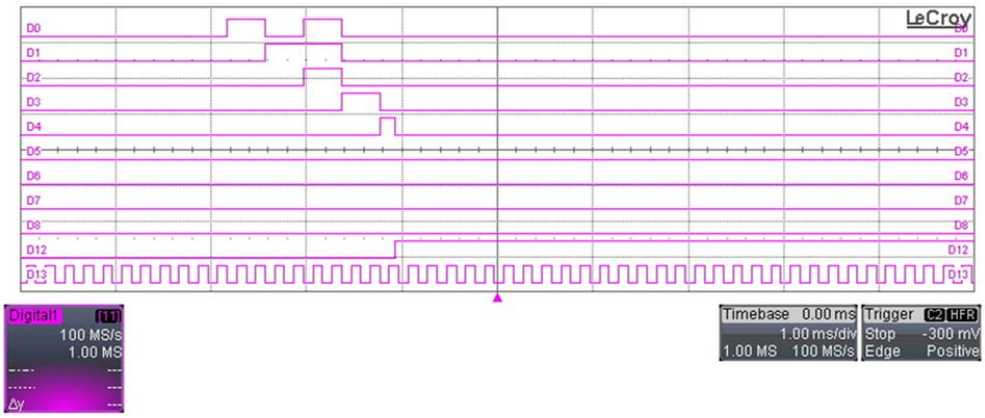

Fig. 4 (a) implementation results of digital encoder on FPGA kit at 50 Hz

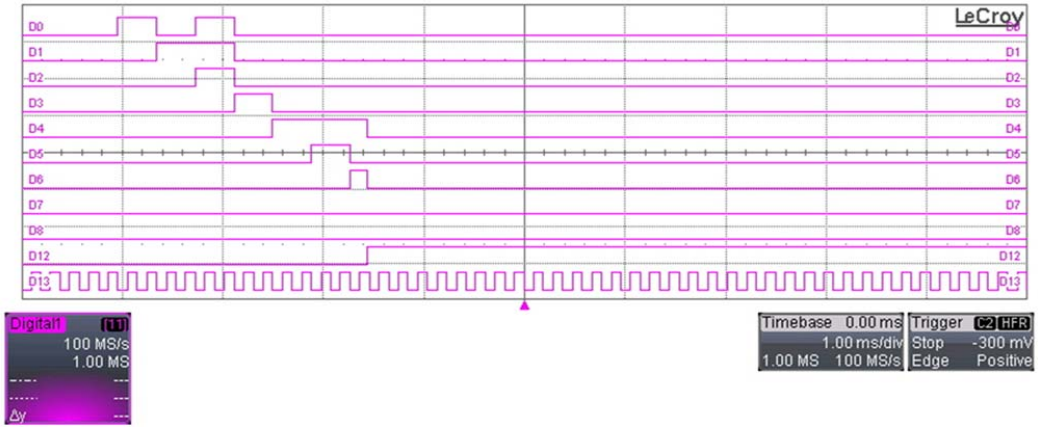

Fig. 4 (b) implementation results of digital encoder on FPGA kit at 52 Hz

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