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A Topology for High Voltage Gain Half-Bridge Z-Source Inverter with Low Voltage Stress on Capacitors

M. Nageswara Rao

***Abstract*—**In this paper, a topology for high voltage gain half-bridge z-source inverter with low voltage stress on capacitors is proposed. The proposed inverter has only one impedance network. It can generate symmetric and asymmetric voltages with different magnitudes during both half-cycles. By selecting the duty cycle it can also produce conventional half-bridge inverter characteristics. It is used in special applications like, electrochemical and electro plating applications. Calculations of voltage ripple of capacitors, capacitors voltage stress inductors current ripple are presented. The proposed topology is simulated using PSCAD software and the simulated values are compared with the theoretical values.

***Keywords*—**Half-bridge inverter, impedance network-source inverter, high voltage gain inverter, power system computer aided design.

I. Introduction

IN conventional inverter, shoot through (ST) state occurs in any one of the legs of inverter. This ST state will damage the inverter. The RMS output AC voltage of conventional voltage source inverter (VSI) is limited to less than input voltage [1]. To avoid the above problems of conventional inverter, a new topology that is, Z-source inverter is presented in [2]. To increase the voltage gain, Z-Source Inverter (ZSI) uses ST state by gating on both the switches of a leg simultaneously. ZSI has some disadvantages; inrush current at starting is very high, voltage stress across capacitor is very high, to overcome this, quasi-Z-source inverter (QZSI) has been presented in [3]. Unlike the ZSI, the QZSI has continuous input current and common ground between input source and inverter stage. To get high-voltage gain switched inductor Z-source inverter (SL-ZSI) has been proposed in [4], its drawback is high voltage stress in comparison with QZSI and conventional ZSI. To reduce number of passive elements in conventional ZSIs, switched-boost inverter (SBI) has been presented in [5]. This inverter has lower value of boost factor than ZSI. To resolve discontinuity problem of input current and to improve the characteristics of SBI, current-fed switched inverter (CFSI) has been presented in [6]. In [7], L-ZSI has been proposed to overcome inrush currents, voltage stress and obtaining high boost factor. Unlike the basic topology, the presented topology in [8] has two impedance networks. The presented half-bridge inverter in [9] has only one impedance network and it is used in industrial applications, such as electroplating and electrochemical. Capacitor voltage stress is high in Half-Bridge Z-Source Inverter (HB-ZSI) with one impedance network. Applications are limited due to positive and negative levels in output waveform. In [10], a quasi-Z-source half-bridge converter has been presented. By implementation of the asymmetrical half-bridge concept, the half-bridge impedance source converter has been simplified and is presented in [11]. For improvement of reliability, some of the researchers presented full-bridge step-up dc/dc converter with cascaded quasi-Z-source networks [12], [13]. In [14], the developed topology for switched-ZSI based on cascaded switched-inductors cells has been presented. Although developed topology has high-voltage gain but voltage stress on capacitor is high. In [15]-[17], a topology for half-bridge SBI based on [5] has been presented. This inverter practices more active elements instead of capacitors and inductors. By using supplementary active elements switching losses can condense efficiency.

In this paper, a topology for half-bridge ZSI is proposed. The proposed inverter has high voltage gain and low capacitors voltage stress. In upcoming sections, in addition to different operating modes of the inverter, calculation of capacitors voltage stress, inductors current ripple, and capacitors voltage ripple are obtained. A control method for proposed inverter is presented. And then, comparison of theoretical and simulation results are compared.

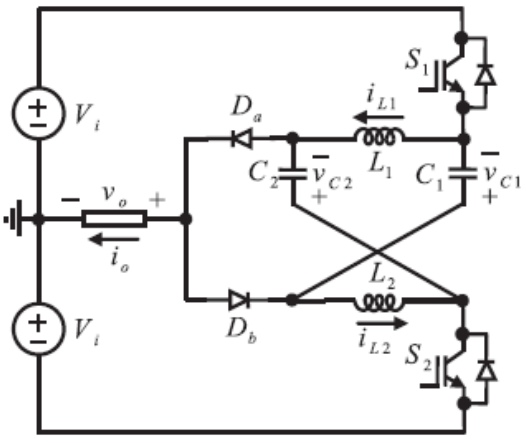


Fig. 1 Power circuit of the proposed half-bridge inverter

Dr.M.Nageswara Rao, Associate Professor, Department of Electrical and Electronics Engineering, University College of Engineering, JNTU Kakinada, Andhra Pradesh, India (e-mail: nagjntuk@gmail.com)

II. Proposed Inverter

Based on connection of LC impedance networks, the power circuit of the proposed inverter with one impedance network is shown in Fig. 1. The proposed half-bridge converter consists of inductors (L1&L2), capacitors (C1&C2), diodes (Da&Db), switches (S1&S2), DC voltage sources (with amplitude Vi) and output load. The anticipated topology can be practiced in electroplating. Some assumptions are made to simplify the circuit: all elements are same, L1 = L2 = L and C1 = C2 = C, the load is taken as resistive.

A. Operating States of the Proposed Inverter in SOD Mode

The operating modes of the proposed inverter in SOD are analyzed in this section. In SOD, the diodes are turned on and turned off simultaneously. In this study, DS1 and DS2 are the duty cycles of switches S1and S2, respectively, and DST is the division result of turn on time period for S1 and S2 simultaneously to the total switching period.

$$D_{S1} = D_{S2} = D \tag{1}$$

$$D = 0.5(1 + D_{ST}) \tag{2}$$

also according to symmetry in Fig. 1, we can write

$$i_{L1} = i_{L2} = i_L \tag{3}$$

$$V_{L1} = V_{L2} = V_L \tag{4}$$

$$V_{C1} = V_{C2} = V_C \tag{5}$$

where i_{L1} and i_{L2} are the inductors currents, respectively, that are shown as i_L. V_{L1} and V_{L2} are the inductors voltages, respectively, and are shown as V_L. Also, V_{C1} and V_{C2} are the capacitors average voltages, respectively, which are shown as V_C.

1. First Operating Mode ($0 \le t < 0.5DSTTs$):

In this operating mode both of S1 and S2 switches are ON and diodes Da and Db are OFF. In this time interval, the inductors' voltage is positive; therefore, their current reaches from a minimum value (ILV) to a maximum value (ILP). Also, the stored energy in capacitors and their voltage are decreased. By using Kirchhoff's voltage law (KVL), we can write

$$V_L = 2V_i + V_C \tag{6}$$

$$V_{Da} = V_{Db} = -V_i - V_C \tag{7}$$

where V_{Da} and V_{Db} are the voltages of diodes Da and Db respectively, that are assumed negative. Because diodes Da and Db are OFF, the load voltage (V_O) in this operating mode becomes zero and we have

$$V_O = 0. \tag{8}$$

Hence, the proposed half-bridge inverter unlike to the conventional one can provide zero-voltage level in the output.

2. Second Operating Mode ($0.5DST\ Ts \le t < 0.5Ts$):

In this operating mode, the switches S1 and S2 are ON and OFF respectively, and both Da and Db are ON. Therefore, the output voltage will be positive and the voltage of capacitors C1 and C2 will be decrease and increase, respectively. Also, due to the negative voltage across inductors, their current decreases from a maximum value (ILP) to a minimum value (ILV). By applying KVL, we can write

$$V_L = -V_C \tag{9}$$

$$V_O = V_{O,max} = V_i + V_C \tag{10}$$

3. Third Operating Mode ($0.5Ts \le t < 0.5(1 + DST)Ts$):

The operating mode in the time interval $0.5Ts \le t < 0.5(1 + DST)\ Ts$ is similar to the mentioned first mode.

4. Fourth Operating Mode ($0.5(1 + DST)Ts \le t < Ts$):

In this operating mode, the switches S1 and S2 are OFF and ON, respectively, and both Da and Db are ON. Therefore, the output voltage is negative and the energy of capacitors C2 and C1 will decrease and increase, respectively. Similar to the previous operating mode, the inductor's current decreases with slope $-V_C/L$ that leads to a decrement in its energy.

The voltage across inductor is the same as (9) and by applying KVL, (11) is obtained:

$$V_o = V_{o,min} = -V_i - V_C\ . \tag{11}$$

Based on the previous discussions, the voltage across inductors is positive when both S1 and S2 are ON and otherwise the voltage is negative. Considering the voltage balance law in inductors and by using (6) and (9), the capacitor average voltage is calculated as:

$$Vc = \frac{2 - 4D}{4D - 3} Vi \tag{12}$$

By replacing the D value from (2), (12) is rewritten as:

$$Vc = \frac{2D_{ST}}{1 - 2D_{ST}} Vi \tag{13}$$

From (13) the theoretical value of DST is in interval $0 < DST < 0.5$. Using (10) and (12), the maximum output voltage is calculated as:

$$Vo\max = -Vo, \min = \frac{1}{3 - 4D} Vi \tag{14}$$

By replacing the D value from (2), (14) is rewritten as:

$$Vo, \max = -Vo, \min = \frac{1}{1 - 2D_{ST}} Vi = BVi \tag{15}$$

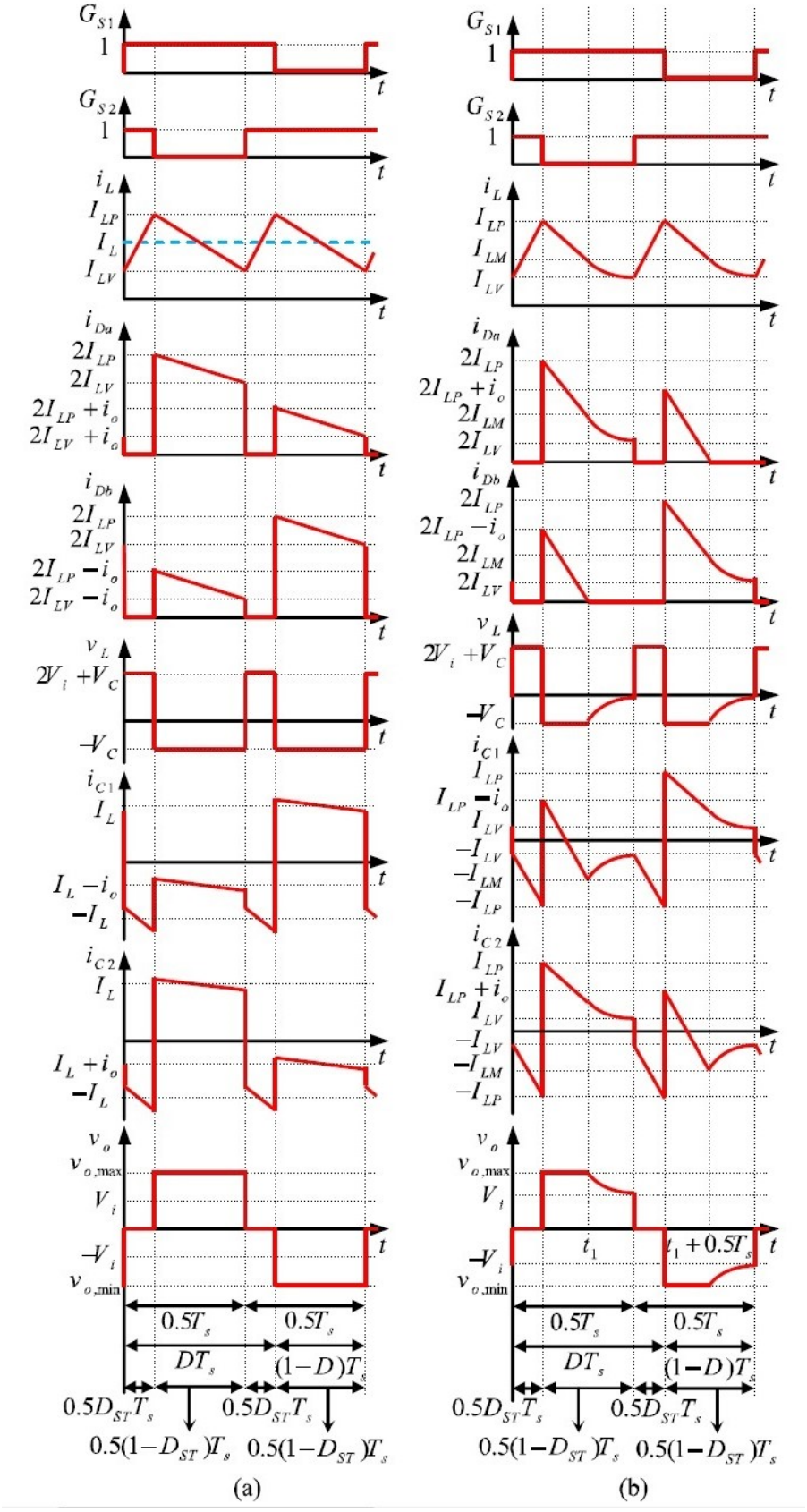


Fig. 2 Voltage and current waveforms of the proposed topology: (a) in SOD and (b) in AOD

Boost factor (B) in (15) is the ratio of maximum output voltage to the value of one of the input voltage sources. Fig. 2

shows the main waveforms of the proposed inverter in SOD. In this figure, GS1 and GS2 are the trigger pulses to the switches S1 and S2, respectively. 1 and 0 are the on and off states of switches, respectively.

B. Operating States of the Proposed Inverter in AOD Mode

The AOD is achieved, if any of the inductance values of inductors, output load, switching frequency, or ST duty cycle is selected in such a way that the current through diode Da in time interval $0.5(1 + DST)Ts \leq t < Ts$ and the current through diode Db in time interval $0.5DSTTs \leq t < 0.5Ts$ becomes zero. In next sections, the different operating in AOD is explained.

1. First Operating Mode

In this operating mode, both S1 and S2 are ON and diodes Da and Db are OFF. The inductors voltage is positive so their current reaches from a minimum value (I_{LV}) to a maximum value (I_{LP}). By applying Kirchhoff's current law (KCL), we can write

$$i_{C1} = -i_{L2} = -i_L \tag{16}$$

$$i_{C2} = -i_{L1} = -i_L \tag{17}$$

Also, (6)-(8) are correct in this operating mode.

2. Second Operating Mode

In this operating mode, the switches S1 and S2 are ON and OFF, respectively. Also, the diodes Da and Db are ON. Sum of the currents through inductors L1 and L2 flows through diode Da. The current through diode Db is calculated as:

$$i_{Db} = i_{L1} + i_{L2} - i_o = 2_{iL} - i \tag{18}$$

Equations (9) and (10) are true for this operating mode; therefore, the currents through L1 and L2 decrease linearly from I_{LP} to I_{LM} at the end of this operating mode (t = t1) and the output voltage will be positive. By applying KCL, the following equations are derived:

$$i_{C1} = i_{L1} - i_o = i_L - i_o \tag{19}$$

$$i_{C2} = i_{L2} = i_L \tag{20}$$

It is noticeable that at the end of this operating mode, the current through diode Db is zero.

3. Third Operating Mode

In this operating mode, the switches S1 and S2 are ON and OFF, respectively. Also, the operation of diodes is asynchronous and the diodes Da and Db are ON and OFF, respectively. Like the second operating mode, sum of the currents through inductors L1 and L2 flows through diode Da. For inductors L1 and L2, by considering the new base time, (21) and (22) are calculated:

$$i_L = \frac{Vi}{2RL} + \left(\frac{Vi + Vc}{2RL} - \frac{Vi}{2RL}\right)e^{-\frac{2Rl}{L}t} \tag{21}$$

Equation (21) shows that the current through inductors decreases exponentially

$$V_L = -V_C e^{-\frac{2Rl}{L}t} \tag{22}$$

Equation (22) shows that the voltage across inductors increases exponentially. By applying KVL and using (22), the output voltage is calculated as:

$$V_o = V_i + V_C e^{-\frac{2Rl}{L}t} \tag{23}$$

Equation (23) shows that the value of output voltage is not constant.

4. Fourth Operating Mode

The fourth operating mode is similar to the mentioned first operating mode.

v) Fifth Operating Mode:

In this operating mode, the switches S1 and S2 are OFF and ON, respectively. Also, the diodes Da and Db are ON. Sum of the currents through inductors L1 and L2 flows through diode Db. The current through diode Da is calculated as:

$$i_{Da} = i_{L1} + i_{L2} + i_o = 2_{iL} + i_o \tag{24}$$

Equations (9) and (11) are true for this operating mode; therefore, the currents through L1 and L2 decrease linearly from I_{LP} to I_{LM} at the end of this operating mode (t = t1 + 0.5 Ts) and the output voltage will be negative. By applying KCL, (25) and (26) are derived:

$$i_{C1} = i_{L1} = i_L \tag{25}$$

$$i_{C2} = i_{L2} + i_o = i_L + i_o \tag{26}$$

It is noticeable that at the end of this operating mode, the current through diode Da is zero.

vi) Sixth Operating Mode:

In this operating mode, the switches S1 and S2 are OFF and ON, respectively. Also, the operation of diodes is asynchronous and the diodes Da and Db are OFF and ON, respectively. Like the fifth operating mode, sum of the currents through inductors L1 and L2 flow through diode Db. For inductors L1 and L2, by considering the new base time, (21) and (22) are true. By applying KVL and using (22), the output voltage is calculated as:

$$V_o = -V_i - V_C e^{-\frac{2Rl}{L}t} \tag{27}$$

Equations (23) and (27) show that the output voltage waveform in AOD changes exponentially; therefore, the symmetry of waveform is destroyed and the proper selection of inductance for not entering into AOD is necessary. Fig. 2

(b) shows the main waveforms of the proposed inverter in AOD.

III. Calculation of Current Ripple for Inductor and Voltage Ripple for Capacitor

For proper design of capacitor and inductor values, calculation of ripples for inductor and capacitor is necessary. In AOD, the symmetry of output waveform is destroyed but in SOD, the output voltage waveform is completely symmetric and the proposed inverter has a better performance; therefore, design considerations are derived just for SOD. Calculations of inductors' current ripple and capacitors' voltage ripple are important factors to design the proper values for inductor and capacitor. First by using equation vL = L(diL /dt), (9), and (13), the value of inductors' current ripple is calculated as:

$$|\Delta i_L| = \frac{D_{ST}(1-D_{ST})T_S}{L(1-2D_{ST})}Vi \quad (31)$$

According to the second operating mode in SOD and assuming that inductors' current ripple is negligible, (32) is obtained for the currents through capacitors C_1 and C_2:

$$i_{C1} = i_{C2} = I_L \quad (32)$$

In (32), IL is the inductors' average current. Using (2), (32), and equation i_{C2} = C2 (dV_{C2}/dt), the voltage ripple of capacitors is calculated as:

$$|\Delta v_c| = \frac{(1-D_{ST})T_S}{2C} I_L \quad (33)$$

Equation (33) shows the important role of I_L in calculation of capacitors' voltage ripple. By considering the current balance law in capacitors, the value of I_L is calculated as:

$$I_L = \frac{1-D_{ST}}{2R_L(1-2D_{ST})^2}Vi \quad (34)$$

where R_L is the value of output resistive load. By replacing I_L from (33), $|\Delta V_C|$ is obtained as:

$$|\Delta v_c| = \frac{(1-D_{ST})^2}{4R_L C f_s (1-2D_{ST})^2}Vi \quad (35)$$

The voltage and current stress values are necessary factors in proper switch selection especially for practical circuits. By applying KCL and using (33), we have

$$i_{S1} = i_{S2} = i_{L1} + i_{L2} = 2i_L \quad (36)$$

According to (36), the maximum value for switch current ($i_{S1,}$max, $i_{S2,}$max) happens when inductors' current is in its maximum value. By using (31) and (34), we can write

$$i_{S1,}\text{max}=i_{S2,}\text{max}= \frac{(1-D_{ST})[L+R_L D_{ST}(1-2D_{ST})T_S]}{R_L L(1-2D_{ST})^2}Vi \quad (37)$$

For the calculation of maximum voltage stress on S1 (VS1,max) and S2 (VS2,max), KVL is applied and by using (14), we can write

$$V_{S1,}\text{max} = V_{S2,}\text{max} = V_{S,}\text{max} = 2(V_i + V_C) = \frac{2}{1-2D_{ST}}Vi \quad (38)$$

In SOD, for determining appropriate values for capacitors used in the proposed converter we may use allowable voltage ripple range, x_c%, which is defined as

$$x_C\% = \frac{|\Delta v_C|}{V_C} \quad (39)$$

Replacing values of $|\Delta v_C|$ and V_C from (35) and (13) in (39), the rated value of capacitance according to allowable voltage ripple range is defined as

$$C = \frac{(1-D_{ST})^2}{8R_L f_s D_{ST}(1-2D_{ST})x_C\%} \quad (40)$$

By same way, by considering current ripple, the appropriate values of inductances can be calculated. Range of allowable current ripple, x_L%, is defined as:

$$x_L\% = \frac{\Delta i_L}{I_L} \quad (41)$$

Replacing the values of I_L and $|\Delta i_L|$ from (34) and (31) in (41), the rated value of inductances can be calculated as:

$$L = \frac{2R_L D_{ST}(1-2D_{ST})}{f_s x_L\%} \quad (42)$$

IV. Control Method

Simple control technique based on pulse width modulation (PWM) is used to generate trigger pulses for switches. A triangular waveform is used as carrier signal with frequency fs and with magnitude of 1pu at time t=0 and 0pu at t=T/2 is used. Two signals V1 and V2 with constant magnitude are used to know ST state.

$$V_1 = D_{ST}, \; V_2 = 1-D_{ST} \quad (43)$$

Moreover, a sinusoidal signal (v_m) with frequency of f_s and magnitude of 1pu is compared with zero value to obtain a signal (w) with frequency of f_s:

$$\begin{cases} \text{If } v_m < 0 & w = 1 \\ v_m < 0 & w = 0 \end{cases} \quad (44)$$

Signals m1 and m2 are obtained by Comparing triangular

wave forms with V_1 and V_2. From this, the new signals ST_1 and ST_2 are obtained by using (45):

$$ST_1 = m_1 \wedge \bar{w} \quad ST_2 = m_2 \wedge w \tag{45}$$

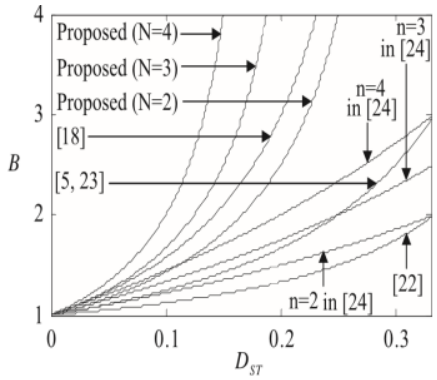
where "$\wedge$" is logical *AND* and $\bar{u}$ is NOT operation of u. By using (45), the switching pulses (G_{s1} and G_{s2}) are extracted as:

$$\text{If } D_2 > D_1, G_{s1} = w, G_{s2} = \bar{w} \vee ST_2 = \bar{w} \vee (m_2 \wedge w) \tag{46}$$

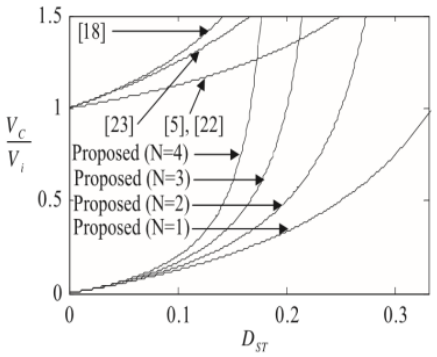
$$\text{If } D_1 > D_2, G_{s1} = w \vee ST_1 = w \vee (m_1 \wedge \bar{w}), G_{s2} = \bar{w} \tag{47}$$

where "$\vee$" is logical OR.

V. Comparison of Proposed Topology with Conventional Inverters



(a)



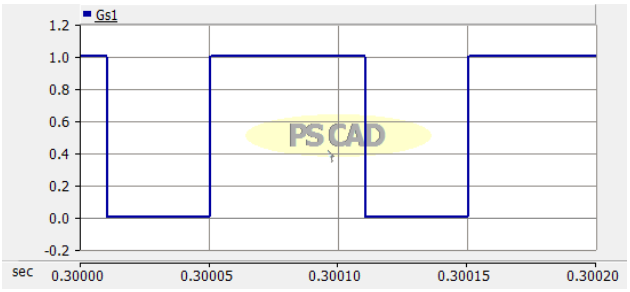
(b)

Fig. 3 Theoretical comparison of proposed and conventional topologies; (a) boost factor (b) voltage stress on capacitors

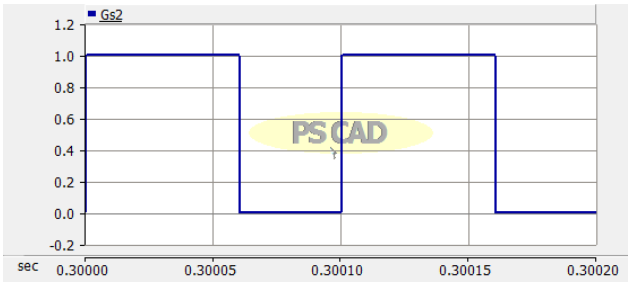
Figs. 3 (a) and (b) give the comparison of boost factor, voltage stress of capacitors with ST duty cycle for proposed topology and conventional topologies. By increasing ST duty cycle, the boost factor is increased. From the figure, the proposed topology has more boost factor compared to others. From Fig. 3 (b), the proposed topology has low voltage stress compared to other conventional topologies.

VI. Simulation Results

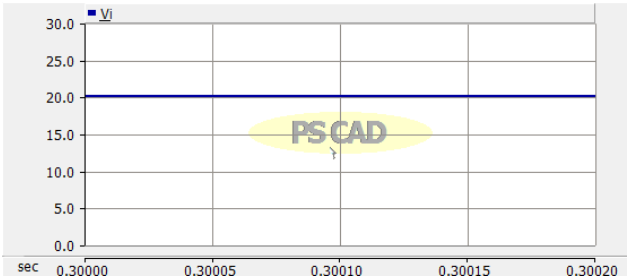
In this section the results of proposed inverter are validated with simulation results by using software PSCAD/EMTDC. Later simulation results are compared with calculated values. The parameter values are given in Table I. And Vi=20V, RL= 14.66 Ω, f_s =10kHz, L=770µH, C=470µF.



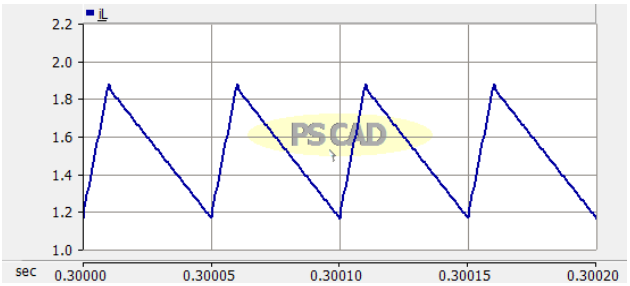
(a) Gate pulse G_{S1}



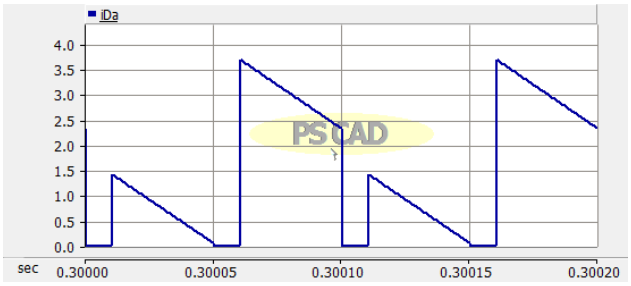
(b) Gate pulse G_{S2}



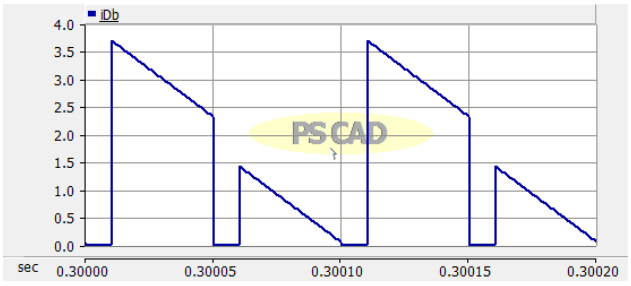
(c) input voltage



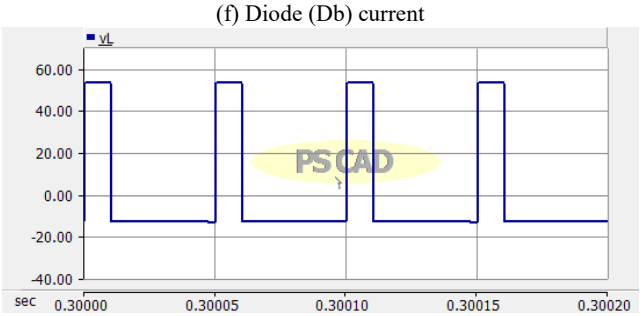
(d) Inductor current



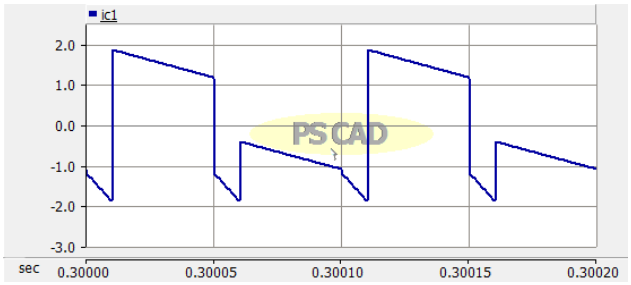
(e) Diode (Da) current



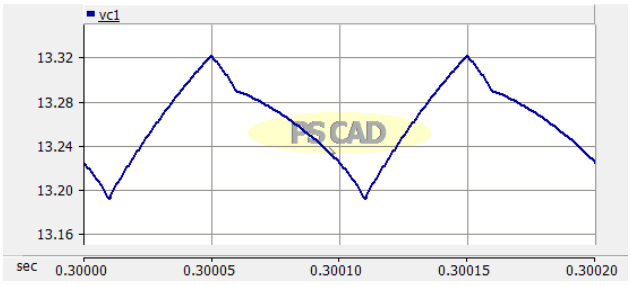
(f) Diode (Db) current



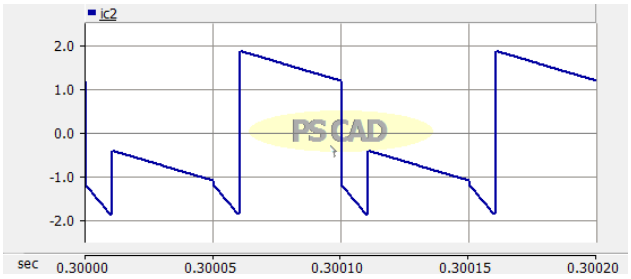
(g) Inductor voltage



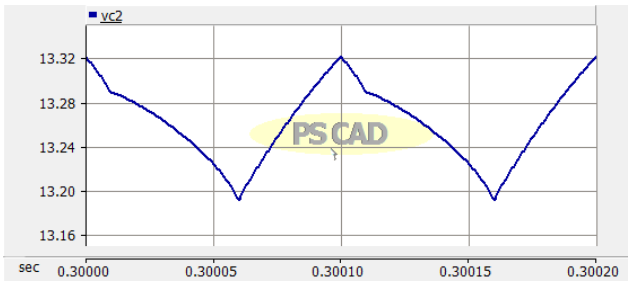
(h) Capacitor (C_1) current



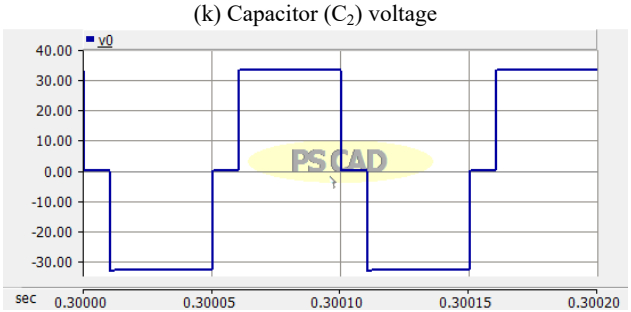
(i) Capacitor (C_1) voltage



(j) Capacitor (C_2) current

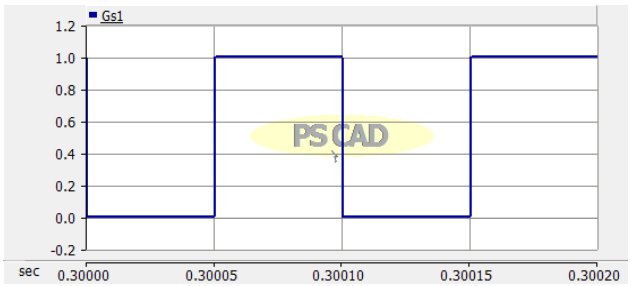


(k) Capacitor (C_2) voltage

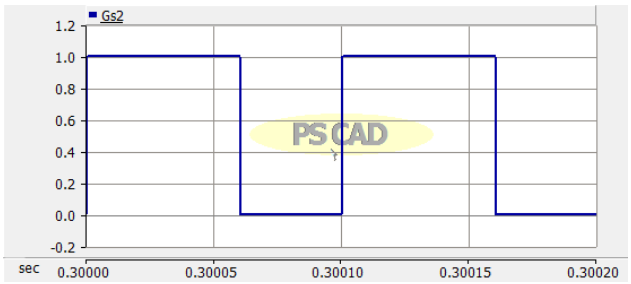


(l) Output voltage

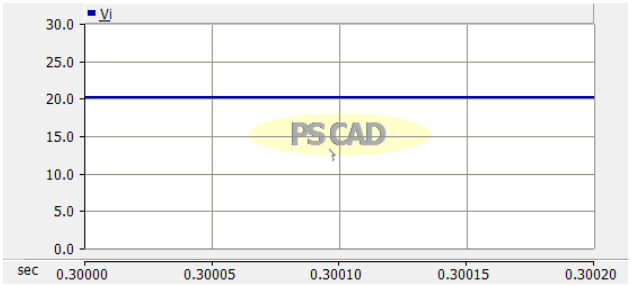
Fig. 4 Simulation waveforms for; $D_1 = 0.6, D_2 = 0.6$



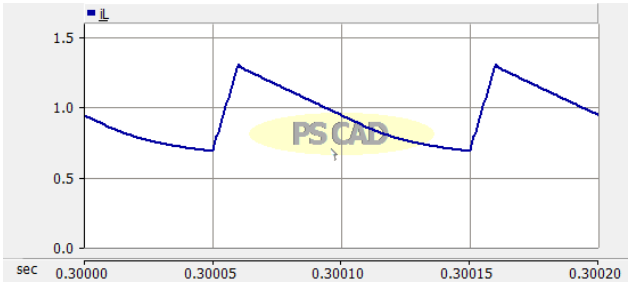
(a) Gate pulse G_{S1}



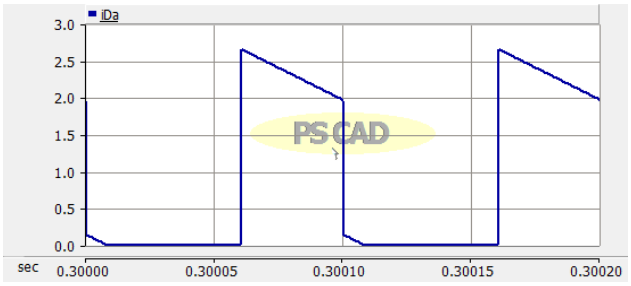
(b) Gate pulse G_{S2}



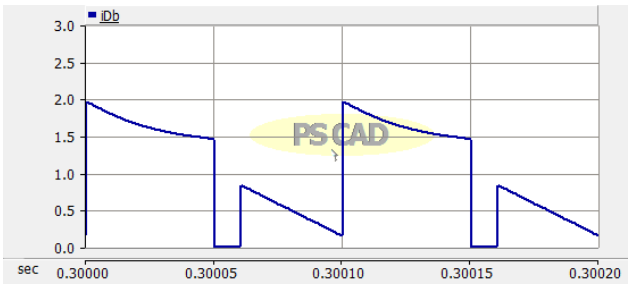
(c) Input voltage



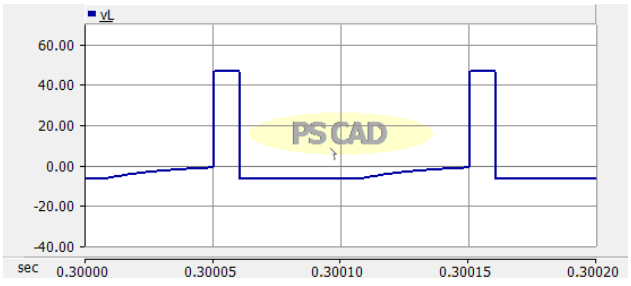
(d) Inductor current



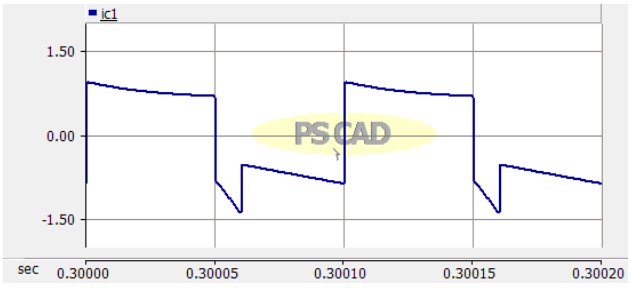
(e) Diode (D_a) current



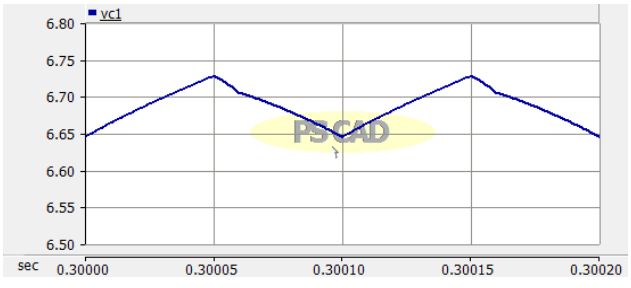
(f) Diode (D_b) current



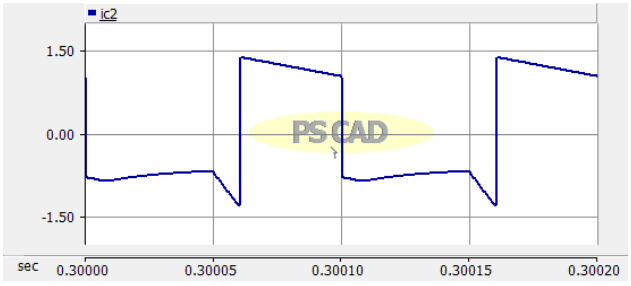
(g) Inductor voltage



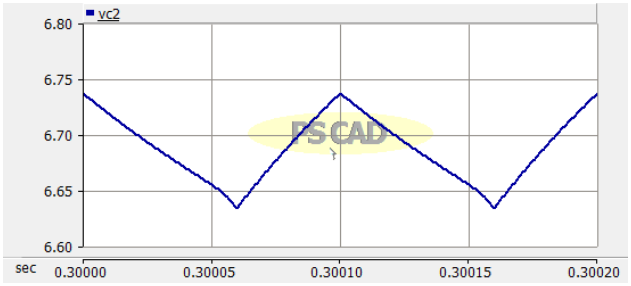
(h) Capacitor (C_1) current



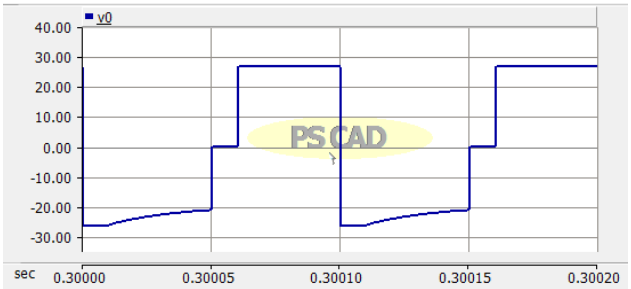
(i) Capacitor (C_1) voltage



(j) Capacitor (C_2) current



(k) Capacitor (C_2) voltage



(l) Output voltage

Fig. 5 Simulation waveforms for; $D_1 = 0.5, D_2 = 0.6$

TABLE I
PARAMETER VALUES

V_i	L	C	x_L%	x_C%	R_L	f_s	D	D_{st}
20V	775µH	470µF	0.454	0.0096	14.66 Ω	10kHz	0.6	0.2

TABLE II
COMPARISON OF RESULTS FOR D1= D2= 0.6

Parameter	Calculated	Simulated	Simulation error (%)
Positive level of output voltage	33.33V	33.25V	0.24
Negative level of output voltage	-33..33V	-33.25V	0.24
Average current of inductors	1.515A	1.500A	0.99
Inductor current ripple	0.688A	0.640A	6.9
Inductor voltage in ST zero state	53.33V	53.15V	0.33
Inductor voltage in non-ST zero state	-13.33V	-13.26V	0.52
Average value of voltage across capacitors	13.33V	13.32V	0.07
Capacitor voltage ripple	0.129V	0.130V	0.77

TABLE III
COMPARISON OF RESULTS FOR D1= 0.5, D2= 0.6

Parameter	Calculated	Simulated	Simulation error (%)
Positive level of output voltage	26.66V	26.64V	0.075
Negative level of output voltage	-26.66V	-26.70V	0.225
Average current of inductors (I_L)	0.9967A	0.99A	0.67
Inductor current ripple (ΔI_L)	0.66A	0.62A	6.06
Inductor voltage in ST zero state (v_L)	46.66V	46.56V	0.21
Inductor voltage in non-ST zero state (v_L)	-6.66V	-6.63V	0.45
Average value of voltage across capacitors (v_C)	6.66V	6.72V	1.35
Capacitor voltage ripple (Δv_C)	0.092V	0.087V	3.26

TABLE IV
COMPARISON OF VOLTAGE STRESS ON CAPACITORS AND BOOST FACTOR

	SL-ZSI	QZSI	ZSI	SBI	CFSI	Half Bridge ZSI
Boost Factor	4	1.66	1.7	1.3	1.66	1.66
Voltage stress across capacitor (V_C)	40	40	27	27	33.2	13.33
Vc/Vi	2	2	1.3	1.3	1.66	0.66
Number of inductors	4	2	2	1	1	2
Number of Capacitors	2	2	2	1	1	2
Number of diodes	11	5	5	6	6	2

VII. CONCLUSION

In this paper, a topology for symmetrical and asymmetrical Z-source half-bridge inverter is presented. The different operating states of proposed inverter are studied. The current ripple of inductor and voltage ripple of capacitor are calculated. The proposed topology produces high voltage gain and capacitor voltage stress is less. The proposed topology produces symmetric and asymmetric voltages by variation of duty cycle with different magnitudes during negative and positive half-cycles. The proposed topology satisfies all characteristics of the conventional H-bridge inverter. Coincidence of simulation results with calculated values confirms the performance of proposed inverter.

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