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Comparison of Different Discontinuous PWM Technique for Switching Losses Reduction in Modular Multilevel Converters

Kaumil B. Shah, Hina Chandwani

***Abstract*—**The modular multilevel converter (MMC) is one of the advanced topologies for medium and high-voltage applications. In high-power, high-voltage MMC, a large number of switching power devices are required. These switching power devices (IGBT) considerable switching losses. This paper analyzes the performance of different discontinuous pulse width modulation (DPWM) techniques and compares the results against a conventional carrier based pulse width modulation method, in order to reduce the switching losses of an MMC. The DPWM reference wave can be generated by adding the zero-sequence component to the original (sine) reference modulation signal. The result of the addition gives the reference signal of DPWM techniques. To minimize the switching losses of the MMC, the clamping period is controlled according to the absolute value of the output load current. No switching is generated in the clamping period so overall switching of the power device is reduced. The simulation result of the different DPWM techniques is compared with conventional carrier-based pulse-width modulation technique.

***Keywords*—**Modular multilevel converter, discontinuous pulse width modulation, switching losses, zero-sequence voltage.

I. Introduction

TODAY, MMC has become one of the most promising multilevel converter topologies for medium/high power applications, like the Voltage-Sourced Converter High-Voltage Direct Current (VSC-HVDC) transmission systems [1]-[3], variable speed motor drive [4], active filters and in STATCOM [5], [6]. In comparison with other multilevel converter topologies, the salient features of the MMC include (i) its modularity and scalability to achieve any voltage level requirements, (ii) its high efficiency which is of significant importance for high-power applications, (iii) low harmonic content due to the high number of output voltage level, thereby the size of passive filters can be reduced, (iv) absence of dc link capacitors, and (v) high degree of modularity and the lowest expense for redundancy due to a large number of cells [7], [8]. The modulation scheme is important because it influences the switching losses, filter size, harmonic content, capacitor voltage ripple and voltage balancing among each submodule.

Various modulation techniques have been proposed like phase shifted [9], level shifted [10], [11], staircase [12], selective harmonic elimination (SHE) [13], nearest level modulation (NLM) [14], [15] and carrier rotation [16], [17]. The disadvantages of the phase shifted and level shifted multi-carrier pulse width modulation (PWM) techniques are that they have high switching losses. In level shifted PWM technique, the harmonics are presented in line-to-line voltage as sidebands around the carrier frequency. In phase shifted PWM technique, to reduce the harmonic content, the N triangle carrier of each arm is shifted by 2Π/N incrementally. Here the optimum angle between upper and lower arm carrier is an analysis of minimizing the harmonic content in output voltage and the circulating current harmonic cancellation [18]. A phase shifted PWM technique generates an effective distribution of power among the sub-module compared to a level shifted PWM technique.

An effective voltage balancing algorithm can be integrated with low frequency modulation to enhance the performance of the phase shifted and level shifted PWM technique. Low-frequency modulation is preferred for MMC, due to high number of output levels. SHE can be applied but the finding of the switching angles becomes complex as the number of level increases [19]. NLM technique is less complex compared to the SHE technique. The quality of the output voltage and current wave in NLM technique distorts more than the carrier base PWM (CPWM) techniques. Level-shifted pulse-width modulation (LSPWM) technique produces better harmonic spectrum in output than that of phase-shifted PWM (PSPWM) technique. Applications of LSPWM are limited because of unequal device conduction periods, which is not acceptable in high-voltage and high-power applications. To generate equal switching and conduction losses, the carrier rotation PWM technique can be used among sub-modules [20]. The DPWM technique is used to minimize the switching losses by reducing the switching operation in a fundamental cycle. It is based on clamping one arm of the converter to a non-switching condition. This clamping effect is generated by addition of a zero-sequence component to the sine reference signal. Here the clamping period is of constant duration. In this paper, performance of different DPWMs are compared. Different DPWM techniques are classified based on discontinuous periods such as 30°, 60° and 120° DPWM. This paper presents the performance comparison of the carrier based PWM and different discontinuous PWM. The different DPWM techniques give a significant reduction in switching loss compared to conventional PWM techniques. The remaining

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paper is organized as follows. Section II explains the principles of operation of the MMC. Section III describes the DPWM technique and Section IV shows the comparison of the simulation results.

II. Basic of the MMC

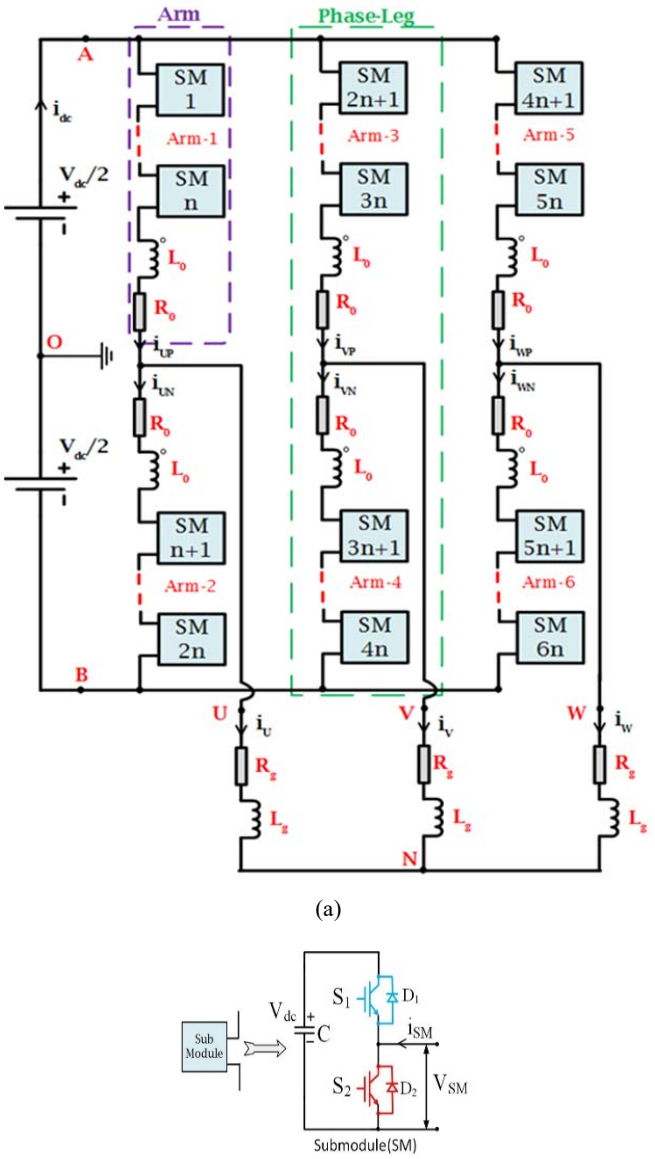


Fig. 1 (a) Circuit diagram of a three-phase MMC with N-SMs per arm (b) Sub module structure

Fig. 1 shows the circuit diagram of a three-phase MMC structure, which is energized by the DC source. The topology consists of two arms per phase-leg where each arm is made of N series-connected, identical sub-modules (SMs) and a series arm inductor L_o and arm resistance R_o. Each phase has two arms, upper and lower. Arm-1,3,5 are the upper arm and Arm-2,4,6 are the lower arm. This MMC is half-bridge sub-modules (HB-SMs) base. In each SM there is a one electrolytic capacitor C and two IGBTs (S_1, S_2). The output voltage at the terminal of the SMs (V_{SM}) has two values: its capacitor voltage (V_c) when S_1 is ON and S_2 is OFF and zero when S_1 is OFF and S_2 is ON. The series connected arm inductor is used to control the circulating current within the phase-leg and to limit the fault current.

Table I shows the switching condition of each power switch in a sub-module show in Fig. 1 (b).

TABLE I
SWITCHING STATE OF EACH SM

S_1	S_2	V_{SM}	Current Direction	Power Path	Capacitor State.
Off	On	0	$i_{SM} > 0$	S_2	Unchanged
Off	On	0	$i_{SM} < 0$	D_2	Unchanged
On	Off	V_{dc}	$i_{SM} > 0$	D_1	Charging
On	Off	V_{dc}	$i_{SM} < 0$	S_1	Discharging

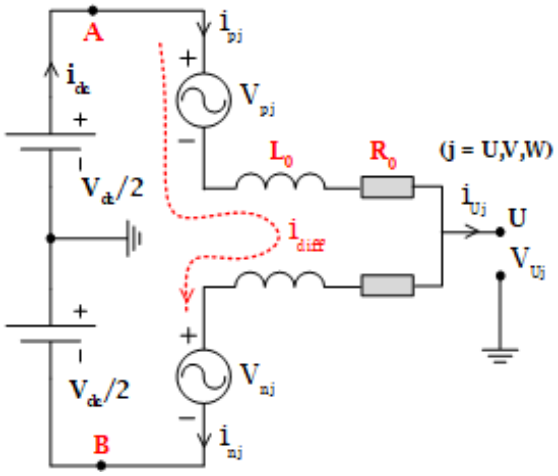


Fig. 2 Equivalent Circuit diagram of MMC

Fig. 2 shows the single-phase equivalent circuit diagram of the MMC. The DC voltage source is center earthed. V_{dc} is the total DC bus voltage and I_{dc} is dc current. R_o and L_o are the arm equivalent resistance and arm inductance respectively. V_{Uj} (j= U,V,W) is the output voltage of the converter at the j phase and i_{Uj} (j= U,V,W) is the converter output current. Addition of each sub module voltage generates total arm voltage and it is denoted as V_{pj} & V_{nj}, where p and n denote the upper and lower arm respectively. The arm current can be express as

$$i_{pj} = i_{diff} + \frac{i_{Uj}}{2} \tag{1}$$

$$i_{nj} = i_{diff} - \frac{i_{Uj}}{2} \tag{2}$$

where i_{diff} is the inner current of the phase j, which flows through both the upper and lower arms.

$$i_{diff} = \frac{(i_{pj} + i_{nj})}{2} \tag{3}$$

$$V_{Uj} = e_j - \frac{R_o}{2} i_{Uj} - \frac{L_o}{2} * \frac{d\, i_{Uj}}{d\, t} \quad (4)$$

where e_j is the inner e.m.f generated in the phase j and is expressed as

$$e_j = \frac{V_{nj} - V_{pj}}{2} \quad (5)$$

In MMC, n sub module in each arm can generate the (n+1) level of voltage at output with respect to midpoint of DC source. Each sub module capacitor voltage is ideally regulated at V_{dc}/n by using active voltage-balancing technique. The terminal voltage of any phase at ac-side of MMC is formulated as

$$V_{Uj} = \frac{n_{lowj} - n_{upj}}{2n} * V_{dc} \quad (6)$$

where V_{Uj}, $j = U,V,W$ is the output voltage at ac-side of the MMC. n_{lowj} and n_{upj} are the total no of sub module which will be turn on in lower and upper arm respectively. n is total no of sub module in each arm. The output voltage V_{Uj} varies stepwise in the range of $V_{dc}/2$ to $-V_{dc}/2$ with a step size of V_{dc}/n. To obtain the specific level of voltage at the output side specific no of SMs in the upper and lower arms (i.e. n_{upj} and n_{lowj}) should be turn on. For each level of voltage there is a different switching combination of switches.

III. Discontinuous Modulation

The key objective of using discontinuous modulation in converter application is to reduce the switching losses. The DPWM can be generated by injecting zero-sequence component into the reference of the three-phase converter. The zero-sequence component generated in such manner that the final reference signal generated is clamped to the upper or lower terminal of the dc-link for a specific period (Fig. 3). Fig. 3 (a) shows the three reference phase voltages (V_{rs}^*, V_{ys}^* ,V_{bs}^*), Fig. 3 (b) shows the obtain zero-sequence component (V_{z_seq}.) and Fig. 3 (c) shows the final reference voltage for DPWM operation (V_{rd},V_{yd},V_{bd}).The DPWM references are generated by adding each reference phase voltage and the zero-sequence voltage. The zero-sequence voltage is calculated by (7):

$$V_{z\_seq} = \begin{Bmatrix} +\frac{V_{dc}}{2} - V_{max};\ |V_{max}| > |V_{min}| \\ -\frac{V_{dc}}{2} - V_{min};\ |V_{max}| < |V_{min}| \end{Bmatrix} \quad (7)$$

$$V_{max} = \max(V_{rs}^*, V_{ys}^*, V_{bs}^*)$$
$$V_{min} = \min(V_{rs}^*, V_{ys}^*, V_{bs}^*) \quad (8)$$

The DPWM reference voltages are express as:

$$V_{jd} = V_{js}^* + V_{z\_seq.} \quad , j = r, y, b. \quad (9)$$

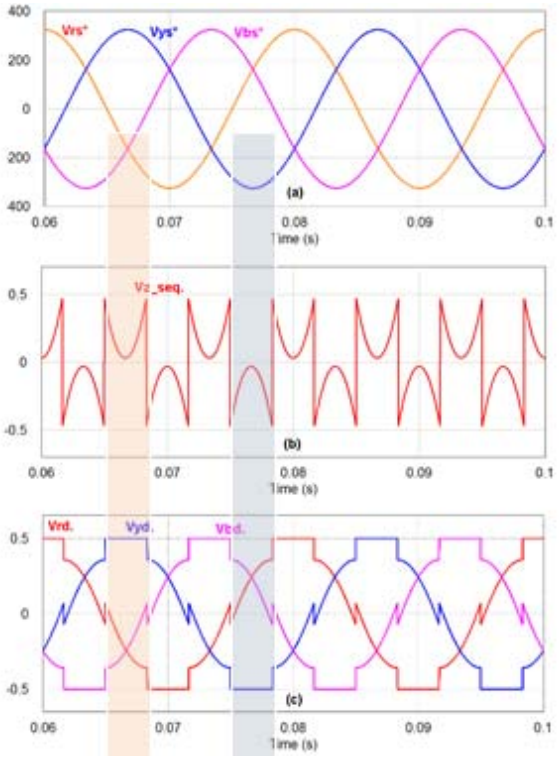


Fig. 3 (a) Reference Voltage (b) Zero-sequence Component (c) DPWM Reference

The modulation signal for upper arm and lower arm are derived as:

$$V_{jd\_u} = \frac{V_{dc}}{2} - (V_{js}^* + V_{z\_seq})$$

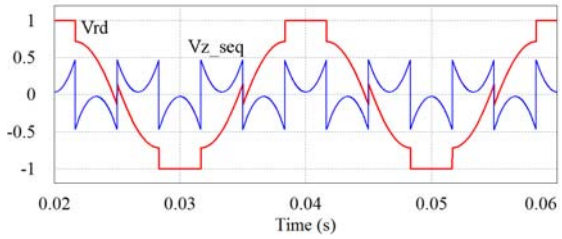
$$V_{jd\_l} = \frac{V_{dc}}{2} + (V_{js}^* + V_{z\_seq}) \quad (10)$$

In this DPWM reference, the switching device of each SM does not perform switching operation during the clamping period when the phase voltage has the greatest magnitude in a fundamental period. Furthermore, it is observed from Fig. 3 (c) that there is always one phase-leg that is not switching for a specific period. Thus the average switching frequency of the power device is reduced. A number of discontinuous modulation techniques has been developed for converters [21], [22]. Here discontinuous modulation is used for the MMC. So all the SMs of one arm of a particular phase-leg are bypass for some intervals that is due to discontinuous modulation. Due to that, phase-leg is clamped to the upper or lower dc-bus terminals for that interval. One arm of the converter is not switching during those intervals. At the end, switching power loss is reduced. Discontinuous modulation also reduces the capacitor voltage ripple amplitudes. Arm currents are divided according to the value of the equivalent capacitances of that arm, as:

$$C_{ju} = \frac{C}{u} \; ; \; C_{jl} = \frac{C}{l} \tag{11}$$

$$i_{ju} = i_j \frac{C_{ju}}{C_{ju} + C_{jl}} \quad i_{jl} = i_j \frac{C_{jl}}{C_{ju} + C_{jl}} \tag{12}$$

The numbers of SMs to be activated in the upper and lower arms are defined as *u and l*. Equation (12) shows that the larger the total capacitance in a specific arm, the more output current passes through that arm. During operation when a phase-leg of the MMC is clamped to a dc-link, the arm which is clamped offers an infinite equivalent capacitance that can be calculated by the substituting *u* or *l* by zero in (11). No current will be circulated through the unclamped arm of the phase-leg, as per (12) that results in a reduction in capacitor voltage ripples. Fig. 4 shows the different DPWM reference wave generated with its corresponding zero sequence component. Here the clamping period of the DPWM reference wave depends on load angle [26], [27].



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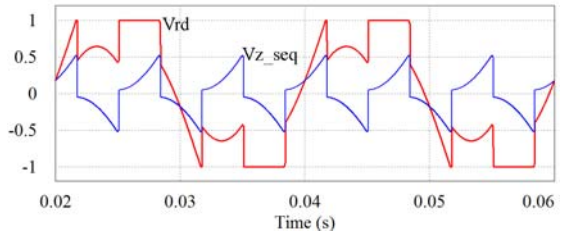

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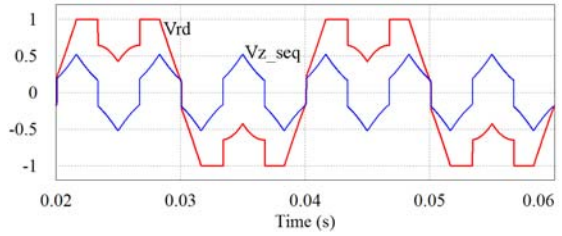


(c)

Fig. 4 Simulated DPWM Reference Wave with its zero-sequence component for different load angle (a) DPWM1 (b) DPWM2 (c) DPWM3

Fig. 4 (a) shows the DPWM1 reference wave in which centre part of the wave is clamped in both positive and negative cycle. Figs. 4 (b), (c) show the DPWM2 and DPWM3 reference wave with different load angles [24], [25]. This DPWM reference wave results in the reduction of the switching loss. In Figs. 4 (a)-(c) red waveform shows the DPWM reference wave and blue waveform show the zero sequence component [22], [23]. Reduction in capacitor ripples voltages and the switching loss of the MMC can be achieved by varying the clamping period of the DPWM wave, which can be varied by the load angle. Here the algorithm clamps the phase leg that carries more output current. The phase-leg with the maximum absolute value of the current can be clamped corresponding to either maximum or minimum value of the reference signals.

Fig. 5 shows the flowchart of the generation of the zero-sequence component and DPWM reference wave. First the reference signal (V_{rs}^*, V_{ys}^* ,V_{bs}^*) and output current (I_r, I_y, I_b) enter into the algorithm, it finds the MAX. and MIN. values of the voltage and current signal. This reference voltage is used to determine a prohibitive phase that should not be clamped to avoid over modulation.

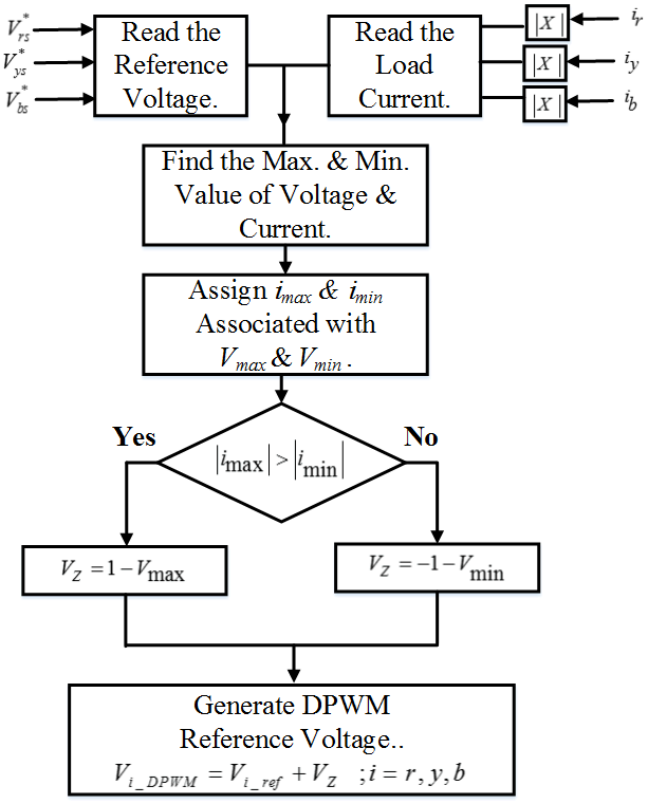


Fig. 5 Flowchart for zero-sequence voltage generation

The prohibitive phase which should be prevented from being clamped corresponds to the phase with a medium voltage (V_{mid}). Therefore the algorithm excluded V_{mid} from the process to generate the zero-sequence voltage. After that, one of the two legs related with V_{max} and V_{min} must be clamped to either positive or negative dc-link, depending on which phase leg conducts a larger load current.

At last by putting condition on max and min value of the current, algorithm will find the zero-sequence component for

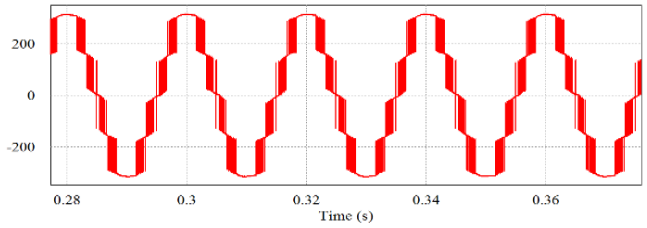
the reference DPWM wave. By adding this zero-sequence component to the reference signal gives the DPWM reference wave.

IV. Simulation Results

Simulation has been done in PSIM software to verify the performance of the said different DPWM technique for MMC. Here the MMC with four SMs per arm (N=4) is simulated. Three different types of the DPWM reference wave are generated called as DPWM1, DPWM2, and DPWM3. The main data of simulated MMC are given in Table II. Switching of SMs switch can be prevented by the algorithm shown in Fig. 5 during the clamping period. In addition, the clamping period generated by the algorithm moves depending upon the load angle.

TABLE II
Simulation Parameters

DC Bus Voltage ($V_{dc}/2$)	340 V
DC Resistance ($R_{dc}/2$)	0.1 Ω
Number of Sub module per Arm (N)	04
SM Capacitance (C)	4000 µF
Arm Inductance (L_o)	5 mH
Sub Module Capacitor Voltage (V_c)	200V
Carrier frequency (f_{cr})	1 KHz
Sampling & Control Frequency (f_s)	10 KHz
Reference Signal Frequency (f_r)	50 Hz
Load-1 (DPWM1)	R= 12 Ω, L= 10 mH
Load-2 (DPWM2)	R= 12Ω, L= 25mH
Load-3 (DPWM3)	R= 0.3218Ω, L= 50mH



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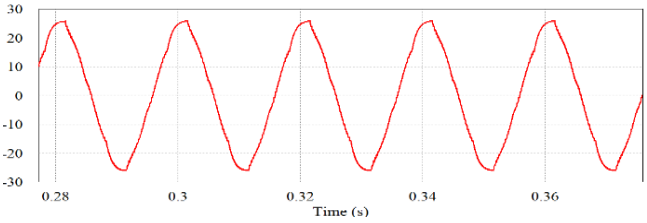

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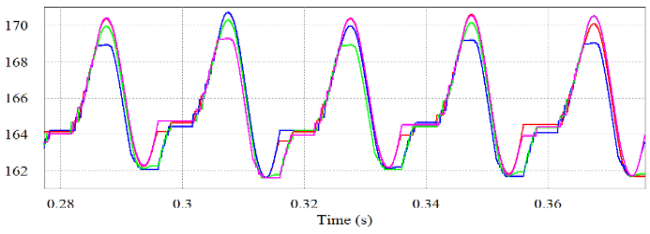

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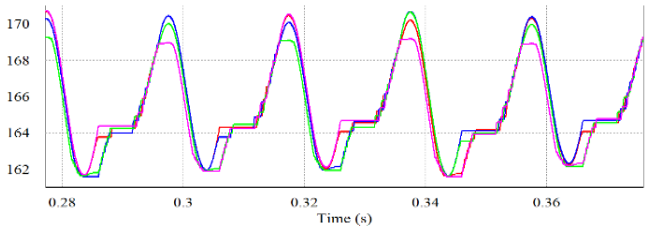

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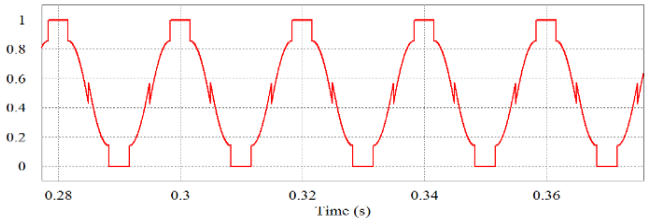

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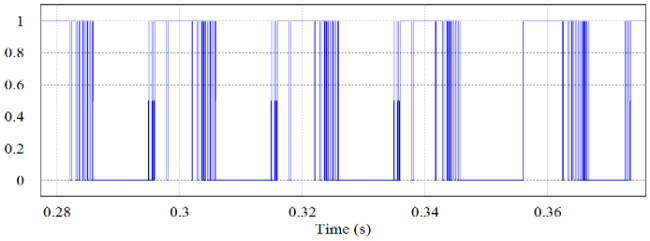

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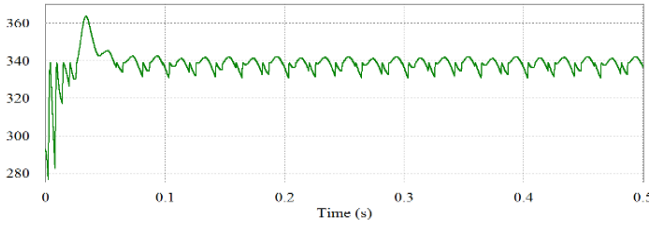
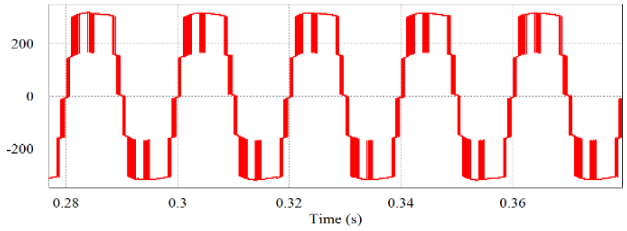


(g)

Fig. 6 (a) Phase Voltage (230 V), (b) Phase Current (17.77 A, 4.42% THD), (c) Upper Arm Capacitor Voltages, (d) Lower Arm Capacitor Voltages, (e) Reference DPWM Wave (DPWM1), (f) Gating signal of SM1 (g) DC link Voltage with load R= 12 Ω, L= 10 mH

Fig. 6 shows the results of the DPWM1 technique in which the center portion of the clamping period is aligned with the peak of the current and voltage reference wave. The described algorithm can also generate the DPWM2 and DPWM3 for a different clamping period. Figs. 6 (a), (b) show the five-level phase voltage and phase current. Figs. 6 (c), (d) show the capacitor voltages of the upper arm and lower arm capacitor, which oscillates between 162 V and 170 V. This upper and lower arm capacitor voltages are balanced by the balancing algorithm. Figs. 6 (e), (f) show the DPWM reference wave with its corresponding gating pulse generated for the first SM of MMC of a leg. Fig. 6 (g) shows the dc link voltage of the converter.



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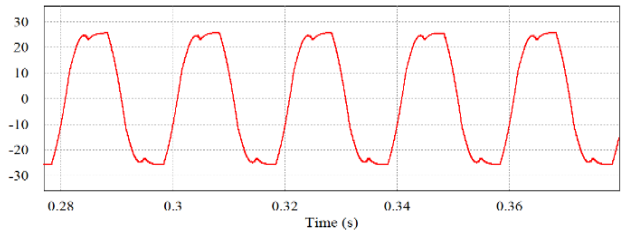

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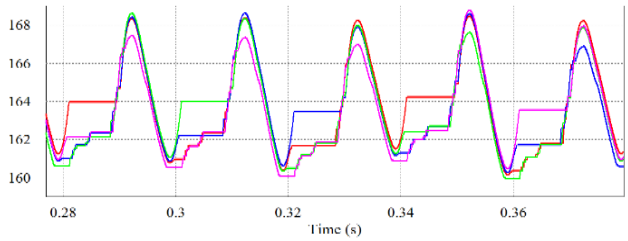

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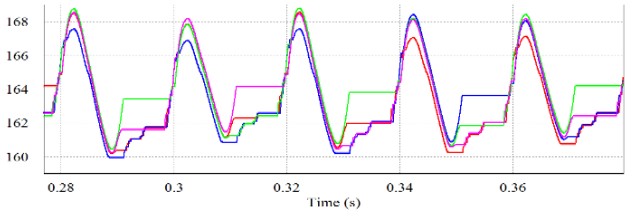

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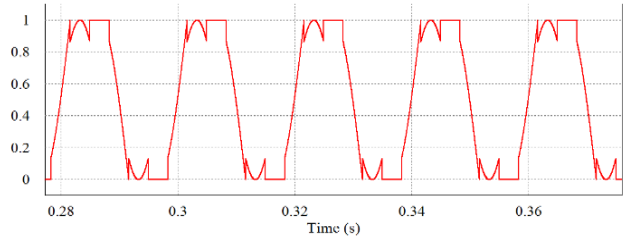

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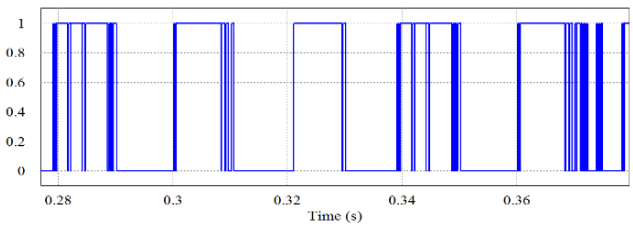

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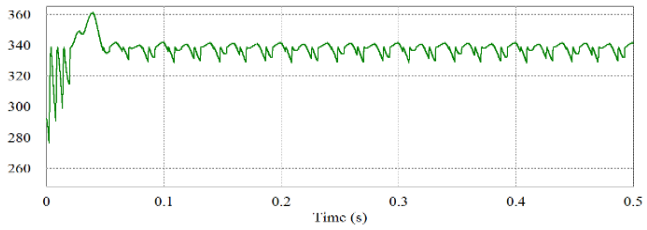
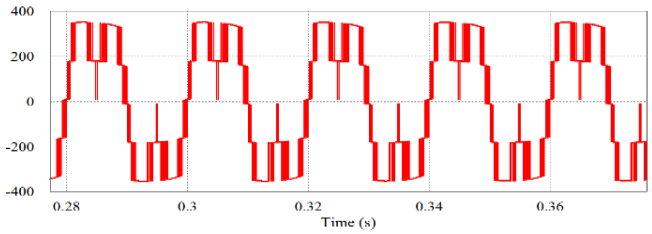


(g)

Fig. 7 (a) Phase Voltage (230 V), (b) Phase Current (20.84 A, 15.86% THD), (c) Upper Arm Capacitor Voltages, (d) Lower Arm Capacitor Voltages, (e) Reference DPWM Wave (DPWM2), (f) Gating signal of SM1 (g) DC link Voltage with load R= 12Ω, L= 25 mH

Fig. 7 shows the simulation results for DPWM2 reference wave. Fig. 7 (a) shows the 5 level phase voltage. Fig. 7 (b) shows the output phase current of the MMC. These results are for different values of the load compared to the result shown in Fig. 6. Here the load became more inductive. Figs. 7 (c), (d) show the capacitor voltages of upper arm and lower arm. Fig. 7 (e) shows the DPWM2 wave generated for the different load angle. Fig. 7 (f) shows the gating pulse of the SM1of the converter.



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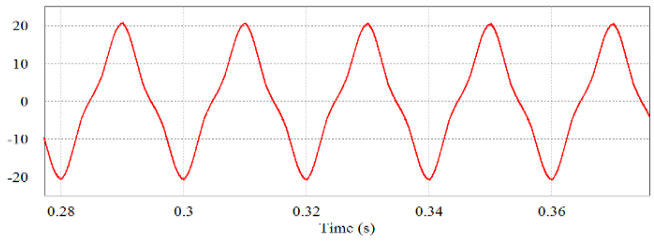

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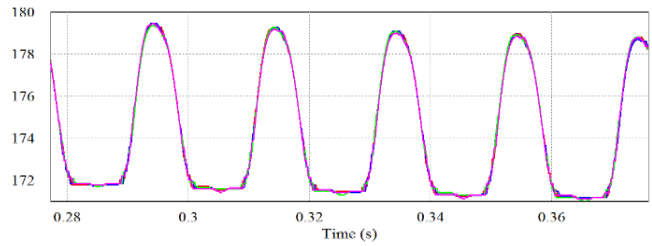

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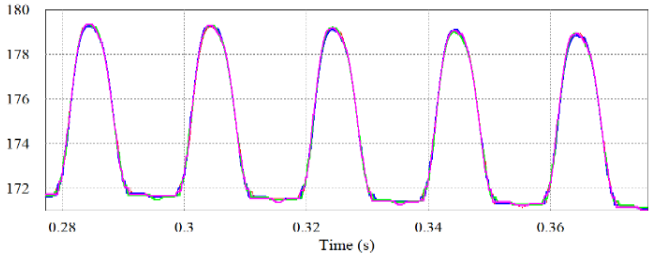

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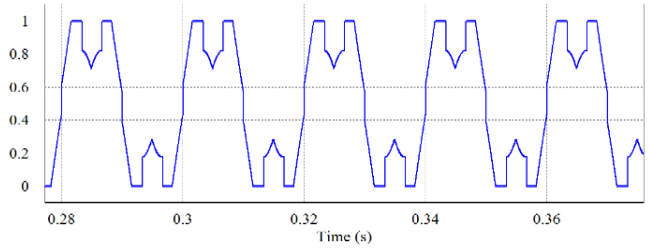
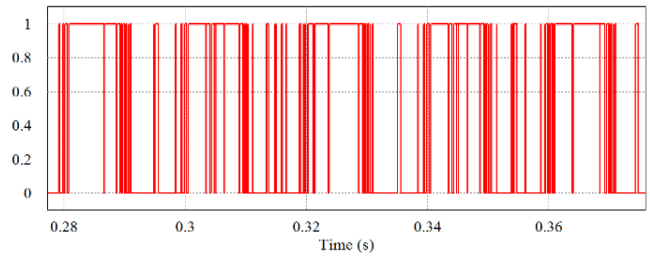
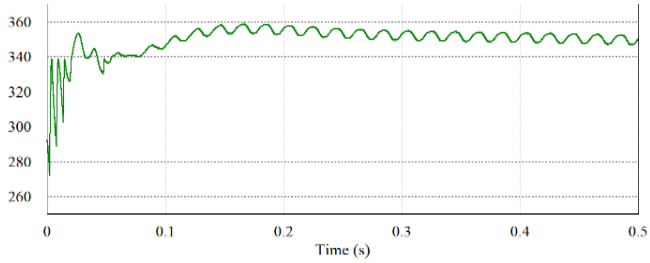


(e)



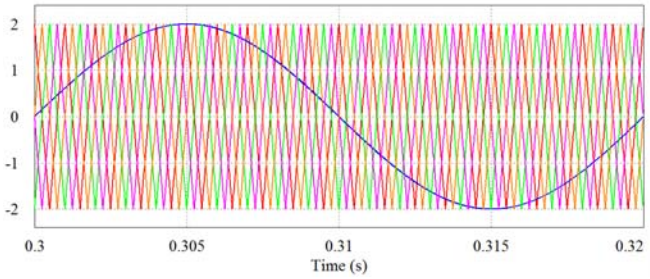
(f)



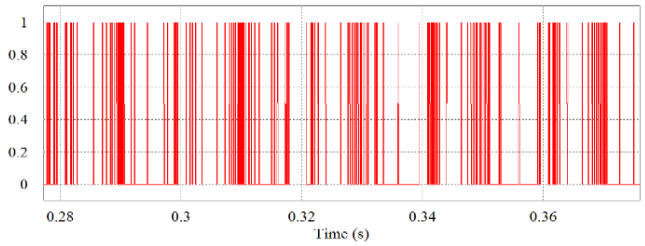
(g)

Fig. 8 (a) Phase Voltage (230 V), (b) Phase Current (12.64 A, 16.61% THD), (c) Upper Arm Capacitor Voltages, (d) Lower Arm Capacitor Voltages, (e) Reference DPWM Wave (DPWM3), (f) Gating signal of SM1 (g) DC link Voltage with load R= 0.3218Ω, L= 50 mH

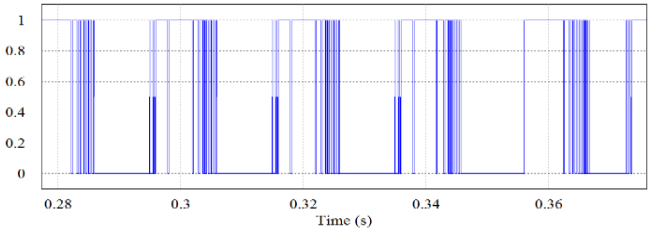
Figs. 8 (a), (b) show the phase voltage and phase current for DPWM3 technique. Figs. 8 (c), (d) show the capacitor voltages of the upper arm and lower arm respectively. It shows that the voltage balancing between the capacitors is effective compared to other DPWM technique. Fig. 8 (e) shows the DPWM3 reference wave generated for a specific load angle. Gating pulse of the sub-module 1 (SM1) is shown in Fig. 8 (f).



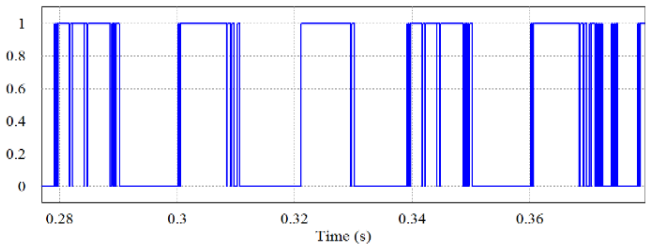
(a)



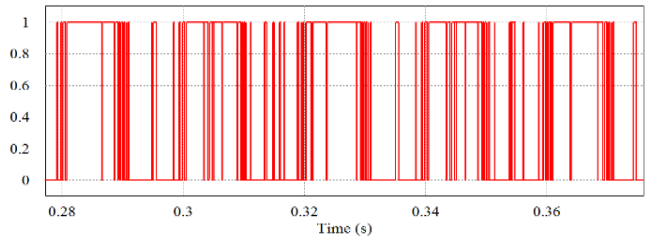
(b)



(c)



(d)



(e)

Fig. 9 (a) Phase shifted carriers and sine reference (b) Gating pulse for PS-PWM technique (c) Gating pulse for DPWM1 (d) Gating pulse for DPWM2. (e) Gating pulse for DPWM3

Fig. 9 shows the comparison of the gating pules for the different PWM techniques. Fig. 9 (a) shows the Phase shifted

PWM technique (PS-PWM) in which one sine reference and four triangles are compared to generate the PWM pulse. Fig. 9 (b) shows the gating pulse generated for the SM1 using PS-PWM technique. The triangle carrier signal has a frequency of 1 KHz. Figs. 9 (c)-(e) show the different gating pulse generated for the SM1 using DPWM1, DPWM2, and DPWM3 respectively. This comparison of PWM signals shows that the switching frequency of different PWM signal of DPWM techniques varies depends on the clamping period. Compared to conventional PS-PWM, DPWM technique gives a reduction in switching loss of the MMC.

V. Conclusion

In this paper, a discontinuous modulation technique with different load angles has been presented. Discontinuous modulation results in a reduction of the switching power losses. This discontinuous modulation technique is based on clamping the phase-leg with the maximum output current to the upper or lower arm terminal of the dc-link. Here two algorithms, capacitor voltage balancing and generation of clamping period, are used in the simulation. Simulation results show the effectiveness of this technique, which reduces the switching losses. Different DPWM reference waves are generated based on the load angle. This DPWM reference waves give the reduced switching operation of the MMC.

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