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CMOS Positive and Negative Resistors Based on Complementary Regulated Cascode Topology with Cross-Coupled Regulated Transistors

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***Abstract*—**Two types of floating active resistors based on a complementary regulated cascode topology with cross-coupled regulated transistors are presented in this paper. The first topology is a high swing complementary regulated cascode active resistor. The second topology is a complementary common gate with a regulated cross coupled transistor. The small-signal input resistances of the floating resistors are derived. Three graphs of the input current versus the input voltage for different aspect ratios are designed and plotted using the Cadence Spectre 0.18-µm Rohm Semiconductor process. The total harmonic distortion graphs are plotted for three different aspect ratios with different input-voltage amplitudes and different input frequencies. From the simulation results, it is observed that a resistance of approximately 8.52 MΩ can be obtained from supply voltage at ±0.9 V.

***Keywords*—**Complementary common gate, complementary regulated cascode, current mirror, floating active resistors.

I. Introduction

An active resistor is a transistor circuit whose input resistance has a real part, which is constant as a function of the input frequency, even though it is not in reality because of the parasitic capacitances of the transistor network. An active resistor circuit can be substituted into a resistor block diagram to implement an analog circuit such as a 2nd-order RLC filter. Even though the input impedance of the transistor circuit has an imaginary part, it might be necessary to perform input impedance matching so that the imaginary part disappears and the frequency response of the entire circuit such as a filter does not deviate from the ideal frequency response. Bilotti [1] proposed a grounded resistor based on an MOS transistor operating in the triode region. Han [2] proposed a voltage-controlled linear resistor that used two MOS transistors operating in the triode region, which showed a harmonic distortion of only 2.7%.

Nagaraj [3] proposed a floating resistor based on a parallel configuration of a differential transconductance amplifier and a source-degenerated active resistor with the drain connected to a current mirror. Singh [4] proposed a floating resistor using CMOS technology on the basis of two circuit diagrams. The first circuit diagram had 16 transistors with eight diodes connected in a current-mirror configuration. The advantage of this circuit was that it was self-biased and did not require additional voltage references. The second diagram had 32 transistors with 16 diodes connected in a cascode current-mirror configuration.

A grounded voltage-controlled resistor was proposed by Wilson [5]. The circuit used a technique called linearization to cancel the term containing the square of the voltage so that the nonlinear term could be minimized. A CMOS floating voltage-controlled negative resistor was proposed by Surakampontorn [6]. The circuit used nonlinearity cancellation with a bias voltage source to cancel the term containing the square of the voltage. A floating resistor that was independent of the threshold voltage was proposed by Sakurai [7], and a voltage-controlled resistor in the floating form was proposed by Senani [8]. These circuits used a single operational amplifier, five resistors, and a single JFET. Popa proposed a low-area tunable CMOS resistor with improved linearity [9]. It acted as an active resistor in the range of 300 kΩ to 3 MΩ with an applied voltage of ±3.6 V.

The circuit proposed in this paper is based on a regulated cascode amplifier configuration published by Hosticka [10]. The circuit is similar to the one in [10], except that the gates of input transistors M1, M2, M7, and M8 are not connected directly to an input signal; rather, they are biased with the voltage reference from the gates of transistors M14 and M17, as shown in Fig. 1.

The remainder of this paper is organized as follows. Section II describes the circuit connections of the floating input resistance based on a regulated cascade configuration with regulated cross-coupled transistors. Section III describes the simulation results of two additional circuits of floating input resistors based on the complementary common-gate configuration with regulated cross-coupled transistor feedback. Finally, Section IV concludes this paper.

II. Input Resistance of CMOS Complementary Regulated Cascode-Based Floating Resistor

A. Low-Frequency Small-Signal Equivalent Circuit

The floating CMOS resistor circuit based on a complementary regulated cascode configuration is presented in this section. NMOS transistors are employed as input transistors because they use high-swing regulated current mirrors. A circuit analysis demonstrates that this circuit acts as a negative resistor. However, it can also act as a bandpass amplifier because the regulated transistors can form a gyrator loop, which can act as an inductor. The NMOS regulated transistor is connected to a

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PMOS regulated transistor, forming a cross-coupled regulated transistor. The PMOS input transistor is connected in the common-gate cascade configuration with a common-source PMOS transistor. The floating input resistance of the proposed circuit can be analyzed by applying Kirchhoff's current law at all nodes in Fig. 1. The result is as follows (some related coefficients obtained from back-substitution are neglected because of space constraints):

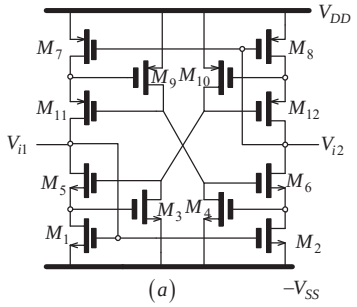

Fig. 1 (a) Proposed circuit diagram

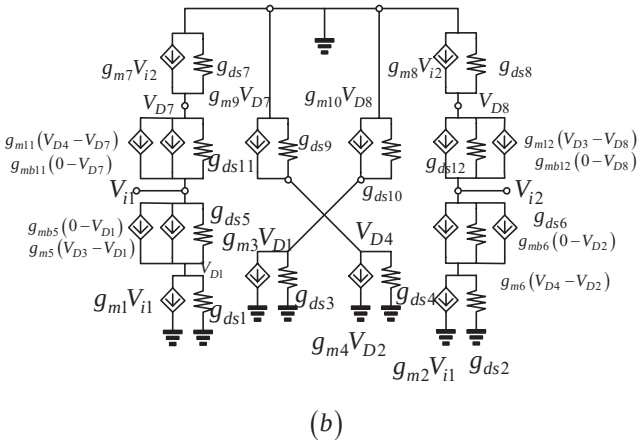

Fig. 1 (b) Low-frequency equivalent circuit of Fig. 1(a)

The parameters *a*, *b*, and *c*, which have subscripts, are a group of small-signal parameters such as the transconductances and conductances of the transistors in Fig. 1. The transconductance subscripts and conductance subscripts correspond to the same subscript of the transistor label. For instance, g_{m1}, g_{ds1} correspond to the transconductance and drain–source conductance of transistor M_1.

$$R_{in1} = \frac{g_{57}}{a_1}, R_{in2} = \frac{g_{58}}{a_{10}} \quad , \tag{1}$$

$$\begin{aligned} &a_1 = g_{m1} - g_{ds5}, a_2 = g_{ds1} + g_{mb5} + g_{m5} + g_{ds5} \\ &a_3 = g_{m5}, a_4 = g_{ds5} + g_{ds11} \\ &a_5 = g_{mb5} + g_{m5} + g_{ds5} \\ &a_6 = g_{m5}, a_7 = g_{m11}, a_8 = g_{m11} + g_{mb11} - g_{ds11} \\ &a_9 = g_{ds11}, a_{10} = g_{m7}, a_{11} = g_{m11} \\ &a_{12} = g_{m11} + g_{mb11} - g_{ds7} - g_{ds11} \end{aligned} \quad , \tag{2}$$

$$\begin{aligned} &b_1 = g_{m2} - g_{ds6}, b_2 = g_{ds2} + g_{mb6} + g_{m6} + g_{ds6} \\ &b_3 = g_{m6}, b_4 = g_{ds6} + g_{ds12}, b_5 = g_{mb6} + g_{m6} + g_{ds6} \\ &b_6 = g_{m12}, b_7 = g_{m6}, b_8 = g_{m12} + g_{mb12} - g_{ds12} \\ &b_9 = g_{ds12} + g_{m8}, b_{10} = g_{m12} \\ &b_{11} = g_{m12} + g_{mb12} - g_{ds8} - g_{ds12} \end{aligned} \quad , \tag{3}$$

and

$$\begin{aligned} &c_1 = g_{m3}, c_2 = g_{ds3} - g_{ds10}, c_3 = g_{m10} \\ &c_4 = g_{m4}, c_5 = g_{ds4} - g_{ds9}, c_6 = g_{m9} \end{aligned} \quad . \tag{4}$$

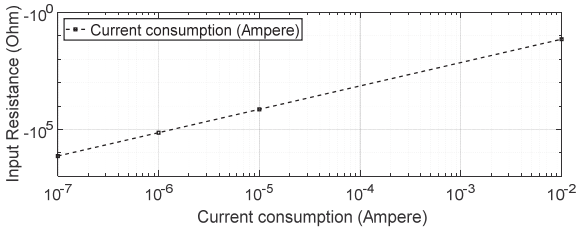

Fig. 2 Current consumption versus input resistance of the proposed circuit

Fig. 2 presents a plot of the current consumption versus the input resistance. The graph indicates that the input resistance increases from the most negative value of −1.39 MΩ at a current consumption of 100 nA to the least negative value of −13.92 Ω at a current consumption of 10 mA. The typical process parameters are as follows: $\mu_n = 506 \times 10^8 \frac{\mu m^2}{V \times s} = 506 \frac{cm^2}{V \times s}$, where μ_n is the electron mobility; $\mu_p = 115 \times 10^8 \frac{\mu m^2}{V \times s} = 115 \frac{cm^2}{V \times s}$, where μ_p is the hole mobility; and $C_{ox} = 3.63 \times 10^{-15} \frac{F}{\mu m^2}$, where C_{ox} is the capacitance per unit area.

III. Simulation Results of the Proposed Floating CMOS Resistor

Two additional CMOS floating resistors are presented in Fig. 3. The proposed circuit has a higher input resistance because of the complementary common gate with regulated transistor cross-coupling. The first version of the CMOS floating resistor has two current sources inserted at the source nodes of the regulated NMOS and PMOS transistors. Each current source is biased with the same branch current but with a different reference voltage.

The current–voltage curves of the CMOS floating active resistor are shown in Fig. 4 for the case where all NMOS transistors have an aspect ratio of 1 μm/0.18 μm and all PMOS transistors have an aspect ratio of 4 μm/0.18 μm. The slope of this graph, which gives the active resistor value, can be approximated to be 3.05 MΩ. The current–voltage curves of the CMOS floating active resistor are shown in Fig. 5 for the case where all NMOS transistors have an aspect ratio of 1 μm/1 μm and all PMOS transistors have an aspect ratio of 4 μm/1 μm. The slope of this graph can be approximated to be 8.52 MΩ. The current–voltage curves of the CMOS floating active resistor are

shown in Fig. 6 for the case where all NMOS transistors have an aspect ratio of 12 μm/0.18 μm and all PMOS transistors have an aspect ratio of 50 μm/0.18 μm. The slope of this graph can be approximated to be 425 kΩ.

A current–voltage curve can be plotted by assuming that there is a current difference between the input nodes (or output nodes), which are the drain nodes of transistors M11, M5, M12, and M6 and can be shown to be a function of the input voltage. The DC operating point can be computed by assuming that there is no offset current at the output node.

The input voltage at the terminals between Vin+ and Vin- can be increased by 0.1 V per step from 0.1 to 0.9 V, which is the maximum supply voltage. Consequently, the drain–source voltages and drain currents of PMOS transistor M11 is reduced. Moreover, the drain–source voltages of NMOS transistor M5 is assumed to increase by 0.1 V per step. As a result, the drain–source voltages and drain currents of NMOS transistor M5 is increased. Thus, the offset current will be the current difference between the drain currents of M5 and M11, which flow through the voltage source (inserted between Vin+ and Vin−). If voltage input Vin+ is increased to 0.2 V compared with Vin-, it means that PMOS transistor drain current is reduced and NMOS transistor drain current M5 is increased. From Kirchoff's current law, offset current is increased, thus, the slope of current input versus input voltage which flow through voltage source should be positive which means active positive resistor.

The input terminal voltage can also be decreased by 0.1 V per step from −0.1 to −0.9 V, which is the minimum supply voltage.

Fig. 7 shows the graphs of total harmonic distortion (THD), for different input amplitudes and different input frequencies. All THD curves show the same trend. When the input amplitude is increased from 1 μV to 100 μV, the THD decreases from less than 1% to less than 0.1%. When the input amplitude is increased from 100 μV to 10 mV, the THD increases from less than 0.1% to less than 10%.

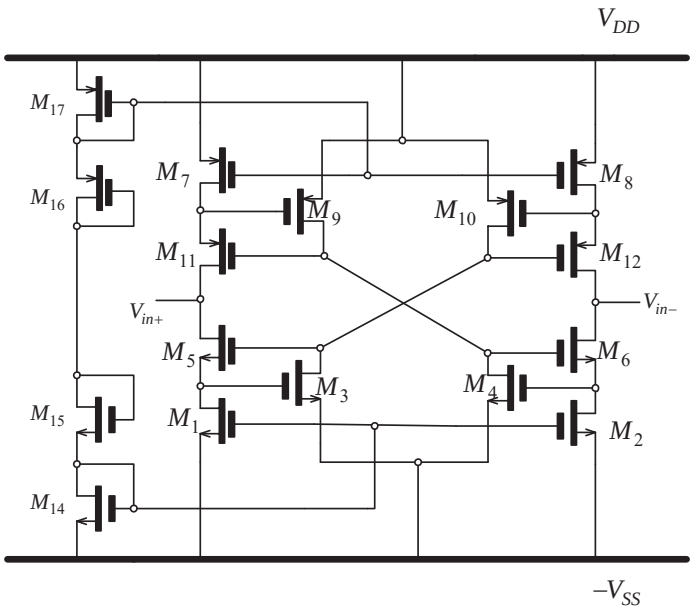

Fig. 3 CMOS floating active resistor based on a complementary common gate without a current source

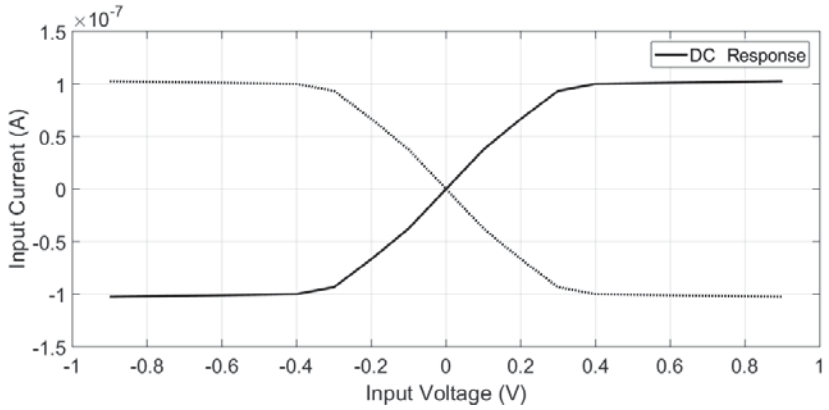

Fig. 4 Current–voltage curves of the CMOS floating active resistor with NMOS aspect ratio = 1 μm/0.18 μm and PMOS aspect ratio = 4 μm/0.18 μm

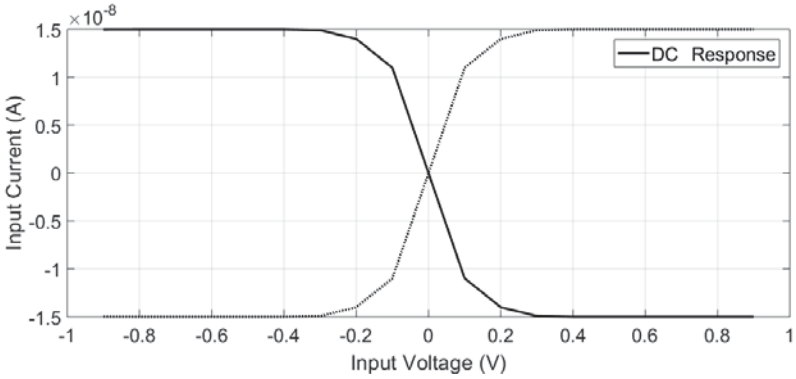

Fig. 5 Current–voltage curves of the CMOS floating active resistor with NMOS aspect ratio = 1 μm/1 μm and PMOS aspect ratio = 4 μm/1 μm.

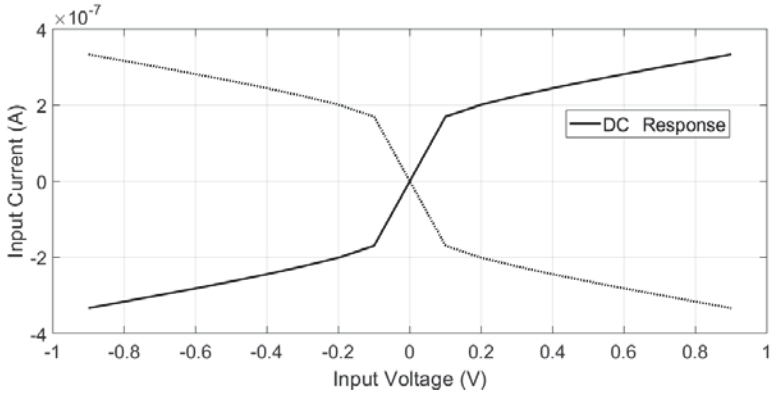

Fig. 6 Current–voltage curves of the CMOS floating active resistor with NMOS aspect ratio = 12 μm/0.18 μm and PMOS aspect ratio = 50 μm/0.18 μm

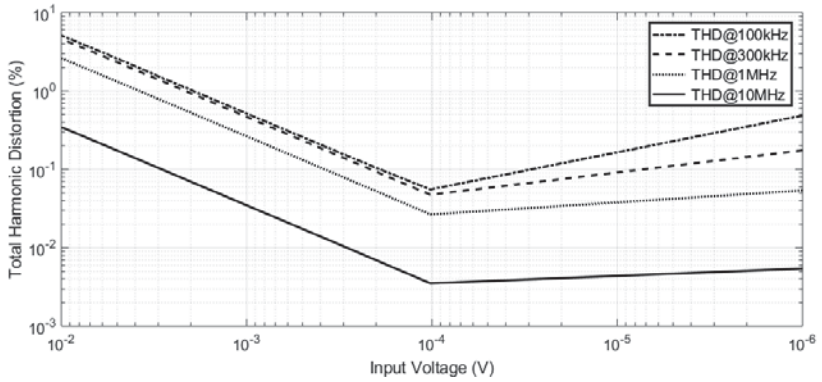

Fig. 7 Total harmonic distortion versus input amplitude for various input frequencies

Fig. 8 presents the THDs for an NMOS aspect ratio of 1 μm/0.18 μm and a PMOS aspect ratio of 4 μm/0.18 μm at various input frequencies. For input amplitudes from 1 μV to 10 mV, the THDs remain constant at different values for different input frequencies. For an input frequency of 100 kHz, the THD remains constant at 30.5%. For an input frequency of 300 kHz, the THD remains constant at 25%. For an input frequency of 1 MHz, the THD remains constant at 22.5%. Finally, for an input frequency of 10 MHz, the THD remains constant at 22.1%.

Fig. 9 presents the THDs for an NMOS aspect ratio of 12 μm/0.18 μm and a PMOS aspect ratio of 50 μm/0.18 μm at various input frequencies. The highest THD for all curves is at 300 kHz; the THD increases from 0% to 2% at an input amplitude 6 mV and reaches 3.3% at an input amplitude of 10 mV. The lowest THD for all curves is at 10 MHz; it increases from 0% to 1.1% at 6 mV.

The current consumption of a version of the circuit in Fig. 4 (given in Table I) is −436 nA. The current consumption of another version of the circuit in Fig. 4 (given in Table II) is −2.172 μA. The current consumption of a third version of the circuit in Fig. 4 (given in Table III) is −25.87 μA.

The active negative resistor can be understood by considering that drain current of transistor M5 in Fig.3 is decreased and drain current of transistor M11 in Fig.3 is increased while voltage drop of drain to source voltage is decreased 0.1 V for M5 and voltage drop of source to drain

voltage is increased 0.1 V for M11, the offset current should flow out of the node through positive terminal of voltage source which is used in simulating the circuit. If the Vin+ terminal is decreased 0.2 V for M5 and source to drain voltage is increased 0.2 V for M11, the offset current should flow out of the node through positive terminal of voltage source more than the first case which is decreased voltage drop of M5 only 0.1V. Thus, it should be negative slope for this case because the more negative input voltage, the more positive offset current.

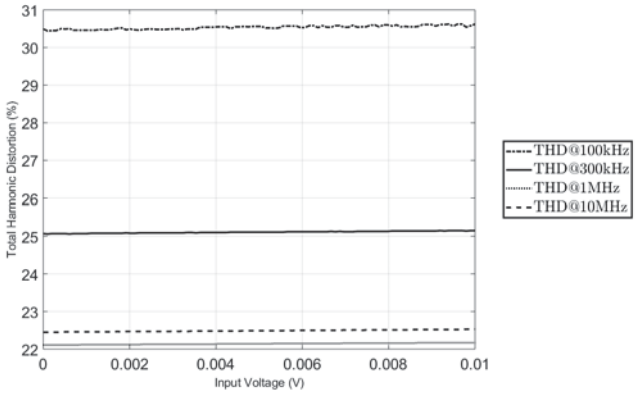

Fig. 8 THD versus input amplitude for various input frequencies

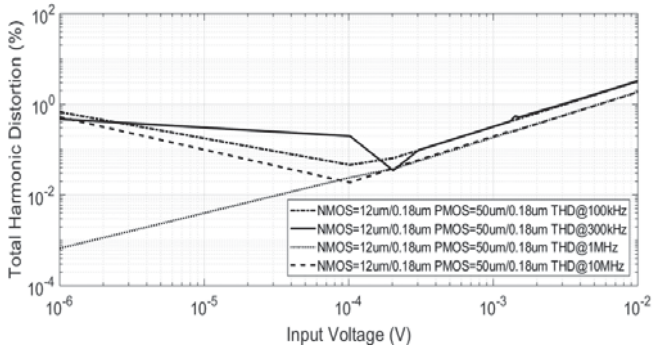

Fig. 9 THD versus input amplitude for various input frequencies

TABLE I
ASPECT RATIOS OF THE TRANSISTORS IN FIG. 4, VERSION 1

Aspect Ratio		Aspect Ratio	
$\left(\frac{W}{L}\right)_1=\left(\frac{W}{L}\right)_2$	$\left(\frac{1\mu m}{1\mu m}\right)$	$\left(\frac{W}{L}\right)_7=\left(\frac{W}{L}\right)_8$	$\left(\frac{4\mu m}{1\mu m}\right)$
$\left(\frac{W}{L}\right)_3=\left(\frac{W}{L}\right)_4$	$\left(\frac{1\mu m}{1\mu m}\right)$	$\left(\frac{W}{L}\right)_9=\left(\frac{W}{L}\right)_{10}$	$\left(\frac{4\mu m}{1\mu m}\right)$
$\left(\frac{W}{L}\right)_5=\left(\frac{W}{L}\right)_6$	$\left(\frac{1\mu m}{1\mu m}\right)$	$\left(\frac{W}{L}\right)_{11}=\left(\frac{W}{L}\right)_{12}$	$\left(\frac{4\mu m}{1\mu m}\right)$
$\left(\frac{W}{L}\right)_{14}=\left(\frac{W}{L}\right)_{15}$	$\left(\frac{1\mu m}{1\mu m}\right)$	$\left(\frac{W}{L}\right)_{16}=\left(\frac{W}{L}\right)_{17}$	$\left(\frac{4\mu m}{1\mu m}\right)$

Fig. 10 shows the *I–V* curves at different temperatures. For the aspect ratios in Table I, the slopes of the *I–V* curve at −20, –10, and 0 °C are −31.94, −19.60, and −14.93 MΩ, respectively.

TABLE II
ASPECT RATIOS OF THE TRANSISTORS IN FIG. 4, VERSION 2

Aspect Ratio		Aspect Ratio	
$\left(\frac{W}{L}\right)_1=\left(\frac{W}{L}\right)_2$	$\left(\frac{1\mu m}{0.18\mu m}\right)$	$\left(\frac{W}{L}\right)_7=\left(\frac{W}{L}\right)_8$	$\left(\frac{4\mu m}{0.18\mu m}\right)$
$\left(\frac{W}{L}\right)_3=\left(\frac{W}{L}\right)_4$	$\left(\frac{1\mu m}{0.18\mu m}\right)$	$\left(\frac{W}{L}\right)_9=\left(\frac{W}{L}\right)_{10}$	$\left(\frac{4\mu m}{0.18\mu m}\right)$
$\left(\frac{W}{L}\right)_5=\left(\frac{W}{L}\right)_6$	$\left(\frac{1\mu m}{0.18\mu m}\right)$	$\left(\frac{W}{L}\right)_{11}=\left(\frac{W}{L}\right)_{12}$	$\left(\frac{4\mu m}{0.18\mu m}\right)$
$\left(\frac{W}{L}\right)_{14}=\left(\frac{W}{L}\right)_{1.}$	$\left(\frac{1\mu m}{0.18\mu m}\right)$	$\left(\frac{W}{L}\right)_{16}=\left(\frac{W}{L}\right)_{17}$	$\left(\frac{4\mu m}{0.18\mu m}\right)$

TABLE III
ASPECT RATIOS OF THE TRANSISTORS IN FIG. 4, VERSION 3

Aspect Ratio		Aspect Ratio	
$\left(\frac{W}{L}\right)_1=\left(\frac{W}{L}\right)_2$	$\left(\frac{12\mu m}{0.18\mu m}\right)$	$\left(\frac{W}{L}\right)_7=\left(\frac{W}{L}\right)_8$	$\left(\frac{50\mu m}{0.18\mu m}\right)$
$\left(\frac{W}{L}\right)_3=\left(\frac{W}{L}\right)_4$	$\left(\frac{12\mu m}{0.18\mu m}\right)$	$\left(\frac{W}{L}\right)_9=\left(\frac{W}{L}\right)_{10}$	$\left(\frac{50\mu m}{0.18\mu m}\right)$
$\left(\frac{W}{L}\right)_5=\left(\frac{W}{L}\right)_6$	$\left(\frac{12\mu m}{0.18\mu m}\right)$	$\left(\frac{W}{L}\right)_{11}=\left(\frac{W}{L}\right)_{12}$	$\left(\frac{50\mu m}{0.18\mu m}\right)$
$\left(\frac{W}{L}\right)_{14}=\left(\frac{W}{L}\right)_{1.}$	$\left(\frac{12\mu m}{0.18\mu m}\right)$	$\left(\frac{W}{L}\right)_{16}=\left(\frac{W}{L}\right)_{17}$	$\left(\frac{50\mu m}{0.18\mu m}\right)$

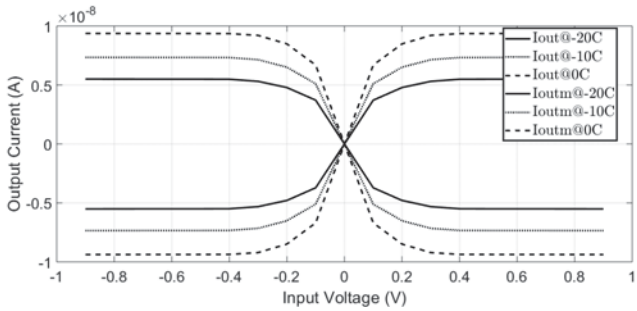

Fig. 10 Current–voltage curves of the CMOS floating active resistor at different temperatures

IV. ACTIVE RESISTORS FOR 2ND ORDER BANDPASS FILTER

Second order Passive filter is implemented by replace passive resistor by active resistor in Fig. 3. The active resistor is useful for implementation at operating frequency above 5 GHz because of little attenuation of magnitude response.

The second order passive filter circuit diagram is described as follows. The resistor is connected between signal source and passive resonance circuit which is a parallel inductor, capacitor and resistor. The design equation is written as follows.

$$\frac{V_{out}}{V_{in}}=\frac{s\left(\frac{1}{R_1L}\right)}{s^2+s\left(\frac{1}{R_1}+\frac{1}{R_2}\right)\left(\frac{1}{L}\right)+\frac{1}{LC}} \quad (5)$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad (6)$$

$$Q = \left(\frac{R_1 R_2}{R_1 + R_2}\right)\sqrt{\frac{L}{C}} \quad (7)$$

The center frequency can be design by equation (6) and quality factor can be design with equation (7). The operating frequency can be maximized by minimized inductor size and minimized capacitor size. Quality factor can be maximized by maximized inductor size and minimized capacitor size. For this design, $L = 1nH, C = 1pF$

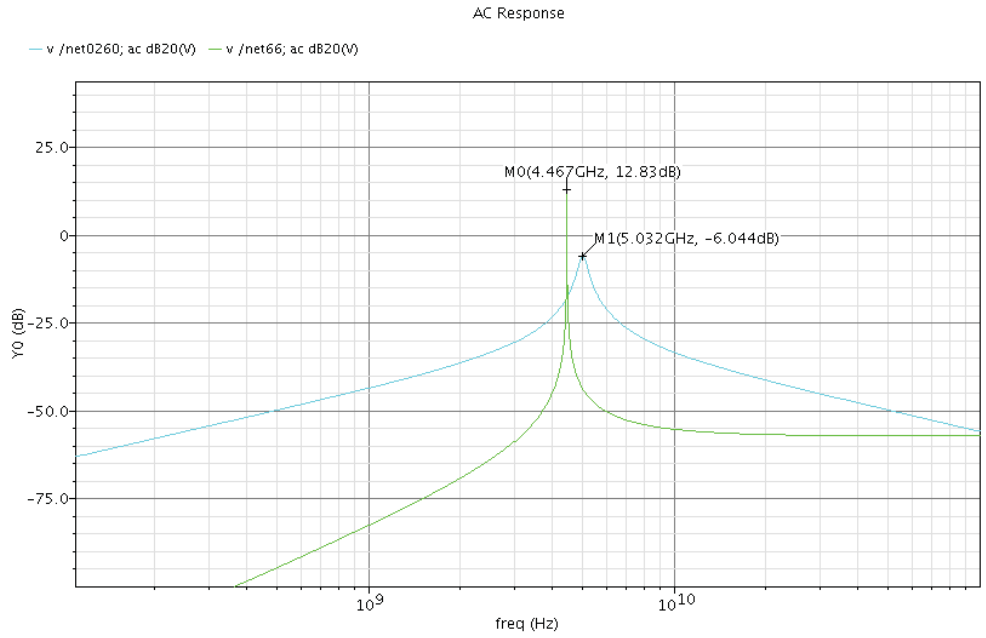

Fig. 11 Passive 2nd order bandpass filter versus Passive 2nd order bandpass filter with CMOS active resistor

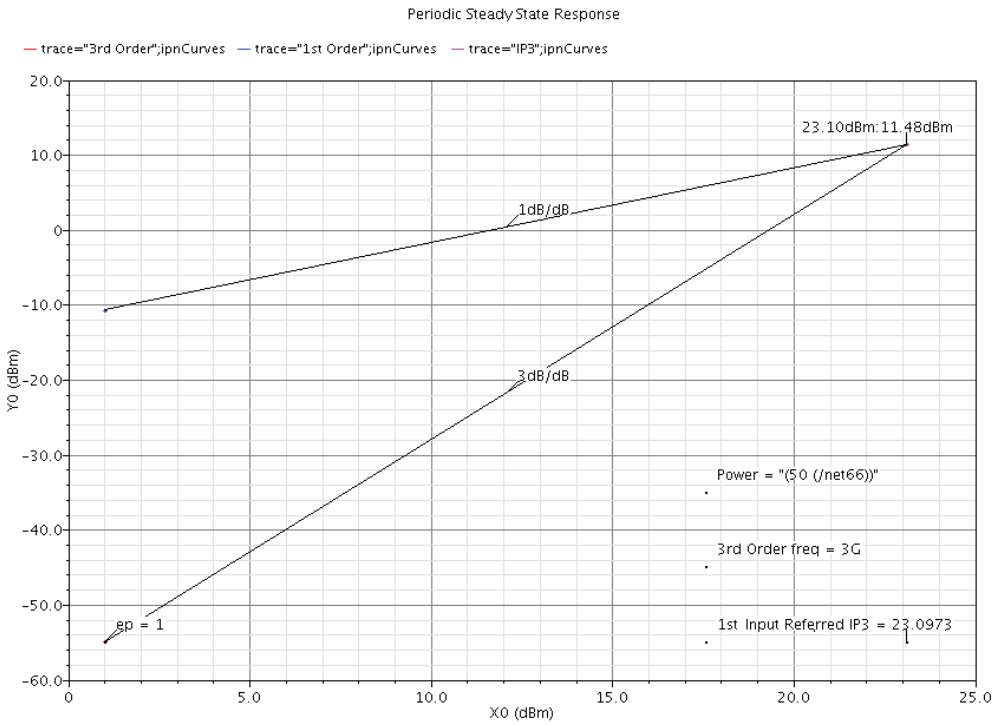

Fig. 12 Input referred third order intercept (IIP3) at input frequency 1 GHz

From Fig. 11, there are some error in operating frequency of 2nd order bandpass filter as a result of miller capacitance of the floating active resistor. From Fig. 12, the input referred third order intercept (IIP3) is computed by Cadence Spectre to have

23.0973 dBm at input frequency 1GHz.

V. Conclusion

Low-voltage low-power floating active resistors were presented in this paper. THDs with three different designed values were plotted with different input amplitudes and different input frequencies. The input voltage and input current of the floating active resistor in Fig. 4 were designed for different temperatures. It could be concluded that, for a higher current consumption, the floating input resistance would be lower, and for a lower temperature, the negative resistance would be larger.

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In 1996, he joined the Department of Electronics and Electrical Engineering, Keio University, as an instructor. He is currently an Associate Professor with the Faculty of Science and Technology, Department of Electronics and Electrical Engineering at Keio University. His research interests include LSI/TCAD, numerical simulation, and modeling. Currently, he is working on the design of on-chip microsystems and biomedical LSIs.