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# Design and Implementation of 4 Bit Multiplier Using Fault Tolerant Hybrid Full Adder

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***Abstract*—**The fault tolerant system plays a crucial role in the critical applications which are being used in the present scenario. A fault may change the functionality of circuits. Aim of this paper is to design multiplier using fault tolerant hybrid full adder. Fault tolerant hybrid full adder is designed to check and repair any fault in the circuit using self-checking circuit and the self-repairing circuit. Further, the use of conventional logic circuits may result in more area, delay as well as power consumption. In order to reduce these parameters of the circuit, GDI (Gate Diffusion Input) techniques with less number of transistors are used compared to conventional full adder circuit. This reduces the area, delay and power consumption. The proposed method solves the major problems occurring in the most crucial and critical applications.

***Keywords*—**Gate diffusion input, hybrid full adder, self-checking, fault tolerant.

## I. Introduction

ADDITION is the most fundamental arithmetic operation performed in many VLSI systems such as microprocessors and application specific Digital Signal Processing (DSP) architecture. All complex arithmetic circuits consist of full adder to execute arithmetic operation such as multiplication, division etc. [1], [2]. These full adders are the nucleus of any system. Many applications contain full adder and it is one of the important parts of circuit.

Faults may lead to failure of the system. So it is necessary to eliminate the fault. A fault may be due to processing, missing materials such as hot carrier effects and metal migration. Faults of this type require the defective part to be replaced. Faults of this type require the defective part to be replaced. The second type of fault is a transient fault where the circuit produces incorrect outputs due to the phenomena such as power supply variation, lightning, α-particles and electromagnetic interference. If the circuit is sequential, the transient fault may cause latch errors which may in turn lead to system failure. A source of transient fault is α-particles present in cosmic rays, which is basis of non-permanent errors in semiconductor circuits [3]. Fault tolerant system is incorporated in applications such as space application, defense surveillance, medical supervisory system and other safety related services. Overall system performance can be effect by the presence of fault in a circuit [4].

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In most of the systems, full adders are encountered in the critical path. The design criteria for full adder are usually multi fold. System complexity depends on transistor count in the ALU. Many fault tolerant full adders were presented in the past. Self-checking full adder can detect the single fault at a time. It is complex and incompatible with its self-checking memory systems. But the usage of conventional full adder in the circuit results in larger delay, area and power consumption [4]. Therefore, in order to overcome this, a fault tolerant full adder is presented. A technique called as GDI is used to optimize the full adder circuit. In addition to the fault detection and fault repair, it can offer a reduced amount of delay and power.

## II. Existing Methods

The GDI based sum cell [5] provides a full adder circuit design with only a less number of transistors when compared with the conventional full adders and hybrid full adder.

The fault-tolerant adder design [4] could check for both the single and double faults that occur in a circuit and also it could repair both faults simultaneously without any error in detection and correction.

Since GDI based full adder has utilized less number of transistors, it occupies lesser area and low delay and power consumption than the conventional full adder [6], [7].

The fault-tolerant adder design has the ability to check the single faults in a circuit and when double faults occur, even though it uses only less number of transistors for the whole circuit design, it cannot repair any of the faults. The fault tolerant hybrid full adder design with GDI techniques is to check single and double error. The proposed method is implemented using fault tolerant hybrid full adder design. They provide better performance than the existing methods.

## III. Proposed Method

The method of fault tolerant full adder uses GDI technique [8] to design the full adder circuit. This is used to design 4 bit multiplier.

### *A. GDI Based Self-Checking Full Adder Design*

Self-checking full adder uses the GDI based sum cell instead of the conventional full adder and existing methods [5], [8], [9].

The output expressions for the sum and carry outputs of the full adder is shown in (1) and (2):

$$\text{Sum}=A\oplus B\oplus Cin \quad (1)$$

Cout=AB+BCin+CinA (2)

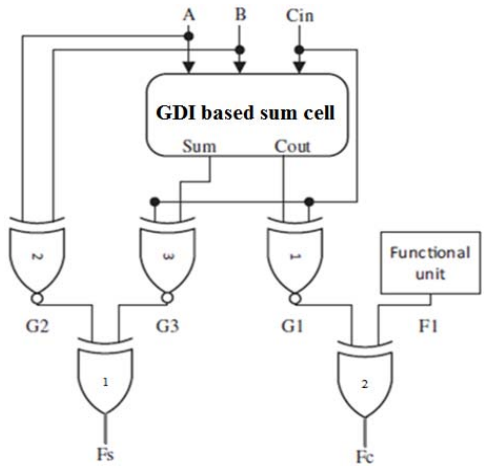


Fig. 1 Proposed self-checking full adder

The proposed method of self-checking full adder as shown in Fig. 1 can detect the faults with the exact indication of its location. In this design, both the sum and carry outputs are checked individually to detect the fault in both the outputs. XNOR gates and equivalent functional unit are used for detecting the fault at the carry output. The output of the functional unit ($A'B'C + ABC'$)and (XNOR-1) are compared using the (XOR-2) to detect the fault. The output expressions of (XNOR-1), functional unit and (XOR-2) are represented in the form of (G1), (F1) and Fc as shown in (3)-(8), respectively.

$$G1 = (\overline{Cout \oplus Cin}) \quad (3)$$

$$F1 = (A'B'C + ABC') \quad (4)$$

$$Fc = (G1 \oplus F1) \quad (5)$$

$$G2 = (\overline{A \oplus B}) \quad (6)$$

$$G3 = (\overline{Sum \oplus Cin}) \quad (7)$$

$$Fs = (G2 \oplus G3) \quad (8)$$

If the output (Fc) indicates 0, it represents the fault free condition. On the other side, if the output of (Fc) indicates 1, it shows that the carry output of the full adder is faulty. Similarly, for detecting the fault in the sum output three XNOR gates are used. The output of the XNOR-2 and XNOR-3 are compared using the XOR-1 to detect the fault. The output expressions of (XNOR-2), (XNOR-3) and (XOR-1) are represented in the form of G2, G3 and Fs and given in (6)-(8), respectively.

If the output (Fs) is 0, it represents the fault free condition. On the other hand, if the output (Fs) is 1, it shows the fault in sum output. In this way the existing design can detect the single and double faults occurred at a time. Finally, the faults, detected at the sum and carry outputs are represented in the form of Fs and Fc, respectively. If any or both of these signals indicate high, it represents the fault in the corresponding outputs. In case of no fault, both the signals indicate low.

### *B. GDI Based Self-Repairing Full Adder Design*

The proposed method of self-repairing full adder is shown in Fig 2 which uses the self-checking full adder with GDI based sum cell.

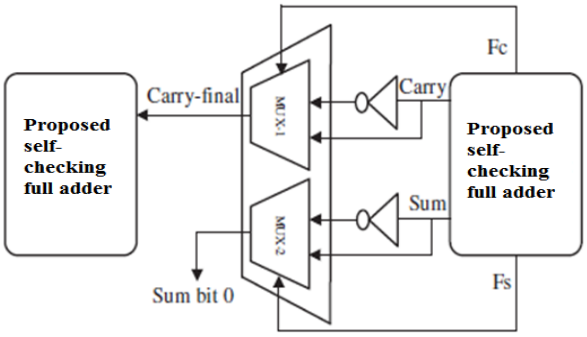


Fig. 2 Proposed self-repairing full adder

The proposed method of self-repairing full adder design is used for repairing the faults detected during the self-checking approach of the hybrid full adder of GDI technique. This design could repair all the faults (transient and permanent) and makes the adder completely fault free.

The approach is based on the following principles:

1. The sum and carry outputs will either 1 or 0 depending on the input combination applied to the GDI based sum cell.
2. If the signal Fs indicates the fault in the sum output then the inverted sum output is selected by the multiplexer under the control of Fs.
3. If the signal Fc indicates the fault in carry output, inverted carry output is selected by the multiplexer under the control of Fc.

Thus the operation of the proposed design is mainly based on the control signals (Fc and Fs) provided by the GDI based self-checking full adder. If the control signal Fs is 0, it shows that there is no fault in the sum output and the sum output coming from the GDI based self-checking full adder will be selected by the multiplexer to generate the final sum. On the other hand, if the control signal Fs is 1, it shows that there is a fault in the sum output. The faulty sum output coming from the GDI based full adder is repaired by using the inverter. The inverted sum output is further selected by the multiplexer to generate the final sum. Similarly, if the control signal Fc is 0, it shows that there is no fault in the carry output, and the carry output coming from the GDI based full adder cell will be selected by the multiplexer to generate the final carry. On the other hand, if the control signal Fc is 1, it shows that the carry output is faulty. The faulty carry output is repaired by using the inverter. The inverted carry output is further selected by using the multiplexer to generate the final carry. In this way, the faulty adder is repaired and converted into a fault free adder. Therefore, this approach can repair single and double faults occurring at the sum and carry outputs at the cost of

minimum hardware resulting in minimum delay and power consumption.

## IV. Results and Discussion

The existing and proposed full adder, multiplier using proposed full adder were designed using Cadence Virtuoso 64 tool of 180 nm technology. The simulation results were obtained. The conventional full adder circuit is designed using Cadence Virtuoso tool and the schematic diagram is given in Fig. 3. The output waveform of the conventional full adder circuit is shown in Fig. 4.

The full adder circuit has been designed using GDI technique and the schematic diagram of the GDI based full adder is shown in Fig. 5. Waveform of GDI based full adder is shown in Fig. 6. Fig. 7 gives the schematic diagram of the self-checking full adder designed using conventional full adder. Fig. 8 gives the output of the self-checking full adder designed using the conventional full adder. In this figure, we could observe that the output of the Fc and Fs are zero since there is no fault in carry and sum respectively.

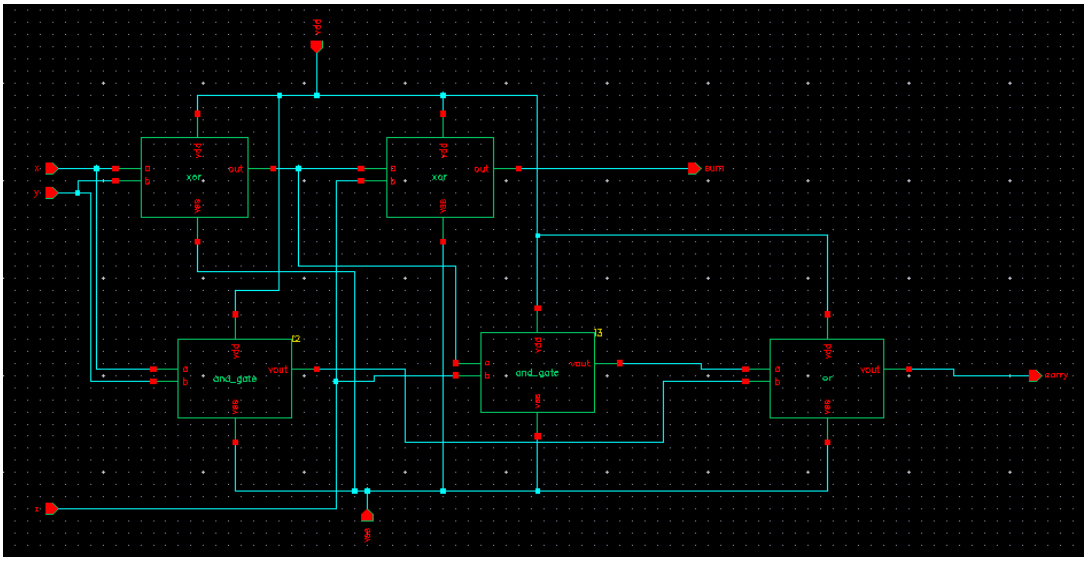


Fig. 3 Schematic diagram of full adder

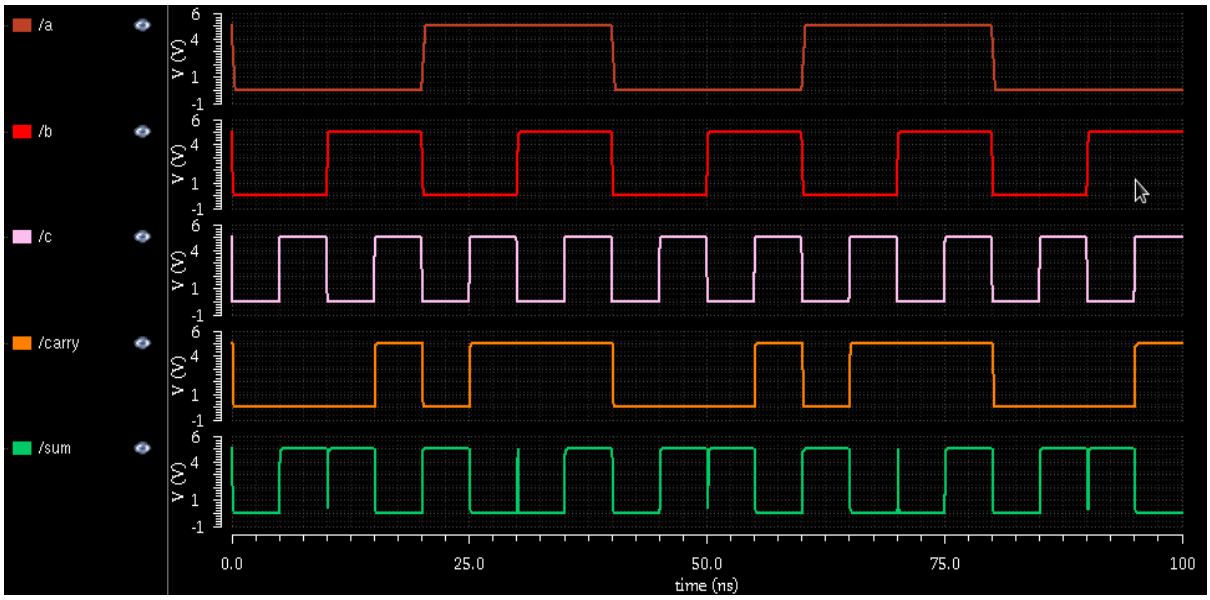


Fig. 4 Waveform of Full adder

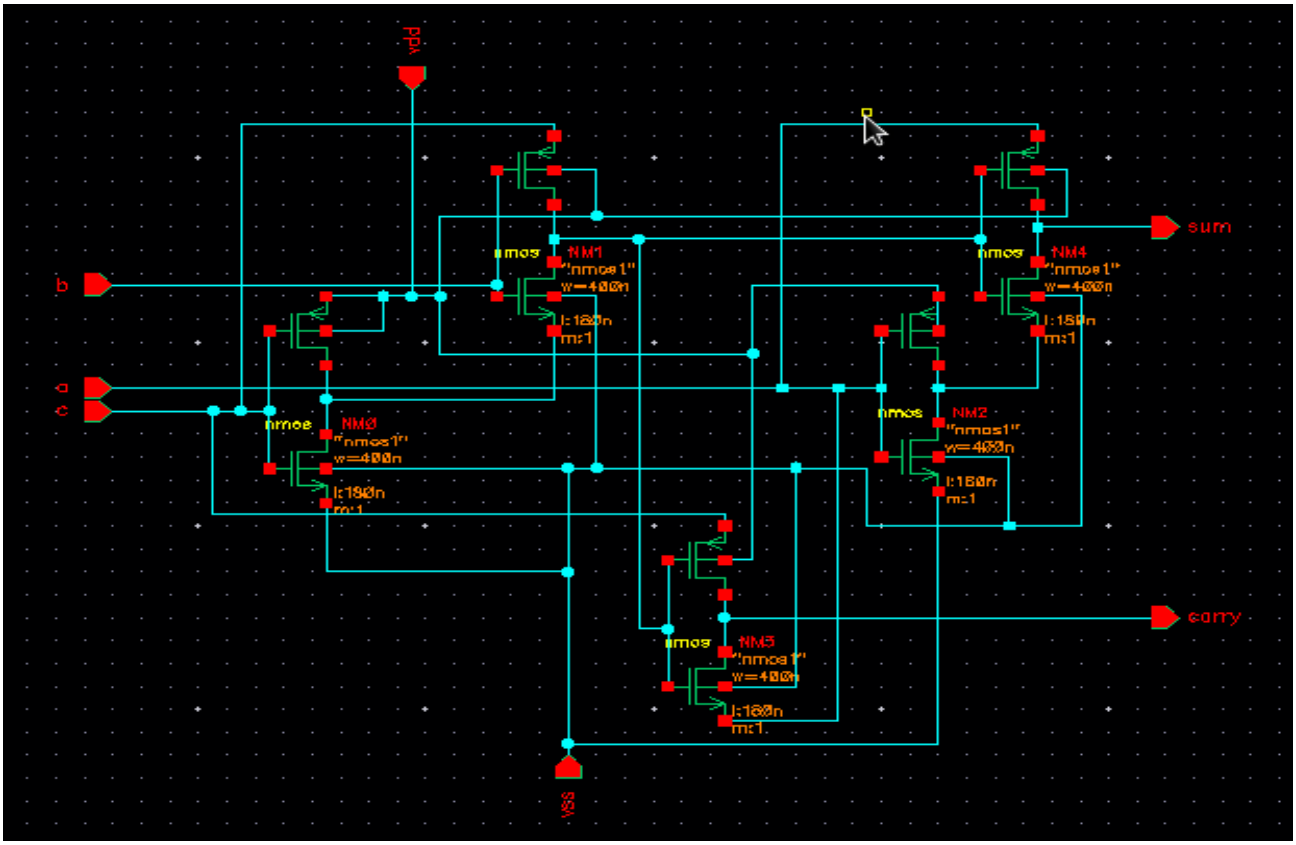


Fig. 5 Schematic diagram of GDI based full adder

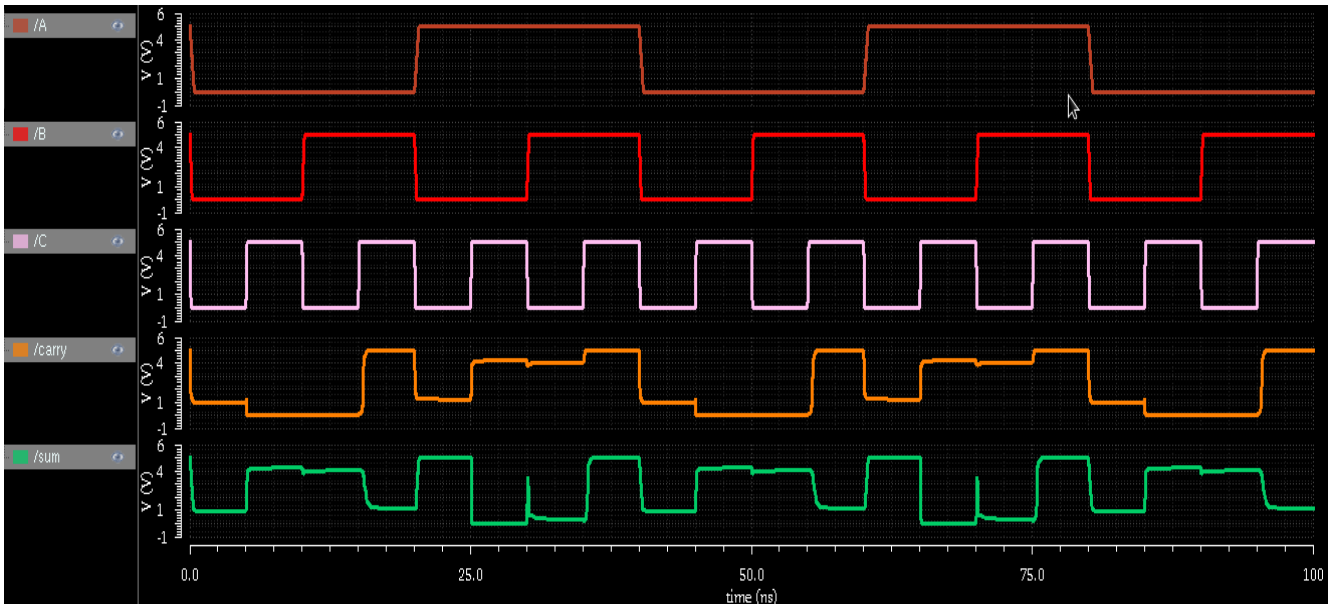


Fig. 6 Waveform of GDI based full adder

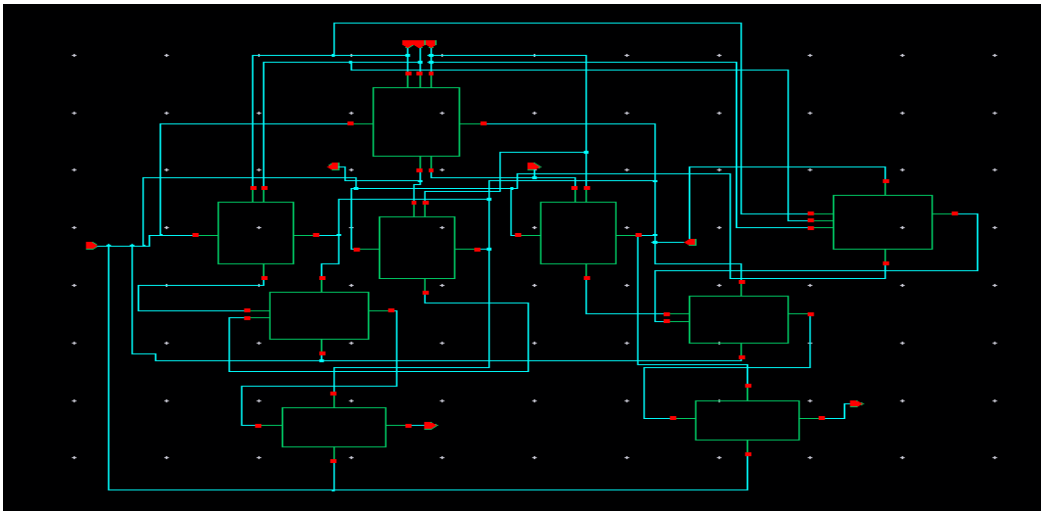

Fig. 7 Schematic diagram of Self-checking full adder

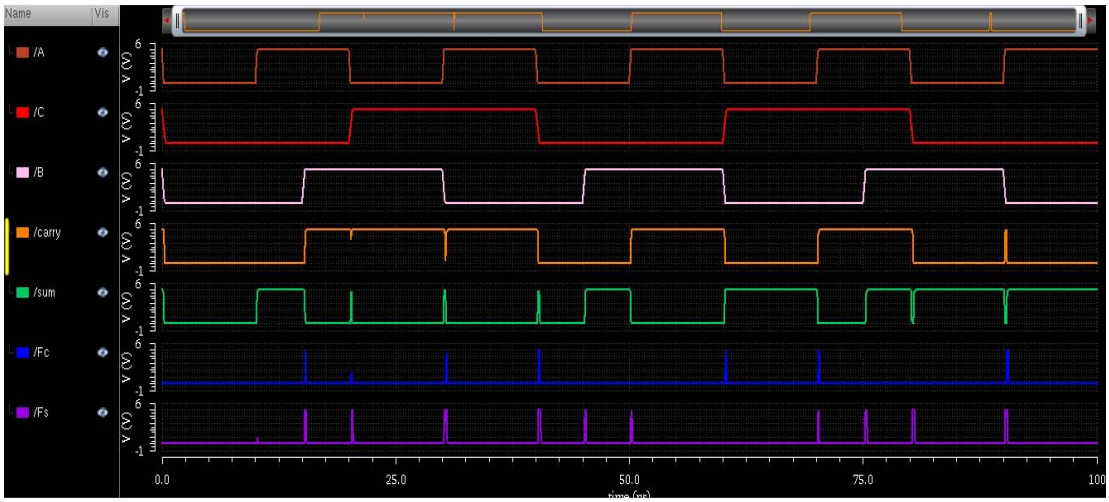


Fig. 8 Output of Self-checking full adder

The schematic diagram and waveform of the self-checking full adder designed using the GDI technique is shown in Figs. 9 and 10 respectively.

The self-repairing full adder is designed using the self-checking full adder and multiplexer and the schematic diagram of this self-repairing full adder is given in Fig. 11. Fig. 12 gives the output of self-repairing full adder. The output fault has been repaired using the self-repairing circuit.

The self-checking full adder designed using the conventional full adder used in the previous self-repairing design is replaced by the self-checking full adder designed using GDI technique. The schematic diagram of this self-repairing full adder is given in Fig. 13.

The output of the self-repairing full adder using GDI is shown in Fig. 14. A multiplier is implemented using the existing method of self-repairing full adder as in [10] which is shown in Fig. 15.

The array multiplier is designed using self-repairing full adder. Fig. 16 gives the schematic diagram of the multiplier designed using the proposed self-repairing full adder.

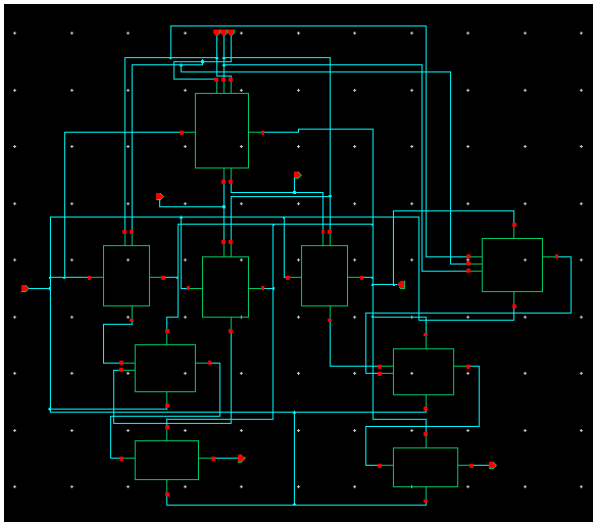

Fig. 9 Schematic diagram of Self-checking full adder using GDI

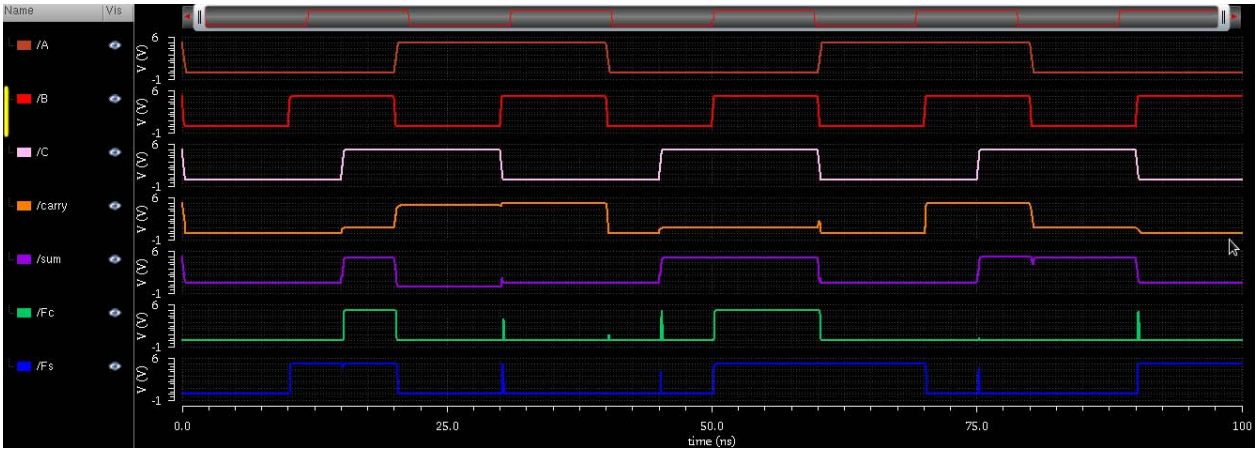


Fig.10 Output of Self-checking full adder using GDI

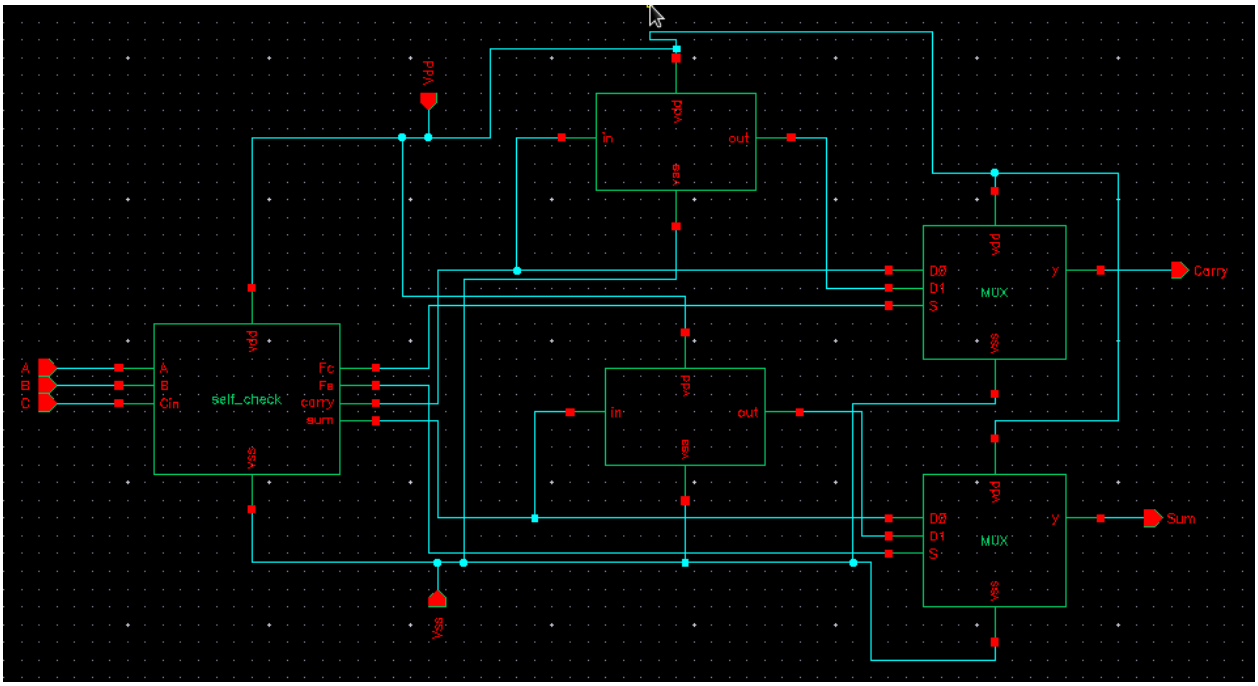


Fig.11 Schematic diagram of Self-repairing full adder

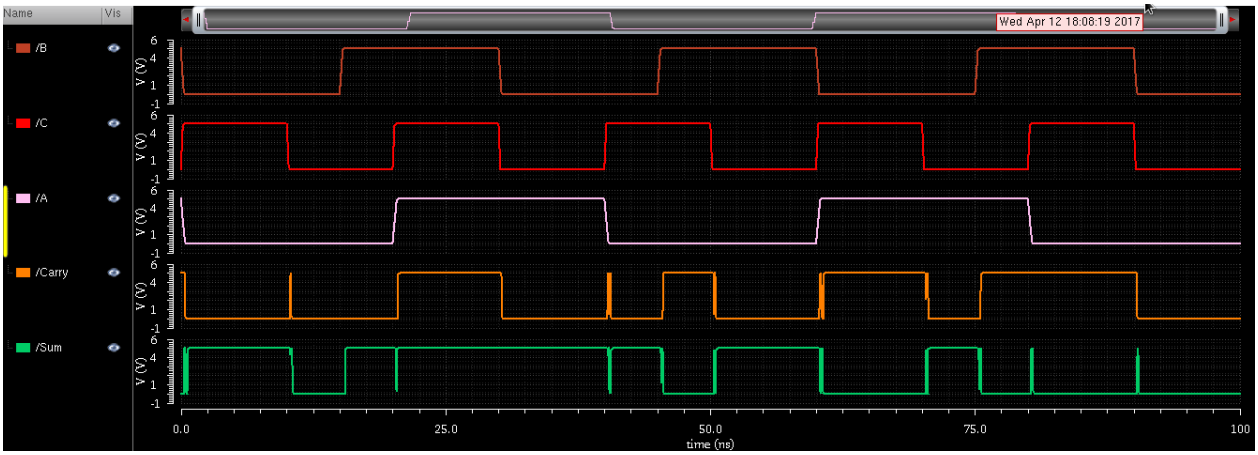


Fig.12 Output of Self-repairing full adder

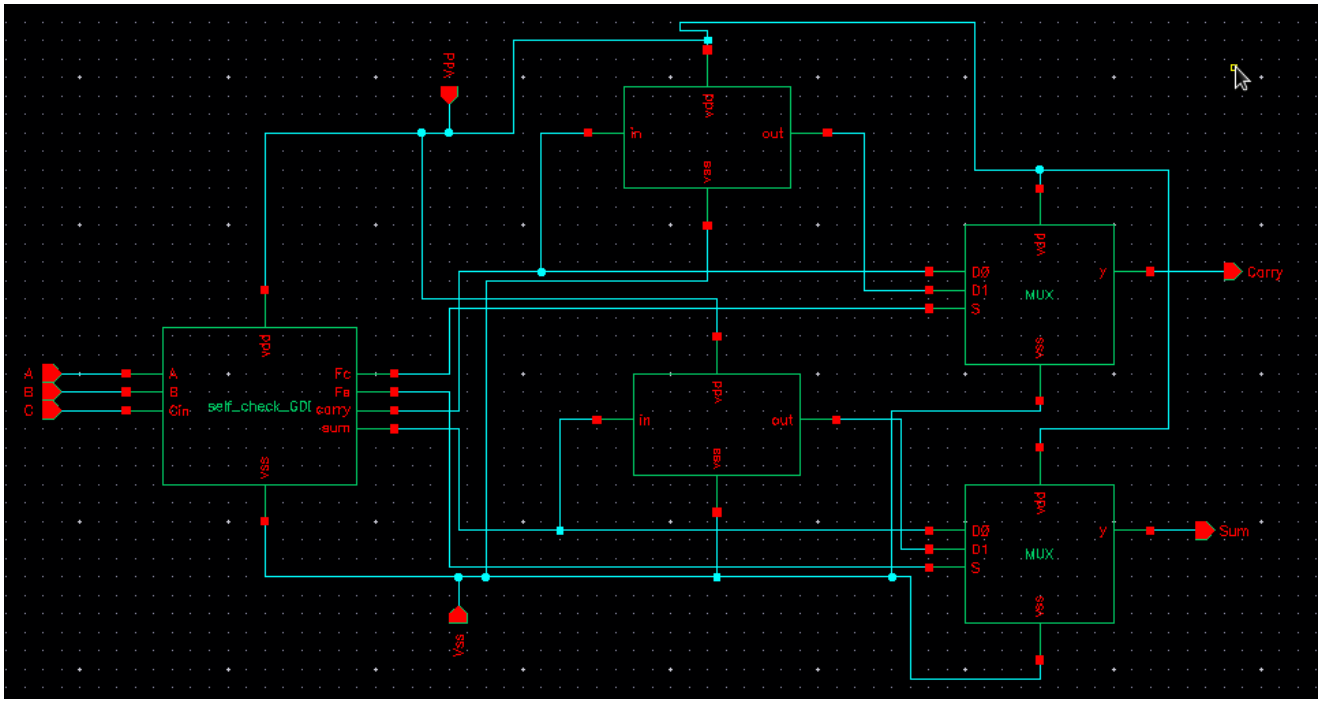


Fig. 13 Schematic diagram of Self-repairing full adder using GDI

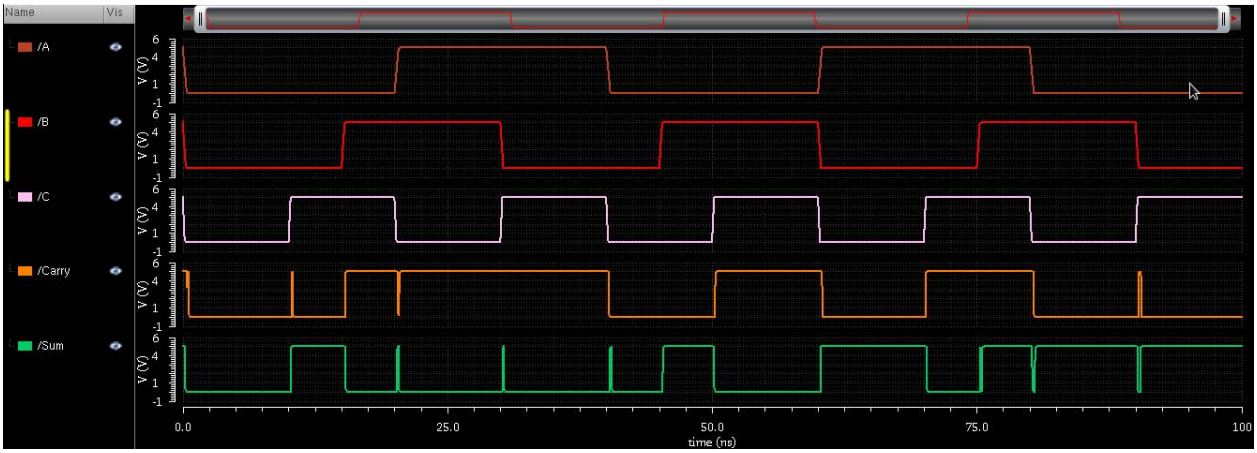


Fig. 14 Self-repairing full adder (GDI) –Output

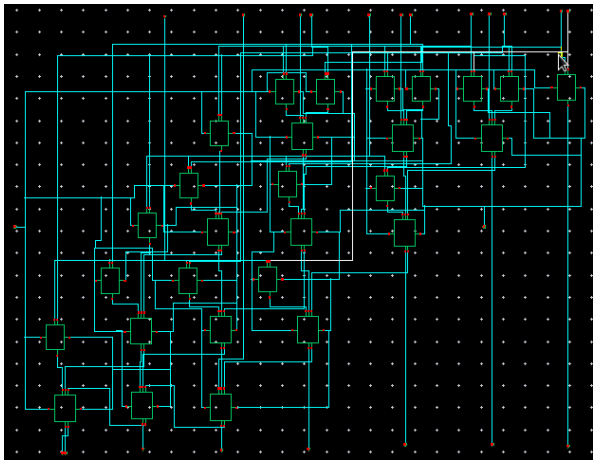

Fig. 15 Schematic diagram of Multiplier

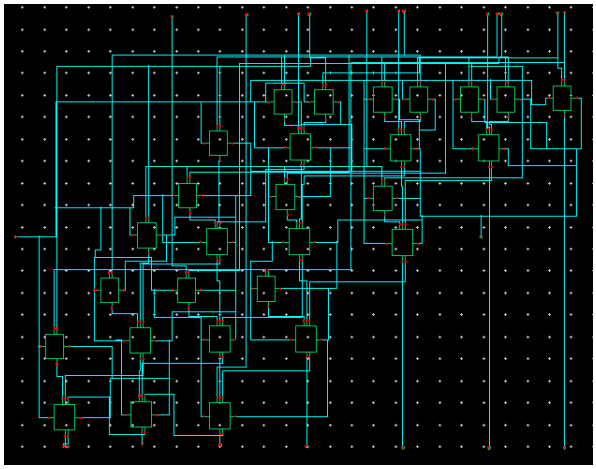

Fig. 16 Schematic diagram of Multiplier with GDI

A detailed comparison on the power, delay and power delay product of all designed circuit are given Table I.

TABLE I
COMPARISON OF POWER, DELAY AND PDP

| Name | Power (mw) | Delay (ps) | Power delay product (pJ) |
|---|---|---|---|
| **Self- check** | 1269.84 | 186.28 | 236.54 |
| **Self-check (GDI)** | 1247.6 | 22.79 | 28.43 |
| **Self-repair** | 1274.9 | 324.9 | 414.22 |
| **Self-repair (GDI)** | 1274.7 | 299.5 | 381.77 |
| **Multiplier** | 972.59 | 327.99 | 318.99 |
| **Multiplier (GDI)** | 659.65 | 311.80 | 205.67 |

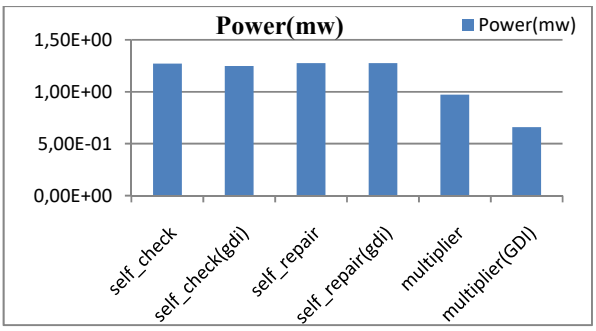


Fig. 17 Comparison chart for power

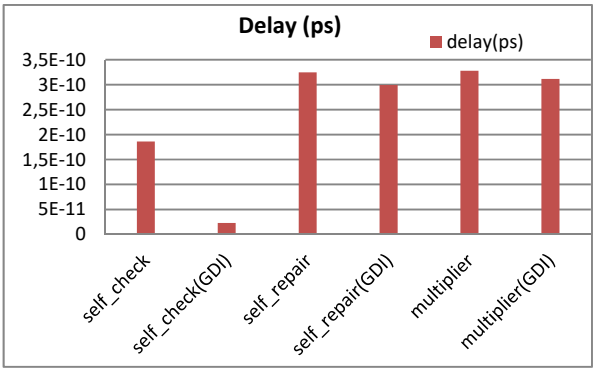


Fig. 18 Comparison chart for delay

From the comparisons made in Tables I, II and Figs. 18, 19 it has been observed that the self-repairing full adder using GDI technique provides less delay and power consumption along with less number of transistors when applied in a multiplier circuit and provides fault-free output.

## V. CONCLUSION

A technique of self-checking and self-repairing full adder using GDI technique has been proposed. The design can detect and repair both single and double faults at a time using less number of transistors providing lesser delay and less power consumption. The comparison results of the designs are found better than the previous existing methods. The design is extendable up to a desirable level. A 4-bit fault tolerant multiplier is also implemented using the design. It works efficiently when cascaded and can handle the faults successfully.

TABLE II
COMPARISON OF NUMBER OF TRANSISTORS USED

| Name | List of logic gates | Transistor count |
|---|---|---|
| **Self-checking full adder** | Full adder-1<br>XNOR-5<br>NOT-2<br>Functional unit-1 | 26<br>60<br>4<br>28<br>Total=118 |
| **Self-checking full adder (GDI)** | Full adder (GDI)-1<br>XNOR-5<br>NOT-2<br>Functional unit-1 | 10<br>60<br>4<br>28<br>Total=102 |
| **Self-repairing full adder** | Self-check adder-1<br>NOT-2<br>MUX-2 | 118<br>4<br>20<br>Total=142 |
| **Self-repairing full adder (GDI)** | Self-check adder (GDI)-1<br>NOT-2<br>MUX-2 | 102<br>4<br>20<br>Total=126 |
| **Multiplier** | Self-repair adder-12<br>AND-16 | 1704<br>96<br>Total=1800 |
| **Multiplier (GDI)** | Self-repair adder (GDI)-12<br>AND-16 | 1512<br>96<br>Total=1608 |

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