World Academy of Science, Engineering and Technology
International Journal of Energy and Power Engineering
Vol:11, No:7, 2017

Field-Programmable Gate Array Based Tester for Protective Relay

H. Bentarzi, A. Zitouni

***Abstract*—**The reliability of the power grid depends on the successful operation of thousands of protective relays. The failure of one relay to operate as intended may lead the entire power grid to blackout. In fact, major power system failures during transient disturbances may be caused by unnecessary protective relay tripping rather than by the failure of a relay to operate. Adequate relay testing provides a first defense against false trips of the relay and hence improves power grid stability and prevents catastrophic bulk power system failures. The goal of this research project is to design and enhance the relay tester using a technology such as Field Programmable Gate Array (FPGA) card NI 7851. A PC based tester framework has been developed using Simulink power system model for generating signals under different conditions (faults or transient disturbances) and LabVIEW for developing the graphical user interface and configuring the FPGA. Besides, the interface system has been developed for outputting and amplifying the signals without distortion. These signals should be like the generated ones by the real power system and large enough for testing the relay's functionality. The signals generated that have been displayed on the scope are satisfactory. Furthermore, the proposed testing system can be used for improving the performance of protective relay.

***Keywords*—**Amplifier class D, FPGA, protective relay, tester.

I. Introduction

THE reliability of the power system depends upon the performance of the thousands of relays that may be used in protective and control system. The failure of a relay to operate as intended may jeopardize the stability of the entire system and its bulk elements. In fact, major failures during a disturbance are more likely due to unplanned relay operation rather than by the failure of a relay to trip. Reliability consists of two aspects: dependability and security. Dependability is known as the degree of assurance that a relay will operate correctly as planned. Security is the degree of assurance that a relaying system will operate unnecessarily during any transient abnormal conditions [1].

Appropriate relay testing provides first guard against relay false-tripping. Relay testing can aid to confirm the design of relay, compare the performance of different relays, verify relay settings, classify system conditions that might cause unplanned relay operation, and carry out post-event analysis to understand the causes of unintentional or incorrect relay actions. Relay tester enhancements need to continue because of the use of relays in smart power grids where the conditions are not the same as in the conventional one. This leads to new relay technologies [2].

Disturbances include transient distortion in the voltage due to post-fault, potential transformer saturation or compensator switching may affect transmission line relays and relaying systems in various ways. The mal-operation of this relay is generally unnecessary tripping during post-fault or compensator connection which produces DC offset and harmonics. This may reduce the security of protection system and hence its reliability.

This work focuses mainly on the design and the implementation of the Class D amplifier which is the amplification part of the testing system. The Class D amplifier has been used in this work to amplify the simulated disturbances that are generated by Simulink power system model to be then injected to the protective relay and monitor its response. LabVIEW has been used for developing the graphical user interface and controlling NI 7851Board.

In this research work, we have used a technology that allow designing an enhanced relay testing system which in turn can be used for improving the performance of protective relay. In order to test both security and dependability and hence the reliability, this work proposes a new frame work of tester based on FPGA associated with acquisition card NI.

II. Testability

Protection system reliability and testability require the design of the protection system for high functional reliability and in-service testability commensurate with the safety function to be performed. They also require a design that permits on-line periodic testing of the functioning of the protective system.

The testing of protection schemes faces many problems since the main function of protection equipment is taken into consideration under operation during system fault conditions, and it cannot readily be tested under normal conditions [3]. This situation is aggravated by increasing the complexity of protection schemes and use of relays containing software.

Type tests may be needed to confirm that a relay satisfies the standard specifications and fulfills all appropriate standards. Since the essential task of the protective relay is to operate correctly under abnormal conditions. It is necessary to evaluate the performance of the relay under such conditions. Therefore, inclusive type tests simulating the operational conditions are investigated during the manufacturer's works while the development and certification of the apparatus [4].

Different tests that can be carried out by the developed testing system are as follows [4]:

H. Bentarzi and A. Zitouni are with the Research Laboratory of Signal and Systems, Institute of Electrical Engineering and Electronics, UMBB University, Boumerdes, Algeria (phone: +213 772288608; fax: +213 24818333; e-mail: lss@univ-boumerdes.dz).

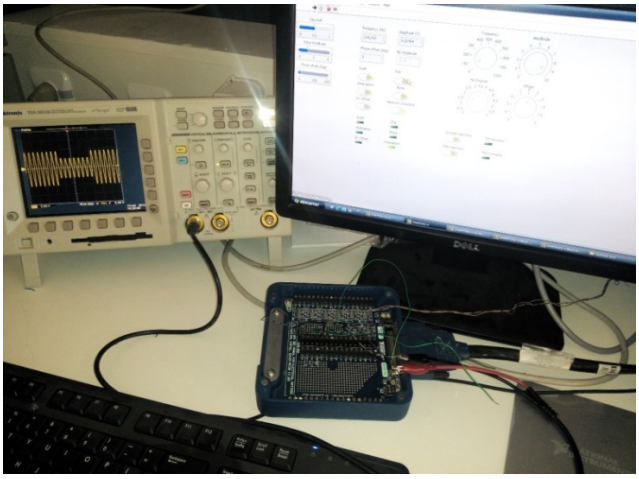

Fig. 1 FPGA based tester

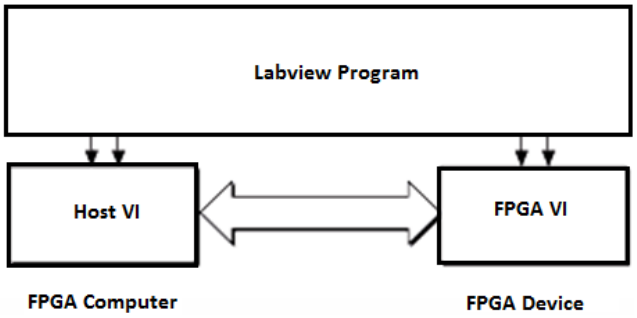

Fig. 2 Using a Host VI to Communicate with the FPGA Target

A. Steady State Test [4]

Usually steady state test is used for the examination of the relay setting by injecting current and voltage at predetermined values for time longer than the setting time of relay. Then, the signal is varied slowly at a rate much smaller than resolution of relay, by manually turning a knob or by an automatic system [4]. This type is of less use in commissioning because the signal does not represent the real power system signal during faults or abnormal condition.

B. Dynamic State Test

Dynamic state test is inspected by simultaneously applying fundamental frequency components of voltage and current which represent power system states of pre-fault, fault and post-fault [4]. Time for relay operation is measured. This type of test can be used in commissioning and troubleshooting.

C. Transient Test

Transient testing may be performed by injecting at the same time both fundamental and non-fundamental frequency components of voltage and current which represent real power system conditions. This type of test may be used for testing a security of the protective relay. The signal that may be used in this type for testing may be obtained from digital fault recorders (DFR) real-time Simulator using MATLAB/ Simulink [5].

The increasing use of digital and numerical technology in instruments such as protection, measurement, and control equipment in power networks has formed the possibility for collecting large numbers of digital data of power system transient events. In addition to these instruments, real-time simulators may be used to generate these digital data. The users of these data are faced the problem of how to convert it to real-time signal by amplifying it without distortion as the signals outputted from instrument transformers [5].

III. Tester Implementation

FPGA based tester has been implemented using the acquisition card NI as shown in Fig. 1. It consists of three main parts which are computer, NI 7851 board, and amplifier.

A. Software Part

Application development for relays tester has been investigated using Simulink and LabVIEW as development tools and driver ofNI7851 board [6].

The NI LabVIEW FPGA module allows the user to graphically implement digital circuits within an FPGA chip using LabVIEW to create VIs and functions that control the I/O, timing, and logic of the device, PCIe 7851, in our case, to generate the desired output [7].Interactive Front Panel Communication has been used to communicate directly with the FPGA board using a FPGA VI, but the communication is limited to the number of functions and operations that can be performed and lacks real times updating as shown in Fig. 2. So, a separate HOST VI, which is running simultaneously with the FPGA VI, has been used to interact with it in real time and provides the user with more control over the inputs of the FPGA. Host VIs are used to share information between the host computer and the FPGA target for the following reasons:

- processing more data than one can fit on the FPGA,
- performing operations not available on the FPGA target,
- controlling the timing and sequencing of data transfer.

The Host VI takes advantage of a number of LabVIEW's inbuilt functions and relies on the FPGA interface functions such as Close/Open FPGA VI Reference to establish a connection/ disconnection between the FPGA VI and the Host VI. Read/Write Control block may be used to read a value from or write a value to a control or indicator in the FPGAVI. Figs. 3 and 4 show the Front Panel and the Block Diagram Host VI.

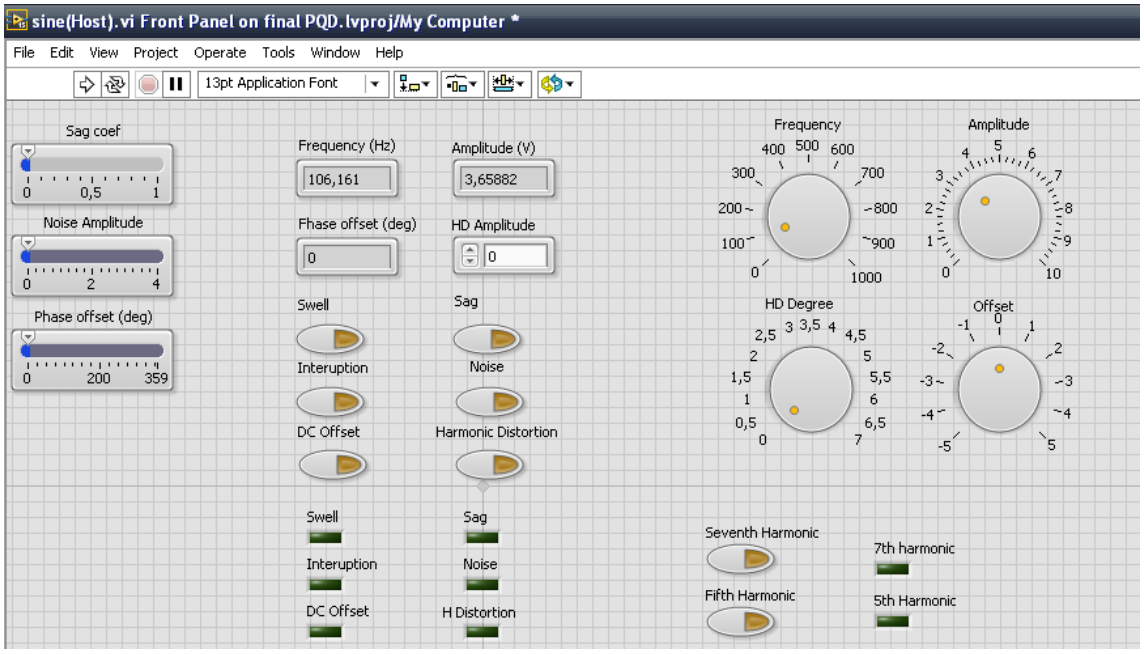

Fig. 3 Host VI Front Panel of Tester

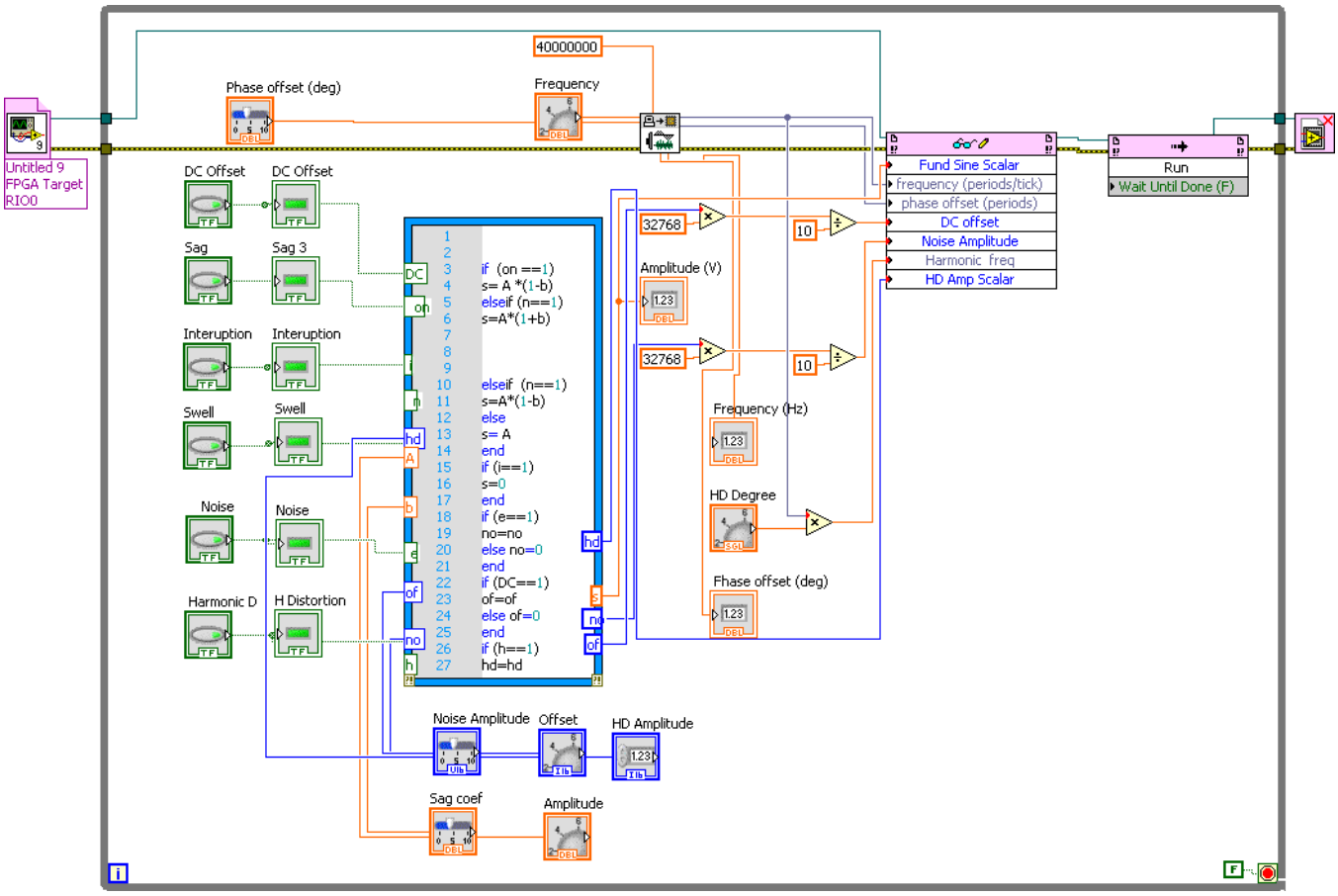

Fig. 4 Host VI Block Diagram of tester.

Fig. 5 Block diagram of class D amplifier

B. Hardware Part

PC outputs the signals generated by simulator via the card NI7851, where the DAC converts the data to analog form, and then to the relay under test using the amplifier [5].

Fig. 5 shows a block diagram of the (class D) amplifier [7]. First, the signal that will be injected to the amplifier has been sampled by the 24-bit analogue-to-digital converter with Bandwidth (0-5 kHz). The produced signal is an input to a digital filter which drives a digital PWM. The power circuit, which can be a half-bridge converter, is followed by a low pass filter to recover the original analog signal [8].

C. Amplifier Development

The final circuit design of this class D amplifier is shown in Fig. 6. The first stage of this class D amplifier is controlled by circuit where the PWM signal generator is fed to the two gate drives. The main role of these gate drives is to create dead-time for avoiding shoot-through current that can damage the output stage. Then, the power stage which consists of H-Bridge and low pass filter is the final stage.

The PCB implementation circuit of the Class D amplifier is shown in Fig. 6.

This circuit first was implemented on proto board in order to test it. After that, it will be implemented on the PCB. The control circuit should be well isolated from the power circuit.

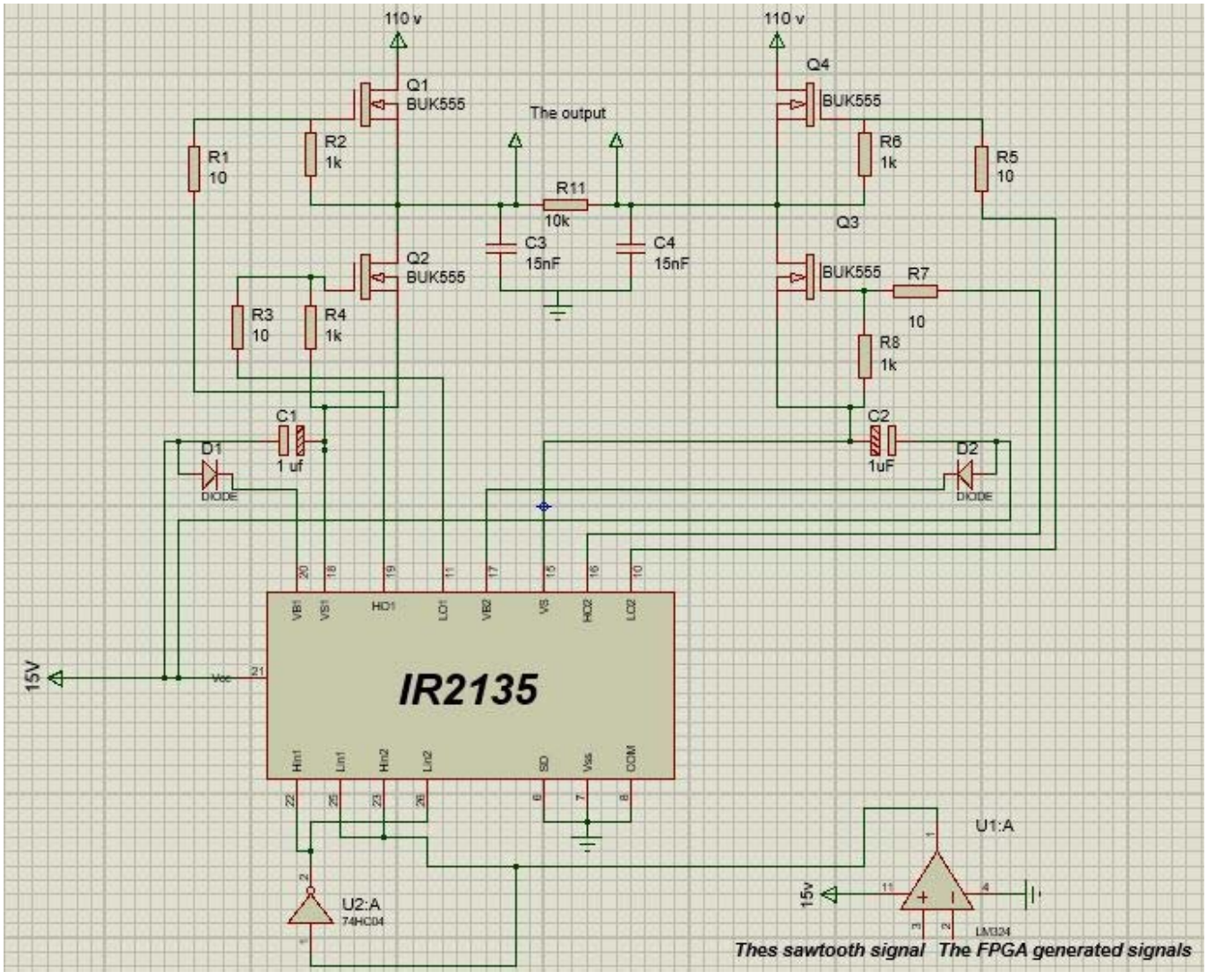

Fig. 6 Class D Amplifier circuit

IV. Performance Evaluation of the Tester

The signal of the PWM is supplied to H-bridge. The output PWM signal of the H-bridge before the using the low passive filter is shown in Fig. 8 where the H-bridge is fed with 12 V.

The output signal of the H-Bridge fed with 18.73 V and a load of 100 Ω are shown in Figs. 9 and 10, and the input signal is a sine wave of 10 V peek to peek and frequency of 50 Hz. This signal has been taken and injected to the Class D amplifier, but the voltage of the H-bridge has been changed to 38.8 V, and the probes were changed to X10 to decrease the scale of the oscilloscope so that each division is 20 V. The amplified output signal voltage is 110 V peak to peak with a frequency of 50 Hz, and its efficiency is approximately 100%. However, in Fig. 11, some distortions are appearing in the output amplified signal, and these distortions are not due to the class D amplifier, but they are part of the disturbance input signal.

The theoretical efficiency of a class D amplifier is 100%, but this is unachievable in practice. However, this efficiency can approach significantly this value by making a good design to minimize switching losses that lead to high power loss.

The formula to calculate the efficiency is:

$$\eta = \frac{P_{OUT}}{P_{in}} * 100$$

The efficiency and the gain are calculated with respect to a sine wave input of 10 V, and the voltage of the source that feed the H-bridge has efficiency is $\eta = 92.4\%$.

The total harmonic distortion (THD) is a very important parameter to evaluate the performance of the Class D amplifier to have a clear signal, and we do not have the proper means to do the calculation to have the exact value, but it appears that the THD is less than 1%.

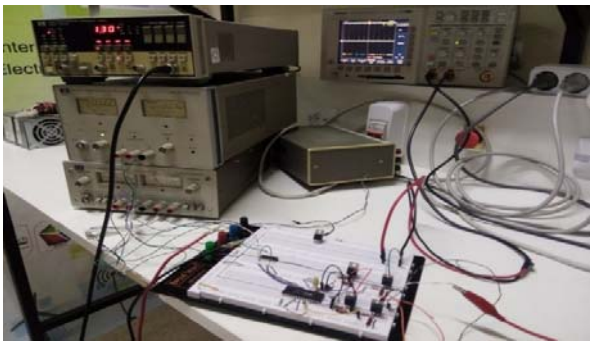

Fig. 7 Class D amplifier circuit

V. Conclusion

The FPGA based tester has been successfully designed and implemented. Simulator is used to generate three-phase voltages and currents presented the actual power grid events mainly the fault and other abnormal conditions to check the relay settings. In fact, a PC has been used to generate these events signals and inject them to the relay under test via the acquisition card NI7851.

User Interface (GUI) has been developed to include some parameters of the relay, to control the generated data of waveform signals, and to display the generated signals.

The Class D amplifier has been selected in this circuit to amplify the simulated disturbances signals. Design and implementation of the Class D amplifier which is the amplification part of the testing system have been investigated in this work.

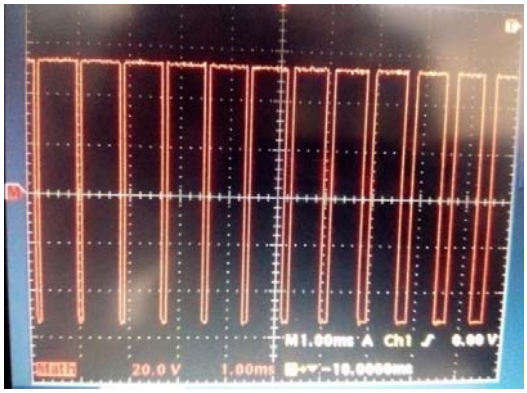

Fig. 8 H-bridge output PWM signal

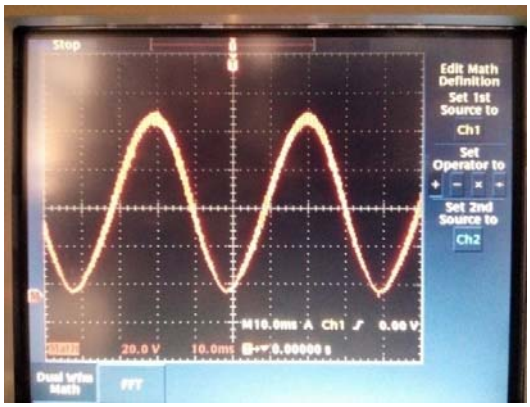

Fig. 9 Output signal of class D amplifier

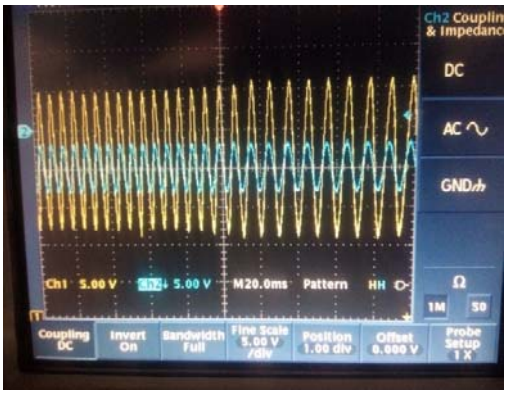

Fig. 10 Amplified sine wave using Class D amplifier

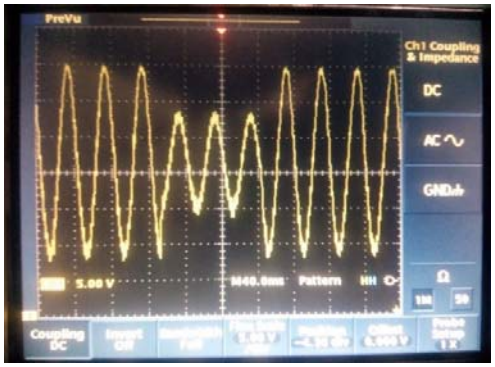

Fig. 11 Voltage sag generated from Disturbances generator

The test results and performance of this tester are very satisfying. This is clearly proven by its high efficiency and very low THD. The Class D amplifier that has been used can amplify any disturbance signal with the same performance results even if the frequency of these disturbances is changing. This ability is possible because the cut-off frequency of its filter can attain 1.1 kHz.

REFERENCES

[1] A. kG. Phadke, T. Hlibka, M. Ibrahim, "A digital computer system for EHV Substation: Analysis and Field Tests", *IEEE Trans. Power Apparatus and System*, Vol. PAS-95, 1976, pp. 291-301.

[2] K.C.A. Dierks, *Relay Specific Computer Aided Testing for Protective Relays*, Eskom, Republic of South Africa 2006.

[3] Relay testing and commissioning (Online). Available: http://www.fecime.org/referencias/npag/chap21-370-397.pdf (Retrieved on 17/12/2016).

[4] M. Chafai, H. Bentarzi, A. Ouadi, A. Zitouni and A. Recioui, "PC based Testing System for Protective Relay", *in Proc. 4th International Conference on Power Engineering, Energy and Electrical Drives*, Istanbul, Turkey, 13-17 May 2013.

[5] A. Ouadi, H. Bentarzi, M. Chafai and A. Zitouni, "Microcontroller Based Protective Relay Testing System," in *Proc. The 10th WSEAS International Conference on Circuits, Systems, Electronics, Control & Signal Processing (CSECS '11), Montreux University*, Switzerland, December, 29-31, 2011.

[6] National Instruments, *NI R Series Multifunction RIO User Manual*, 2009.

[7] M. Chafai, H. Bentarzi, and A. Ouadi, "A New Frame Work for Protective Relay Tester "*NNGT Journal: International Journal of Signal Processing and Imaging Engineering*, Vol. 1, pp.60 -65, (2014).

[8] Texas Instruments, *LMx24-N, LM2902-N Low-Power, Quad-Operational Amplifiers*, 2015.

H. Bentarzi (M'17) received his Ingeniorat and Magister degrees from Institut National d'Electricité et Electronique (INELEC), Boumerdes, in 1989 and 1992 respectively. Both are in applied Electronics. However, he achieved his PhD degree at the Ecole Nationale Polytechnique, Algiers, in Micro-Electronic, in 2004.

His current research interests include power systems protection and wide area measurement systems improvement using the recent developed technologies of communication. He has been author and co-author in more than hundred technical papers.