A Physically-Based Analytical Model for Reduced Surface Field Laterally Double Diffused MOSFETs

M. Abouelatta, A. Shaker, M. El-Banna, G. T. Sayah, C. Gontrand, A. Zekry

Abstract**—**In this paper, a methodology for physically modeling the intrinsic MOS part and the drift region of the n-channel Laterally Double-diffused MOSFET (LDMOS) is presented. The basic physical effects like velocity saturation, mobility reduction, and nonuniform impurity concentration in the channel are taken into consideration. The analytical model is implemented using MATLAB. A comparison of the simulations from technology computer aided design (TCAD) and that from the proposed analytical model, at room temperature, shows a satisfactory accuracy which is less than 5% for the whole voltage domain.

Keywords**—**LDMOS, MATLAB, RESURF, modeling, TCAD.

I. Introduction

THE LDMOS acts as an important component in intelligent power integrated circuits for the properties of superior isolation, low leakage current, and easy integration [1]-[3]. Optimal design of RF power amplifiers requires physical LDMOS models that should describe the device characteristics accurately over a wide range of biases and temperatures.

Several LDMOS models have been proposed [4]-[6], but a complete physical model is still missing. A frequently approach in modelling the LDMOS transistor on a circuit level is achieved by either a sub-circuit model [4], [7] or a semi-numerical model [8], [9]. The disadvantage of this approach is that, during circuit simulation, these models may increase the computation time, or may have convergence problems. Furthermore, most of these models lack an accurate description of one or more specific device characteristics. For instance, in the models of [8], a conventional low-power MOS model with uniform doping has been taken for the graded channel, while in the sub-circuit model of [7], the drift region is only described by a linear resistor. The drawback of the models [9] is that the potential drop over the channel varies only linearly with position.

For the development of power semiconductor device models, several effects have to be considered since they dominate the static and dynamic device characteristics. These effects are not described correctly by standard device models because their influence on low-power devices is less important or negligible [10]-[12]. So, better investigation of the physics of the HV devices and clear understanding of the special effects are needed.

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The modeling of the lateral structures came into play as these devices were integrated in standard technologies. Remarkable progress in the modeling field is conducted to geometrical approximations of the drift zone (regional approach), which seems to be the most promising approach.

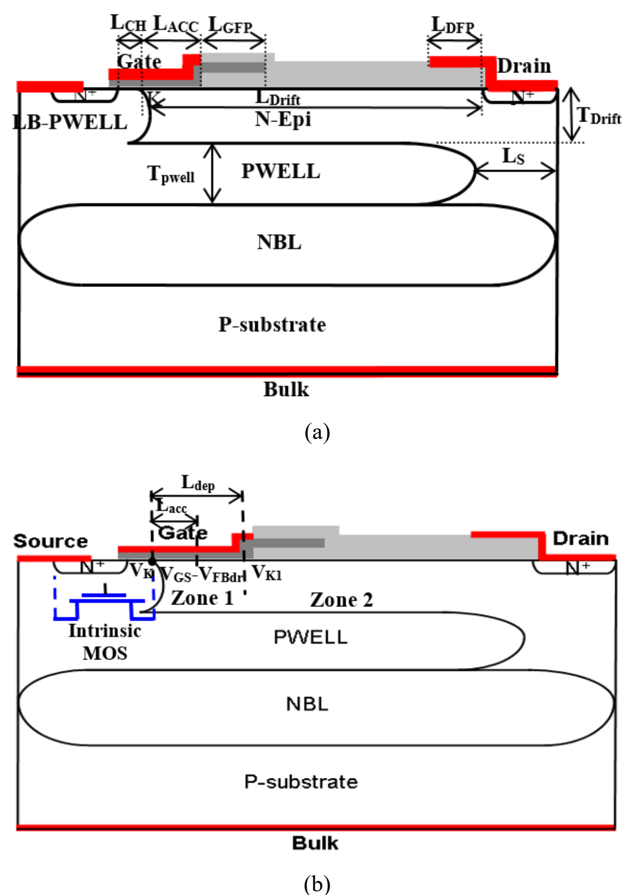

Fig. 1 The schematic cross-section of the RESURF LDMOS implemented in BiCMOS technology, a) Geometrical and technological parameters, and b) Critical electrostatic potentials

In the first part of this paper, an approach for physically modeling of the intrinsic MOS part and the drift region is presented. In the proposed model, all the physical effects are considered. The device charges are calculated and integrated to provide analytical expressions for the currents. The second part of the paper presents implementation of the model. Finally, the DC characteristics using the model are compared with the results of TCAD simulations showing good accuracy.

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II. Analytical Modelling of LDMOS

Some critical points are encountered in the attempt to analytically model a HV LDMOS. This is mainly related to the fact that a typical HV LDMOS structure is made of intrinsic MOS part and the extension of the drain, the architecture of which dictates the high voltage capabilities (see Fig. 1)

The drift region of the device is divided into two distinct parts as shown in Fig. 2. The first zone is a depleted area in which the carriers are injected by the intrinsic MOSFET, and the second zone is the non-depleted area at the drain side [13], [14].

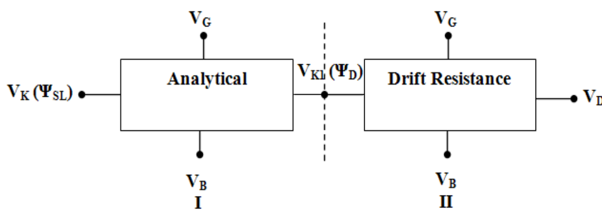


Fig. 2 Drift region functional partition

The technological parameters are indicated in Table I whereas the optimum geometrical parameters are shown in Table II.

TABLE I
THE TECHNOLOGICAL PARAMETERS OF THE N-CHANNEL LDMOS

P-WELL (1.25×10^{17} cm^{-3})	N-WELL (1.0×10^{17}cm^{-3})
PBL (2.5×10^{17} cm^{-3})	N-Epi (2.5×10^{16} cm^{-3})
NBL (3.5×10^{18} cm^{-3})	P-substrate (2.0×10^{15} cm^{-3})

TABLE II
THE OPTIMUM GEOMETRICAL PARAMETERS OF NLDMOS

L_{CH} = 1.00 µm	L_{Drift} = 6.00 µm
L_{ACC} = 0.40 µm	T_{Drift} = 1.80 µm
L_{GFP} = 1.50 µm	T_{pwell} = 2.15 µm
L_{DFP} = 0.50 µm	L_S = 1.65 µm

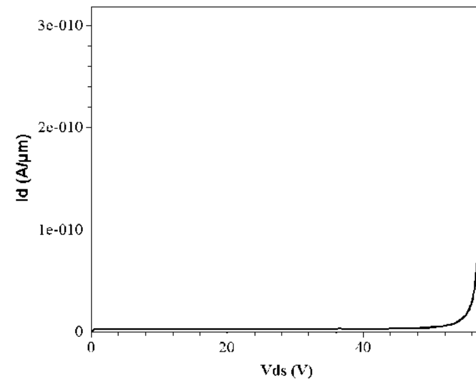
By using these parameters, the breakdown voltage of the nLDMOS and the impact ionization distribution are shown in Fig. 3. It is obvious that BV ≈ 60V and the avalanche breakdown is occurred at the Pwell / N-buried junction far from the surface. In Fig. 4, the electric field and potential lines distributions are illustrated at the breakdown condition. The potential lines are uniformly distributed over the drift region with surface electric field smaller than 3×10^5 V/cm.

A. Channel Region Model

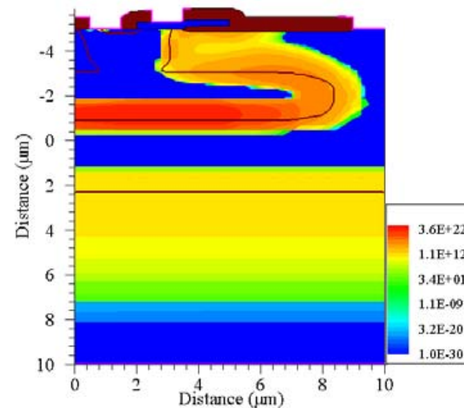
The model is derived based on the following basic assumptions:

1. The laterally non-uniform channel (P-body) doping density can be approximated as a simple exponential function,
2. The gradual channel approximation is valid,
3. The surface potential of the graded-channel varies linearly with position, and
4. A simple relationship between the inversion charge density Q_n and the local potential $\psi_s(x)$.

The non-uniform doping density along the channel can be approximated as an exponential function $N_A(x) = N_{A0}\exp(-\eta x / L_{ch})$, where N_{A0} is the concentration near the source and η is the doping gradient, chosen to be $\ln(N_{A0} / N_D)$, so that ($N_A(L_{ch})$ = N_D [14]–[17]. We use a piecewise-continuous electron velocity model [18].

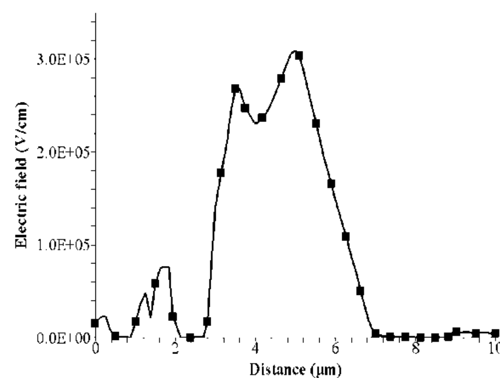


(a)



(b)

Fig. 3 (a) Breakdown voltage characteristic, and (b) Impact ionization distribution at *BV* of nLDMOS



(a)

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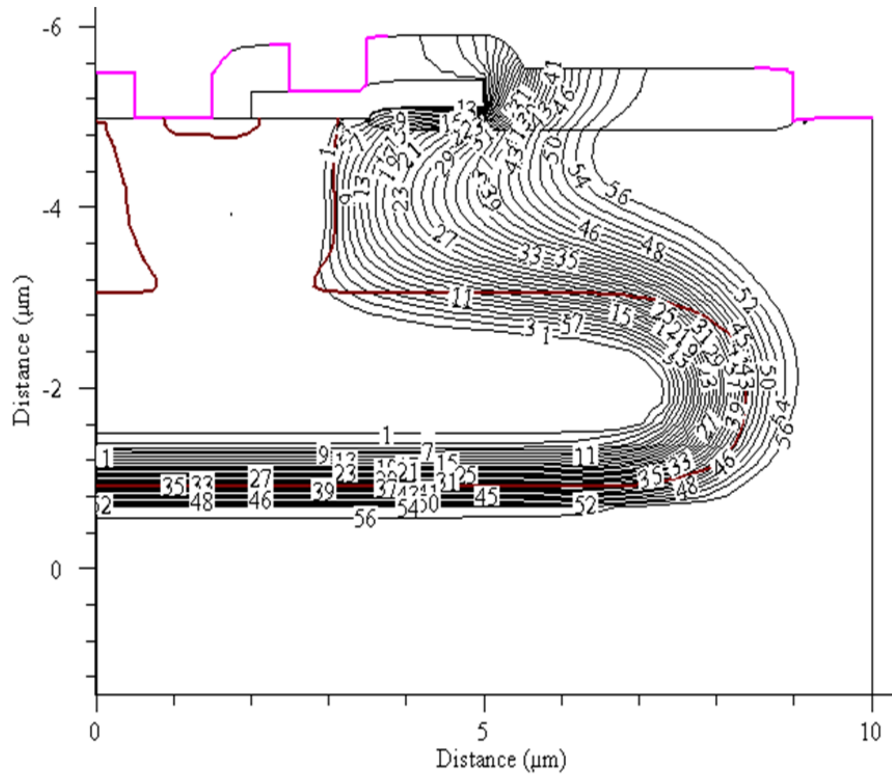

(b)

Fig. 4 (a) Electric field, and (b) potential distributions, of nLDMOS

$$v = \frac{\mu_{neff} E_x}{1 + (\mu_{neff} E_x / 2v_{sat})}, \qquad v \le v_{sat} \qquad (1)$$
$$= v_{sat}, \qquad \text{otherwise}$$

where E_x is the longitudinal electric field, v_{sat} ($\approx 10^7$ cm/s) is the saturated drift velocity, and, where μ_{n0} is the low field mobility, θ is the fitting parameter that defines the transverse-field dependence.

1) Channel Region Model

The threshold-voltage is defined as the gate-voltage at which the semiconductor surface is at the onset of strong inversion. Hence, the concentration near the source is higher than the concentration near the drain, so the semiconductor surface near the drain is inverted before that near the source. So, to obtain an expression of V_{TH}, we use the bulk doping concentration at the source side N_{A0}.

$$V_{TH} = V_{FB} + 2\varphi_F + \frac{\sqrt{4 q \varepsilon_s N_{Aeff} \varphi_F}}{C_{ox}}, \qquad (2)$$

where ϕ_F is the Fermi-potential ($\phi_F = \frac{KT}{q} \ln \frac{N_{A0}}{n_i}$)

2) Channel Current

The quasi-static channel current is described by $I_{ch} = -WvQ_n$ (W is the device width and Q_n is the inversion charge density) from source to drain, and by using $\frac{dQ_n}{dv} = C_{ox} + \overline{C_d}$, the Channel current in the linear region is [17]:

$$I_{ch} = -\frac{W \mu_{neff}}{L_{ch}[1 + (\mu_{neff} / 2v_{sat} L_{ch}) \quad V_K]}. \qquad (3)$$
$$[C_{ox}.(V_{GS} - V_T) + (C_{d0}.\eta.\phi_F) - 0.5 \quad (C_{ox} + C_{d0}).V_K].V_K$$

where V_K is the intrinsic drain voltage. $C_{ox} = \varepsilon_{ox} / t_{ox}$ is the capacitance of the of the oxide layer with permittivity ε_{ox} and thickness t_{ox} . $\overline{C_d}$ is the average depletion capacitance which assumed to be invariant along the channel.

$$\overline{C_d} = C_{d0}(1 - \frac{2\eta\phi_F}{V_k}) \text{ where, } C_{d0} = \sqrt{-(q\varepsilon_s N_{A0} / 4\phi_F)} \qquad (4)$$

In saturation, the current is saturated due to the electron velocity saturation at the source end of the channel. However, velocity saturation at the source and the drain side both can occur depending on the channel length and the channel region doping gradient.

If the channel is very long or the doping gradient is very

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small, the electron velocity saturation occurs at the drain end of the channel. On the other hand, if the gradient is very high, the inverted electron concentration is much higher at the drain end than the source end and the velocity will saturate there. Generally, to get an expression for the saturation current, the following differential equation is used:

$$\left.\frac{\partial I_{ch}}{\partial V_K}\right|_{V_K=V_{Ksat}}=0 \tag{5}$$

where V_{Ksat} is the value of the intrinsic drain voltage at the onset of current saturation.

$$V_{Ksat}=\frac{C_{ox}.(V_{GS}-V_T)+(C_{d0}.\eta.\phi_F)}{C_{ox}+C_{d0}} \tag{6}$$

Substituting (6) into (3), one gets;

$$I_{chsat}=-\frac{W\mu_{neff}}{2\ \ L_{ch}[1+(\mu_{neff}/2v_{sat}L_{ch})\ \ V_{Ksat}]}.\frac{0.5.[C_{ox}.(V_{GS}-V_T)+(C_{d0}.\eta.\phi_F)]^2}{(C_{ox}+C_{d0})} \tag{7}$$

This saturation current is general and independent on the location at which $v = v_{sat}$ (source side or K-point).

III. Drift Region Model

The flow chart of the modelling methodology, which represents the various cases, is shown in Fig. 5:

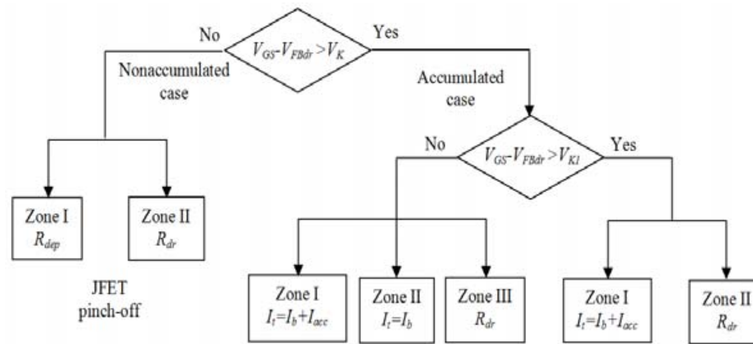

Fig. 5 Modeling flow chart

The model is split into two cases:
Case 1. The accumulated case, V_G-$V_{FBdr} > V_K$.
Case 2. The non-accumulated case, V_G-$V_{FBdr} < V_K$.
where V_{FBdr} is the flat band voltage, V_G is the gate voltage, V_K is the surface potential of the intrinsic MOS drain, and (V_G-V_{FBdr}) is the limit of the accumulation layer.

A. The Accumulated Case, V_G-$V_{FBdr} > V_K$

1. Case of V_{GS}-V_{FBdr}<V_{K1}

i. Zone I

The accumulation charge can be computed by using simple capacitance equivalence [4], [13], [15].

$$Q_{acc} = -C_{ox}.(V_{GS}-V_{FBdr}-\psi_s) \tag{8}$$

where C_{ox} is the oxide capacitance, ψ_s is the surface potential. The integration of the accumulation charge with the position leads to the current component given by the accumulation layer.

$$I_{acc}=-WQ_{acc}v. \tag{9}$$

where v is the carrier velocity, defined as in (1).

$$I_{acc}=-WQ_{acc}\frac{\mu_{aneff}E_x}{1+(\mu_{aneff}E_x/2v_{sat})}. \tag{10}$$

where $E_x=d\psi_s/dx$, and μ_{aneff} is the effective electron mobility in the accumulation region.

$$I_{acc}L_{acc}=\frac{W\mu_{aneff}.C_{ox}}{2\left[1+\mu_{aneff}\dfrac{(V_G-V_{FBdr}-V_K)}{2L_{acc}.v_{sat}}\right]}.\int_{V_K}^{V_G-V_{FBdr}}(V_G-V_{FBdr}-\psi_s)\ d\psi_s \tag{11}$$

$$\Rightarrow I_{acc}=\frac{W\mu_{aneff}.C_{ox}}{2.L_{acc}\left[1+\mu_{aneff}\dfrac{(V_G-V_{FBdr}-V_K)}{2L_{acc}.v_{sat}}\right]}.\left(V_G-V_{FBdr}-V_K\right) \tag{12}$$

The second type of charge present in *zone I* is the drift charge. The drift charge concentration is approximated constant for the drift zone.

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$$Q_b = -q.N_{dr}.y_{path} \quad (13)$$

where y_{path} is the depth of the current path. As for the accumulation current, the integration of the drift charge provides the expression for the drift current.

$$I_b = -WQ_b v. \quad (14)$$

where v is the carrier velocity, defined in (1).

$$I_b L_{acc} = \frac{qW\mu_{aneff}}{2\left[1+\mu_{aneff}\dfrac{(V_G - V_{FBdr} - V_K)}{2L_{acc}.v_{sat}}\right]}\int_{V_K}^{V_G - V_{FBdr}} y_{path}\, d\psi_s \quad (15)$$

$$\Rightarrow I_b = \frac{qW\mu_{aneff}N_{dr}.\tan\alpha}{2\left[1+\mu_{aneff}\dfrac{(V_G - V_{FBdr} - V_K)}{2L_{acc}.v_{sat}}\right]}\left(V_G - V_{FBdr} - V_K\right) \quad (16)$$

where *tan α* is the slope of the current path at the K-point.

$$I_t = I_{acc} + I_b \quad (17)$$

where I_t is the total current through the drift region.

ii. Zone II

Zone II represented by a current $I_t = I_b$

$$I_b = \frac{qW.\mu.N_{dr}.L_{acc}.\tan\alpha}{(d_{dep} - L_{acc})\left[1+\mu\dfrac{(V_G - V_{FBdr} - V_K)}{2L_{acc}.v_{sat}}\right]}\left(V_{K1} - V_G - V_{FBdr}\right) \quad (18)$$

iii. Zone III

Zone III is represented by a drift resistance R_{dr} as shown in the following. The drain current penetrates in the semiconductor to a depth referred here as Z_{dr}. The drain current equation can be written in the drift zone as follows:

$$I_{dr} = -WvQ_{dr} \quad (19)$$

where Q_{dr} is the drift region charge density, which is uniform $Q_{dr} = qnZ_{dr}$, $n_{dr} = N_{dr}$, where N_{dr} is the drift region doping concentration, and v is the carrier velocity defined in (1).

$$I_{dr} = qN_{dr}WZ_{dr}\frac{\mu_n E_x}{1+(\mu_n E_x / 2v_{sat})} \quad (20)$$

where $E_x = dV(x)/dx$

By integrating the above current relation over the drift region, an expression for the current in the drift region is obtained as follows:

$$I_{dr} = [qN_{dr}WZ_{dr} - \frac{I_{dr}}{2v_{sat}}]\mu_n\frac{dV(x)}{dx}$$

$$\Rightarrow \int_{L_{dr}} I_{dr}\,dx = [qN_{dr}WZ_{dr} - \frac{I_{dr}}{2v_{sat}}]\mu_n\int_{\Psi_D}^{V_D} dV(x)$$

$$\Rightarrow I_{dr}[L_{dr} + \frac{\mu_n(V_D - \Psi_D)}{2v_{sat}}] = qN_{dr}WZ_{dr}\mu_n(V_D - \Psi_D)$$

$$\Rightarrow I_{dr} = \frac{qN_{dr}WZ_{dr}\mu_n}{L_{dr}[1+\dfrac{\mu_n(V_D - \Psi_D)}{2v_{sat}.L_{dr}}]}.(V_D - \Psi_D) \quad (21)$$

As, $R_{dr} = \dfrac{(V_D - \Psi_D)}{I_{dr}} = \dfrac{L_{dr}\left[1+\dfrac{\mu_n(V_D - \Psi_D)}{2v_{sat}.L_{dr}}\right]}{qN_{dr}WZ_{dr}\mu_n}$

$$\Rightarrow R_{dr} = \frac{L_{dr}}{q\mu_n N_{dr}WZ_{dr}} + \frac{(V_D - \Psi_D)}{2qN_{dr}WZ_{dr}v_{sat}} \quad (22)$$

where, $L_{dr} = L - d_{dep}$, and, $Z_{dr} = T_{Drift} - Z_{dep}$

We notice that the expression of the drift resistance consists of two terms, the first one represents the drift resistance at low voltage conditions R_{d0}, and the second term represents the drift region resistance due to high voltage and current conditions R_{dvsat}.

$$R_{dr} = R_{d0} + R_{dvsat}$$

2. Case of $V_{GS} - V_{FBdr} > V_{K1}$

i. Zone I

$$I_{acc} = \frac{-W\mu_{aneff}.C_{ox}[(V_G - V_{FBdr} - V_{K1})^2 - (V_G - V_{FBdr} - V_K)^2]}{2d_{dep}\left[1+\mu_{aneff}\dfrac{(V_{K1} - V_K)}{2d_{dep}.v_{sat}}\right]} \quad (23)$$

and,

$$I_b = \frac{qW\mu.N_{dr}.L_{acc}.\tan\alpha}{2\left[1+\mu\dfrac{(V_{K1} - V_K)}{2d_{dep}.v_{sat}}\right]}\left(V_{K1} - V_K\right) \quad (24)$$

ii. Zone II

Zone II is represented by a drift resistance R_{dr}.

B. The Non-Accumulated Case

The accumulated case, $V_G - V_{FBdr} < V_K$.

i. Zone I

This area is modelled as a depletion resistance, which is associated with the so called JFET pinch-off. The starting point is Poisson's equation.

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$$\frac{dE}{dx} = \frac{\rho}{\varepsilon_s} \tag{25}$$

where E is the electric field and ρ is the charge density.

$$-\frac{d^2\psi_s}{dx^2} = \frac{\rho}{\varepsilon_s}, \ \rho = qN_{dr} \tag{26}$$

Ψ_s is the potential function of position which depends only on the lateral position. After the double integration of (26) between the limits Ψ_{SL} and Ψ_D, the following expression is obtained for the potential,

$$\psi_s(x) = \frac{qN_{dr}}{2\varepsilon_s}x^2 + \left[\frac{\Psi_D - \Psi_{SL}}{d_{dep}} + \frac{qN_{dr}}{2\varepsilon_s}d_{dep}\right]x + \Psi_{SL} \tag{27}$$

To link the potential variation with the position on the resistance of the depleted area, the simple formulation for the mobile charge can be used in conjunction with the conductance of a depleted zone.

$$n(x) = n_o \exp\left(\frac{q\psi_s}{kT}\right) \tag{28}$$

$$R_{dep} = \frac{\int_0^{d_{dep}} e^{\frac{q\psi_s}{kT}} d\psi_s}{q\mu n_o WT} \tag{29}$$

ii. Zone II

Zone II is represented by a drift resistance R_{dr}.

IV. Simulation of the Analytical Model

The analytical model was simulated using MATLAB. Before proceeding, the physical key constants and parameters are stated below in Table III.

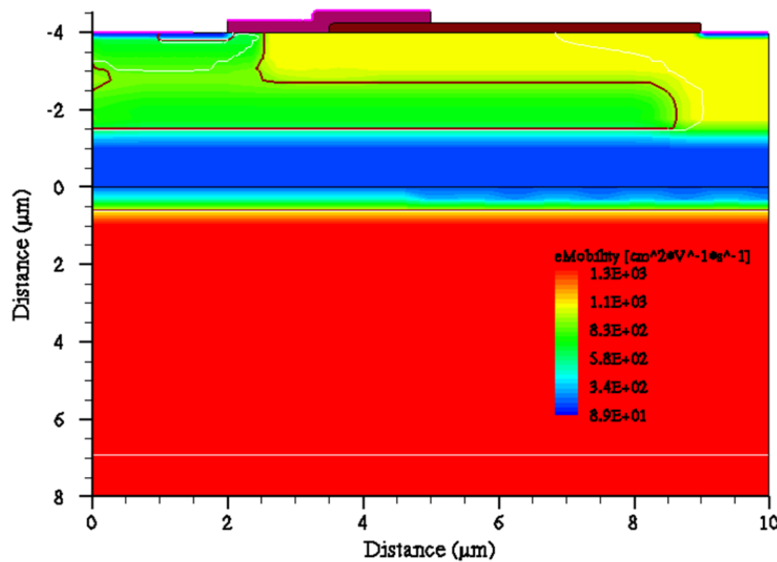
In the current relations of the implemented analytical model, the mobility is taken as 1025 cm^2/V.sec, which has excellent correspondence with the TCAD simulation results in Fig. 6(a). The current density distribution is also shown in Fig. 6(b). The distribution shows the slope of the current path at the K-point which is considered in our proposed model.

By using the above key constants and parameters, the threshold voltage of the device is equal to 0.576 V. The capacitances C_{gs} and C_{gk1} are equal to 6.3×10^{-15} F and 1.8×10^{-15} F, which are approximately matched with the value obtained from TCAD simulation.

TABLE III
Physical Key Constants and Parameters

$T = 1.8\times10^{-4}$ cm	$N_{dr} = 9.5\times10^{15}$ cm^{-3}
$C_{ox} = 4.5435\times10^{-7}$ F/cm^2	$N_{A0} = 9.5\times10^{17}$ cm^{-3}
$Temp$ = 300 K	Φ_F = 0.46513 V
$n_i = 1.482\times10^{10}$ cm^{-3}	$L_{dr} = 6.0\times10^{-4}$ cm
V_{Fbinv} = -0.95 V	$P_{well} = 1.5\times10^{17}$ cm^{-3}
V_{FBdr} = -0.2 V	$T_{pwell} = 2.15\times10^{-4}$ cm
$v_{sat} = 4.5\times10^{7}$ cm/sec	$L_s = 1.65\times10^{-4}$ cm
V_{ther} = 0.025875 V	

The I_D -V_{DS} characteristics of the nLDMOS are shown in Fig. 7. It is observed that the model approximately follows the behaviour of the TCAD simulated device, as V_{GS} is increased. The deviation of the analytical model from the TCAD simulation is due to the injection of carries in the drift region and the accumulation layer formation under the gate oxide. These phenomena are not taken into account in the analytical model, as their addition complicates the model.



(a)

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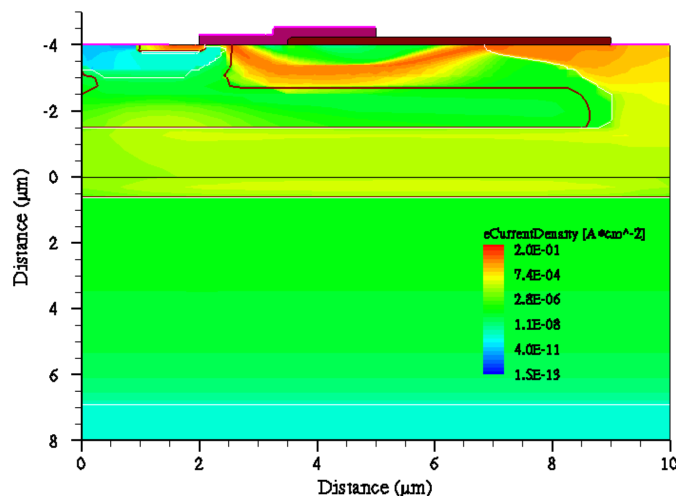

(b)

Fig. 6 (a) Mobility distribution, and (b) Current density distribution

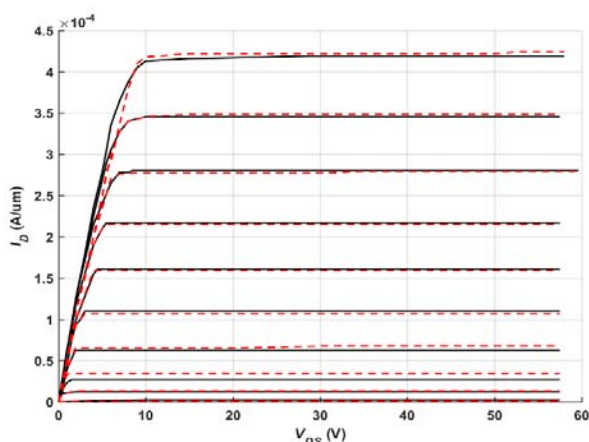

Fig. 7 Comparison of the TCAD simulation (Black solid curves) and the model simulation (Red dashed curves) for nLDMOS (V_{GS} = 0 – 3.3 V)

V. Conclusion

A methodology for physically modeling the LDMOS is presented. The physical effects of velocity saturation and mobility reduction in the channel and the drift region are included in the proposed analytical model. The proposed compact model is implemented by using MATLAB as a numerical computing environment. The comparison of the simulation results using SENTAURUS TCAD and the analytical model at room temperature shows a good agreement along the whole voltage domain.

References

[1] M. Mehrad, and A. A. Orouji, "Injected charges in partial SOI LDMOSFETs: a new technique for improving the breakdown voltage," *Superlattices Microstruct*., vol. 57, pp. 77-84, May 2013.

[2] N. Prasad, P. Sarangapani, K. N. S. Nikhil, N. Das Gupta, A. Das Gupta, and A. Chakravorty, "An improved Quasi-Saturation and charge model for SOI-LDMOS transistors," *IEEE Trans. Elect. Devices*, vol. 62, no. 3, pp. 919-926, Mar 2015.

[3] J. F. Yao, Y. F. Guo, T. Xia, J. Zhang, and H. Lin, "3D analytical model for the SOI LDMOS with alternating silicon and high-k dielectric pillars," *Superlattices and Microstructures*, vol. 96, pp. 95-103, Aug 2016.

[4] J. Victory., C. C. McAndrew, R. Thoma, K. Joardar, M. Kniffin, S. Merchant, and D. Moncoqut, "A Physically-Based Compact Model for LDMOS Transistors," *IEEE Proc. International Conference on Simulation of Semiconductor Processes and Devices SISPAD*, pp. 271-274, 1998.

[5] Y.-S. Kim, J. G. Fossum, and R. K. Williams, "New Physical Insights and Models for High-Voltage LDMOST IC CAD," *IEEE Trans. Electron Devices,* vol. 38, pp.1641-1649, July 1991.

[6] J. Jang, O. Tornblad, T. Arnborg, Q. Chen, K. Banerjee, Z. Yu, and R. W. Dutton, "RF LDMOS characterization and its compact modeling," *IEEE MTT S INT MICROWAVE SYMP DIG*, vol. 2, pp. 967-970, May 2001.

[7] J. Jang et al., "Circuit Model for Power LDMOS including Quasi-Saturation", *Proc. SISPAD*, pp. 15-18, 1999.

[8] M. Y. Hong, and D. A. Antoniadis, "Theoretical Analysis and Modeling of Submicron Channel Length DMOS Transistors", *IEEE Trans. Electron Devices*, vol. 42, no 9, pp. 1614-1622, 1995.

[9] Y. Chung, "LADISPICE-1.2: A Nonplanar-Drift Lateral DMOS Transistor Model and its Application to Power IC TCAD", *IEE Proc. Circuits Devices Syst.*, vol. 147, no 4, pp. 219-227, 2000.

[10] R. Kraus, and H. Mattausch, "Status and Trends of Power Semiconductor Device Models for Circuit Simulation", *IEEE Trans. Power Electronics*, vol. 13, no 3, May 1998.

[11] W. Fichtner, N. Braga, M. Ciappa, V. Mickevicius, and M. Schenkel, "Progress in Technology CAD for Power Devices, Circuits and Systems", *IEEE Proc. ISPSD*, pp. 1 – 9, 2005.

[12] *Modelling of high-voltage LDMOS in power ICs*, Agilent, 2006. http://www.paper.edu.cn/download_feature_paper.php?serial_number=Agilent2006D002.

[13] C. Anghel, *High voltage devices for standard MOS technologies-characterisation and modelling*, Ph.D. dissertation, EPFL, 2004. http://biblion.epfl.ch/EPFL/theses/2004/3116/EPFL_TH3116.pdf.

[14] Y. S. Chauhan, C. Anghel, F. Krummenacher, A. M. Ionescu, M. Declercq, R. Gillon, S. Frere, and B. Desoete, "A Highly Scalable High Voltage MOSFET Model", *IEEE Proc. ESSDERC*, pp.270-273, 2006.

[15] C. W. Tang, and K. Y. Tong, "A compact large signal model of LDMOS," *Solid-State Electronics*, vol. 46, no. 12, pp. 2111-2115, 2002.

[16] J. Meng, S. Gao, J. Ning, and C. D. Ming Ke, "The analysis and modeling of on-resistance in high-voltage LDMOS", *IEEE Proc. International Conference on Solid-State and Integrated Circuit Technology ICSICT*, pp. 1327 – 1329, 2006.

[17] A. Aarts, N. D'Halleweyn, and R. van Langevelde, "A surfacepotential-based high-voltage compact LDMOS transistor model," *IEEE Trans. Electron Devices*, vol. 52, no. 5, pp. 999- 1007, 2005.

[18] J. C. W. Ng, and J. K. O. Sin, "Extraction of the Inversion and Accumulation Layer Mobilities in n-Channel Trench DMOSFETs", *IEEE Tran. Electron Devices*, vol. 53, no. 8, pp. 1914 – 1921, 2006.

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