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Design of 900 MHz High Gain SiGe Power Amplifier with Linearity Improved Bias Circuit

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***Abstract*—**A 900 MHz three-stage SiGe power amplifier (PA) with high power gain is presented in this paper. Volterra Series is applied to analyze nonlinearity sources of SiGe HBT device model clearly. Meanwhile, the influence of operating current to IMD3 is discussed. Then a β-helper current mirror bias circuit is applied to improve linearity, since the β-helper current mirror bias circuit can offer stable base biasing voltage. Meanwhile, it can also work as predistortion circuit when biasing voltages of three bias circuits are fine-tuned, by this way, the power gain and operating current of PA are optimized for best linearity. The three power stages which fabricated by 0.18 μm SiGe technology are bonded to the printed circuit board (PCB) to obtain impedances by Load-Pull system, then matching networks are done for best linearity with discrete passive components on PCB. The final measured three-stage PA exhibits 21.1 dBm of output power at 1 dB compression point (OP1dB) with power added efficiency (PAE) of 20.6% and 33 dB power gain under 3.3 V power supply voltage.

***Keywords*—**High gain power amplifier, linearization bias circuit, SiGe HBT model, Volterra Series.

I. Introduction

RECENTLY, the radio frequency integrated circuit (RFIC) develops rapidly due to growing demands of wireless communication systems. However, PA has a long way to catch up with RFIC development trends of low power consumption and high level of integration. The reason is that for limitation of breakdown voltage and power performance, most commercial PAs adopt III-V HBTs rather than silicon based semiconductor devices. Nevertheless, researchers have focused on SiGe PA [1], [2] for its better noise characteristic, better thermal conductivity and better compatibility with the Si technology when compared with its III-V HBT counterparts. Meanwhile, SiGe HBT has higher breakdown voltage and better power performance than CMOS transistor for being applied in silicon-based PA applications.

Since linearity is a critical performance index for SiGe PA and wireless communication system, many efforts have been paid to improve the linearity of SiGe HBT, and the study of device model is indispensable for linearity improvement. With the help of device model analysis [3], it can be known that the sources of nonlinearity are found out, then influences of these nonlinearity sources will be changed and partially cancelled with each other under different biasing conditions. Though the working mechanism of nonlinearity sources in the device model is complicated, it can be analyzed clearly with Volterra Series [4], [5], which is a popular tool to analyze the weak nonlinearity of device model. Besides, Volterra Series is also used to analyze the influences of source and load impedances to small signal linearity [3], [5]. In general, the power transistor of PA operates at small signal state when RF input power is low, and goes into large signal operation with increasing RF input power. It is always a headache problem to analyze the nonlinearity sources in large signal model. However, Volterra Series is applies to analyze IMD3 and IM3 of PA [6], [7] [9], then sources of nonlinearity and their working mechanisms can be explained. The conclusions of analysis are not only beneficial for modeling nonlinearity sources of device, but also favorable to circuit design. In terms of circuit design, a lot of work has been done to improve the linearity of PA. The PAs with cascode and differential structures are usually applied for improving linearity, because they can avoid linearity degeneration caused by C_{BC} [8] and second order distortion [9], respectively. But their disadvantages on poor PAE cannot be ignored. Beyond that, through the method of predistortion, feedback [10], bias circuit selection [11] etc., the linearity of PA can be compensated and improved effectively. Especially, the bias circuit with predistortion technique can compensate the linearity degeneration [6], this method can get obvious improvement on IMD3 and IP1dB (input power at 1 dB gain compression point). The aforementioned bias circuit in [6] adopts β-helper Widlar current mirror structure, which has been widely used in high performance PAs [11]-[13]. In addition to excellent current driving capability, the bias circuit can also offer gain compensation and fine-tuned operating current by varying the biasing voltage of bias circuit.

In this paper, a high power gain SiGe PA operating in 900 MHz is presented. It is composed of three power stages with linearity improved bias circuits and matching networks. In Section II, the model of SiGe HBT is analyzed with Volterra Series. And the influence of operating current on IMD3 is analyzed and discussed. In order to improve linearity, the corresponding β-helper Widlar current mirror is adopted to fine tune the operating current. Finally, the three power stages with bias circuits are designed on-wafer, and measurement of three-stage PA is done with off-chip matching networks. The measurement results of the PA are shown in Section III.

II. Analysis of PA

As PA is fabricated by SiGe technology, the common emitter

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nonlinear model of SiGe HBT is shown in Fig. 1. V_{IN} is the input voltage source of SiGe HBT. v_π is the base emitter voltage and g_m is the transconductance of the SiGe HBT. I_B is base current and I_C is collector current, both of them are the function of nonlinearity v_π. C_{diff} is the diffusion capacitance of base emitter junction, and it is the main contributor of nonlinearity. It is assumed to be linear with I_C. The depletion capacitance of base emitter junction is C_j, and it is regarded as a linear capacitor. Z_S and Z_L are source and load impedances, respectively, their corresponding admittances are Y_S and Y_L. Besides the aforementioned parameters, which describe small signal linearity of SiGe HBT, the base collector capacitance C_{BC} and collector substrate C_{CS} are large signal nonlinearlity sources. However, when the junction of device is under forward bias condition, depletion capacitance of junction is much smaller than diffusion capacitance of junction. Since C_{CS} is depletion capacitance, the distortions caused by C_{CS} can be neglected when they are compared with the distortions caused by diffusion capacitors [14]. So Ccs can be neglected in SiGe HBT model. In general, C_{BC} is assumed to be linear [9]. Then this model can be analyzed with Volterra Series.

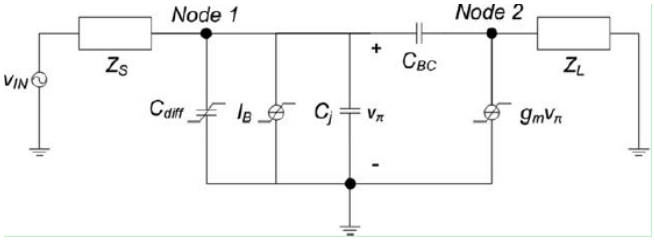


Fig. 1 Nonlinear model of SiGe HBT [6]

The model in Fig. 1 is expressed in Volterra Series with format of matrix, so we can get the first order Volterra kernel voltages $V_{11}(s)$ and $V_{12}(s)$ in node 1 and node 2. The matrix is shown as [6] [9]:

$$\begin{bmatrix} Ys(s)+g_{\pi 1}+s\left(C_{diff1}+C_j+C_{BC}\right) & -sC_{BC} \\ g_{m1}-sC_{BC} & Y_L(s)+sC_{BC} \end{bmatrix} \times \begin{bmatrix} V_{11}(s) \\ V_{12}(s) \end{bmatrix} = \begin{bmatrix} Y_S(s)V_{IN}(s) \\ 0 \end{bmatrix} \quad (1)$$

where in (1) and (3) s=jω. C_{diff1} is first order current source coefficient caused by C_{diff}. $g_{\pi 1}$ and g_{m1} are the admittance of first order current source I_B and I_C in Fig. 1 [9]. In the way described in [9], the second and third order Volterra kernel voltages are obtained, then IMD3 can be represented. In (4), i_{c3} is third order nonlinearity current of collector, similarly, i_{b3} and i_{diff3} are third order nonlinearity current of I_B and C_{diff}.

$$\text{IMD3} = \frac{3}{4}{V_{IN}}^2 \left|\frac{V_{32}(S_1,S_2,S_3)}{V_{12}(S_1)}\right| \quad (2)$$

$$V_{12}(s) = \frac{-Y_S(s)[g_{m1}-sC_{BC}]}{(Y_L(s)+sC_{BC})[Y_S(s)+g_{\pi 1}+s\left(C_{diff1}+C_j+C_{BC}\right)]+sC_{BC}(g_{m1}-sC_{BC})} \quad (3)$$

$$V_{32}(s) = \frac{-(Y_S(s_1+s_2+s_3)+g_{\pi 1}+(s_1+s_2+s_3)(C_{diff1}+C_j+C_{BC}))i_{c3}}{M(s)} + \frac{g_{m1}(1-\frac{(s_1+s_2+s_3)C_{BC}}{g_{m1}})(i_{b3}+i_{diff3})}{M(s)} \quad (4)$$

where, in (2) and (4) $M(s)=[Y_S(s_1+s_2+s_3)+g_{m1}+(s_1+s_2+s_3)(C_{diff1}+C_j+C_{BC})](Y_L(s_1+s_2+s_3)+C_{BC})+(s_1+s_2+s_3)C_{BC}(g_{m1}-(s_1+s_2+s_3)C_{BC})$ and $s_1=s_2=j\omega_1$, $s_3=-j\omega_2$. By substituting (3) and (4) into (2), then for the simplification of IMD3, C_{BC} is set to be zero [4]. Then IMD3 can be written as:

$$\text{IMD3} = \frac{3}{4}{V_{IN}}^2 \left| \frac{\left(\frac{\left(Y_S(s_1+s_2+s_3)+g_{\pi 1}+(s_1+s_2+s_3)(C_{diff1}+C_j)\right)i_{c3}}{g_{m1}}-(i_{b3}+i_{diff3})\right)}{[Y_S(s_1+s_2+s_3)+g_{m1}+(s_1+s_2+s_3)(C_{diff1}+C_j)](Y_L(s_1+s_2+s_3))} \times \frac{Y_L(s_1)[Y_S(s_1)+g_{\pi 1}+s_1(C_{diff1}+C_j)]}{Y_S(s_1)} \right| \quad (5)$$

The collector current I_C can be expressed as:

$$I_C = I_Q e^{\frac{v_\pi}{V_T}} \quad (6)$$

where I_Q is operating current, V_T is thermal voltage of transistor. With Taylor series, I_C can be rewritten as:

$$I_C = I_Q\left[\frac{v_\pi}{V_T}+\frac{1}{2}\left(\frac{v_\pi}{V_T}\right)^2+\frac{1}{6}\left(\frac{v_\pi}{V_T}\right)^3+\cdots\right] \quad (7)$$

As the first order Taylor coefficients can be expressed as [6]:

$$g_{m1} = \frac{I_Q}{V_T} \quad (8)$$

$$g_{\pi 1} = \frac{g_{m1}}{\beta} \quad (9)$$

$$C_{diff1} = \tau_F g_{m1} \quad (10)$$

where β is current gain of transistor, and τ_F is forward transmit time [6]. By substituting (8)-(10) into (5), IMD3 can be rewritten as:

$$\text{IMD3} = \frac{3}{4}{V_{IN}}^2 \left|K\left(Bi_{c3}-\left(i_{b3}+i_{diff3}\right)\right)\right| \quad (11)$$

$$B = \frac{V_T Y_S(s_1+s_2+s_3)}{I_Q}+\frac{1}{\beta}+(s_1+s_2+s_3)\left(\tau_F+\frac{V_T C_j}{I_Q}\right) \quad (12)$$

$$K = \left|\frac{\frac{Y_L(s_1)}{Y_S(s_1)}\left[Y_S(s_1)+\frac{I_Q}{\beta V_T}+s_1\left(\frac{\tau_F I_Q}{V_T}+C_j\right)\right]}{\left[Y_S(s_1+s_2+s_3)+\frac{I_Q}{V_T}+(s_1+s_2+s_3)\left(\tau_F\frac{I_Q}{V_T}+C_j\right)\right](Y_L(s_1+s_2+s_3))}\right| \quad (13)$$

$$K = \left|\frac{Y_S(s_1)+\frac{I_Q}{\beta V_T}+s_1\left(\frac{\tau_F I_Q}{V_T}+C_j\right)}{\left[Y_S(s_1+s_2+s_3)+\frac{I_Q}{V_T}+(s_1+s_2+s_3)\left(\tau_F\frac{I_Q}{V_T}+C_j\right)\right](Y_S(s_1))}\right| \quad (14)$$

$$K = \left| \frac{Y_S(s_1)+\frac{I_Q}{\beta V_T}+s_1\left(\frac{\tau_F I_Q}{V_T}+C_j\right)}{\left[Y_S(s_1+s_2+s_3)+\frac{I_Q}{V_T}+(s_1+s_2+s_3)\left(\tau_F\frac{I_Q}{V_T}+C_j\right)\right](Y_S(s_1))} \right| \quad (15)$$

It is inferred from (14) that K is a function of I_Q with all parameters assumed to be constants; the values of these constant parameters are obtained from simulation of device model in 0.18 μm SiGe technology. In general, Z_L and Z_S are base and collector resistors whose values will not change with frequency. So it is reasonable to assume that $Y_S(s_1)= Y_S(s_1+s_2+s_3)$, $Y_L(s_1)=Y_L(s_1+s_2+s_3)$. By replacing the aforementioned constant parameters with simulated values of PA in Fig. 2, it can be known that though the I_Q is a variable, the influence of I_Q to K is negligible. So K can be regarded as a constant coefficient which represents the amplitude variation of third order nonlinearity current Bi_{c3}-(i_{b3}+i_{diff3}). But in (13), B is the coefficient of i_{c3}, and B will decrease when I_Q is increasing. Then, (12)-(14) show that third order nonlinearity current Bi_{c3}-(i_{b3}+i_{diff3}) will decrease with decrease of B, and the corresponding IMD3 will decrease. Meanwhile, as it is shown in (13) and (14), when alternating current gain β is a variable and other parameters are assumed to be constants, the increasing of β will lead to decrease of B and K. Then, the decrease of B and K will induce the decrease of third order nonlinearity current Bi_{c3}-(i_{b3}+i_{diff3}) and IMD3. Overall, IMD3 will decrease with increasing of I_Q and current gain [4], [6], this conclusion offers important clues to improve the linearity of SiGe PA.

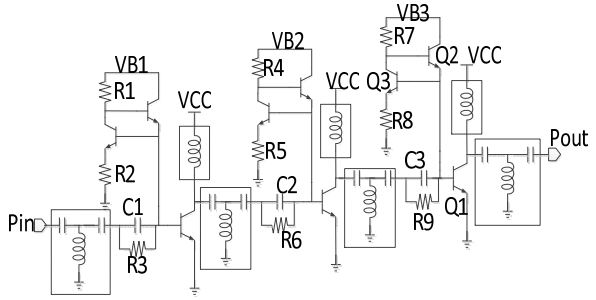


Fig. 2 Topology of three stage PA. (The components in the dotted rectangle are discrete components)

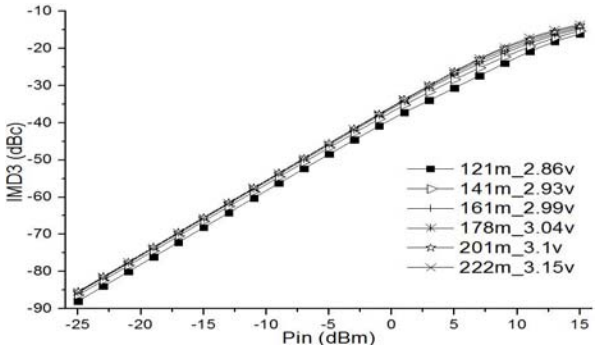


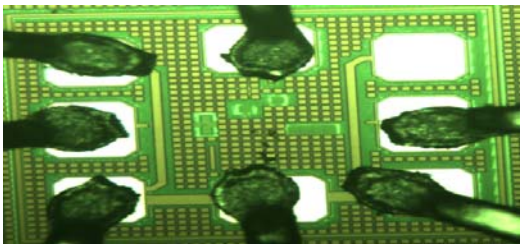
Fig. 3 The change of IMD3 versus operating current obtained by post-simulation of last power stage

III. Design and Measurement of PA

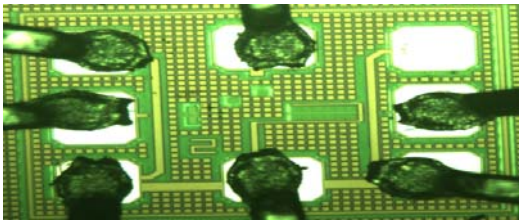
Based on the analysis and conclusion of Section II, the linearity improvement of PA can be done by increasing operating current and current gain of power transistor. The increase of operating current and current gain can be realized by changing the biasing voltage of bias circuit, so the bias circuit not only provides bias voltage, but also can improve linearity by reducing IMD3. According to above considerations, the bias circuit of β-helper Widlar current mirror structure [11], [12] is adopted as it is shown in Fig. 2. On one hand, this kind of bias circuit can compensate base emitter voltage drop of power transistor caused by increasing base current when RF input power is increasing. Thus, the base bias voltage can be kept steady and the linearity of power transistor is improved over wide input power range. On the other hand, by adjusting the bias voltage VB1 and VB2 in Fig. 2, the PA can provide increased gain which can compensate the decrease of gain at input power of 1 dB compression point [6]. So a constant overall power gain and higher output power of 1 dB gain compression point can be obtained. By adjusting VB3 in Fig. 2, the operating current is increased and corresponding IMD3 can be improved as predicted in Section II. Meanwhile, the parallel RC network at the base of each power transistor is used as anti-oscillation network. In order to show the influence of bias circuit to IMD3, the post-simulation results of third stage of PA are shown in Fig. 3, then the relationship of bias voltage and IMD3 of PA is depicted as follows. In Fig. 3, IMD3 of this power stage is increased with the increasing operating current and power gain. The simulated results are consistent with the analysis results of Volterra Series in Section II. However, the increment of IMD3 is reduced at larger bias voltage and operating current, the reason is that power performance of PA will not be improved obviously when the increasing operating current is near the optimum current density corresponding f_T of power transistor. So the final bias voltage and operating current of third power stage are set as 2.99 V and 160 mA for better linearity.

The three power stages of PA are fabricated by 0.18 μm SiGe technology, and the high breakdown voltage HBT is adopted as power transistor, whose emitter area is 28.8 μm^2. So the supply voltage is 3.3 V. In order to get high power gain, three power stages are cascaded with the last power stage biased in class AB mode. The first stage provides high power gain, the second stage provides enough input power for the output stage and the third stage provides high output power. The number of power transistors in each stage is 4, 12 and 72, respectively. The layout of each stage is shown in Figs. 4 (a)-(c). The choke inductor and matching networks are made with chip inductors and chip capacitors on the PCB as shown in Fig. 4 (d). Maury Load-Pull system which connects to the SMA ports of the corresponding PCB is utilized to get input and output impedances of each power stage, and the reference plane is calibrated to the point of transmission line on PCB which is near the input of the power stage chip. For the transmission line between SMA port and the calibration plane, it can be calibrated out by the measurement data of same length transmission line on another calibration PCB. Thus, the

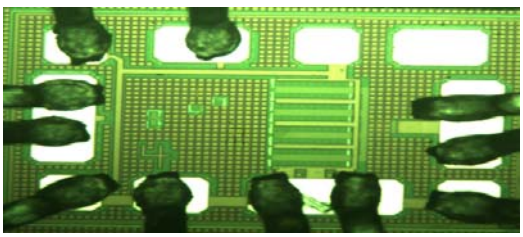
measured impedances include not only impedance of power stage but also those of bonding wire and part of transmission line on PCB, and the measured impedances are obtained with input power of 3dB compression point, so they can be regarded as large signal impedances. The measured optimum source and load impedances of first power stage are 43.59+j24.34 and 67.12+j15.04. For the second power stage, the optimum source and load impedances are 24.89+j4.61 and 22.37+j5.57, the optimum source and load impedances of third stage are 11.14-j5.66 and 6.11-j2.78. Then the input matching and inter-stage matching network are based on highest gain matching, and the output matching network is done for best linearity. All the band-pass matching networks are done by T match network for its higher degree of freedom.



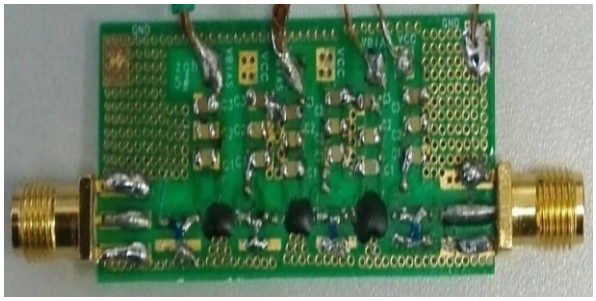
(a)



(b)



(c)



(d)

Fig. 4 Layout of (a) first power stage (b) second power stage (c) third power stage and (d) test board

The test board is shown in Fig. 4 (d), all the meatal layers of supply voltage are connected together on the back of PCB, so is the metal layers of ground. The decouple capacitors are connected between ground and biasing voltages which include supply voltage and biasing voltages of three bias circuits. The measurement of test board is accomplished by Agilent N5247A vector network analyzer. As aforementioned, biasing current of last stage is fine-tuned from 160 mA to 180 mA to improve linearity, the power performance comparison of PA operating at 180 mA and 200 mA is shown in Fig. 6, since the restrict of test equipment, the output power is measured instead of IMD3. The OP1dB has been improved 1 dBm when the operating current is tuned from 180 mA to 200 mA. This comparison result is also in accord with the analysis results of Volterra Series. During the measurement, because of unexpected power degrade of second stage, the VB2 is reduced for more output power. At last, the biasing currents of three stages are 15.6 mA, 6 mA and 180 mA, respectively. The measured S-parameter and power performance are shown in Figs. 5 and 6, from which we can know that the measured PA shows OP1dB of 21.1 dBm with 33 dB power gain and 20.6% PAE. The power performances of PA operating at frequency of 850 MHz and 950 MHz are shown in Table I. It is inferred from the measured S11, S22 and Table I that the performance of PA keeps steady in 100 MHz bandwidth. Because the center frequency of input matching network shifts to frequency higher than 900 MHz, performance of higher frequency is better than lower frequency in bandwidth of 850 MHz to 950 MHz.

TABLE I
COMPARISON OF MEASURED PERFORMANCE OF PA AT DIFFERENT FREQUENCIES

	IP1dB（dBm）	OP1dB（dBm）	Gt(dB)	PAE（%）
850M	-11.5	20.9	33.47	18.31
900M	-10.75	21.1	32.98	20.59
950M	-9.25	21.2	31.43	22.05

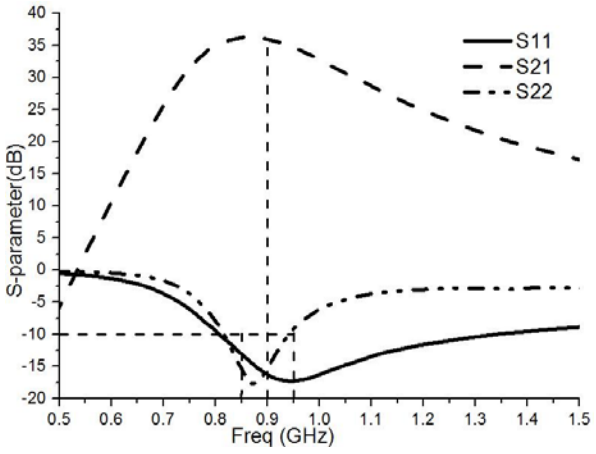


Fig. 5 Measured S-parameter of three-stage PA

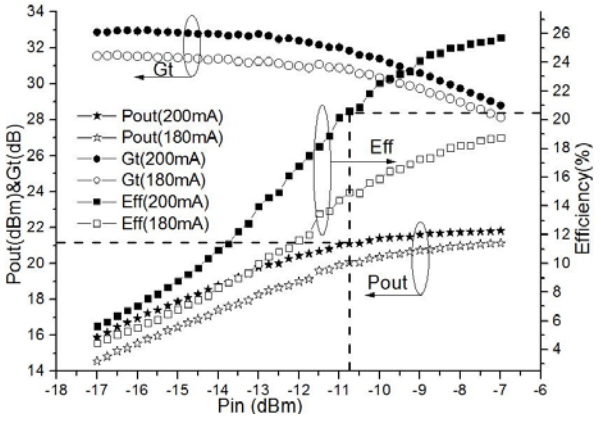


Fig. 6 Measured P1dB, Gain and PAE of three-stage PA

IV. Conclusion

This paper presents a three-stage linearity improved and high gain SiGe PA which works on 900 MHz. Volterra Series is successfully applied to deduce and analyze nonlinearity sources in SiGe HBT model. Then influences of current gain and operating current to IMD3 is discussed. The β-helper current mirror structure is utilized to improve linearity, and the biasing voltages of three bias circuits are fine tuned to obtain the optimum power gain and operating current for best linearity. For the power stages fabricated with 0.18 um SiGe technology, their impedances are measured by load-pull system, then all the matching networks are made on test board. The cascaded PA shows OP1dB of 21.1 dBm with PAE of 20.6%, and the measured power gain is 33 dB. And the measured power performance can keep steady in 100 MHz bandwidth.

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