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Simulation of High Performance Nanoscale Partially Depleted SOI n-MOSFET Transistors

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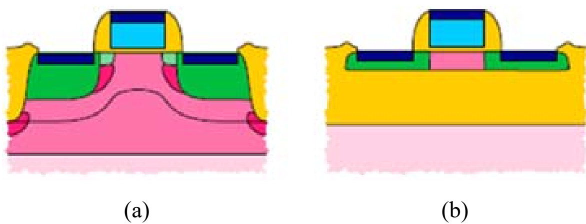
***Abstract*—**Invention of transistor is the foundation of electronics industry. Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has been the key for the development of nanoelectronics technology. In the first part of this manuscript, we present a new generation of MOSFET transistors based on SOI (Silicon-On-Insulator) technology. It is a partially depleted Silicon-On-Insulator (PD SOI MOSFET) transistor simulated by using SILVACO software. This work was completed by the presentation of some results concerning the influence of parameters variation (channel length L and gate oxide thickness T_{OX}) on our PDSOI n-MOSFET structure on its drain current and kink effect.

***Keywords*—**SOI technology, PDSOI MOSFET, FDSOI MOSFET, Kink Effect, SILVACO TCAD.

I. Introduction

SOI technology has now been widely demonstrated and recognized to be a mature and viable alternative to mainstream bulk Si for the realization of high-speed, low-power digital, and analog CMOS circuits, as well as niche applications under extremely high temperature or radiation operating conditions [1], [2].



(a) (b)

Fig. 1 Cross-section of a (a) bulk and a (b) SOI MOSFET: The SOI device is separated from the mechanical substrate by an insulating layer [5]

Compared to bulk, the basic characteristic of SOI technology is the separation of the top active region from the underlying mechanical substrate by a thick insulator layer (Fig. 1). This difference leads to some advantages over bulk silicon [3]:

- Reduction of the substrate parasitic capacitances. The reduction of the total capacitance of a MOSFET will increase the cut-off frequency of the transistor, allowing to use circuits at higher frequency.
- Small devices without latch-up. The buried oxide prevents any current from flowing between devices, eliminating the latch-up effect.
- Reduction of short-channel effects. In fully-depleted devices, the space charge in the thin film is well controlled by the gate, reducing the loss of gate control experienced in short-channel MOSFETs.
- Improved subthreshold slope. The lower inverse subthreshold slope, compared to bulk, allows better performances at low supply and the FET shows higher efficiency due to the lower dependence on the body potential.
- Reduction of the substrate noise. The insulator prevents from high crosstalk through the substrate in mixed-mode HF circuits [4].

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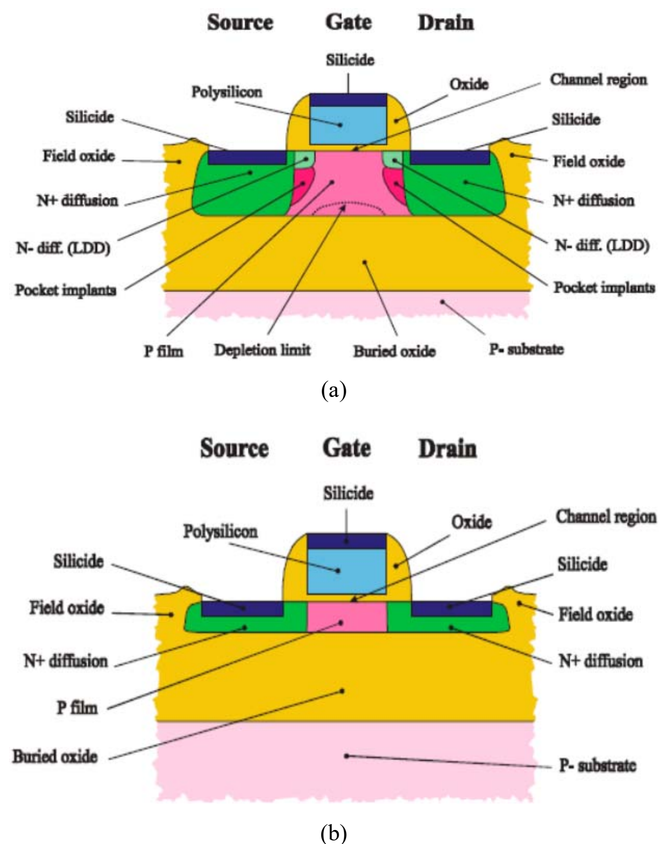

Fig. 2 (a) Structure of partially depleted SOI MOSFET and (b) structure of fully depleted SOI MOSFET [7]

Depending on the thickness of the top silicon layer, the silicon thin-film may be fully or partially depleted (FD or PD, respectively). When the top silicon layer is large (top than 50 nm), the depletion zone does not reach the box, and a neutral

zone is thus observed, as shown in Fig. 2 (a). In this case, we talk about the partially depleted transistors (PD SOI MOSFET). On the other hand, when the thickness of the silicon film is sufficiently thin for the depletion zone or each the box (Fig. 2 (b), the term called a fully depleted transistor (FDSOI MOSFET) is used [6].

II. Partially Depleted

An SOI MOSFET is said to be partially depleted when there is a neutral region below the gate, and the thickness of silicon film is larger than the depletion region as shown in Fig. 2 (b). For the thicknesses, smaller than the depletion, the transistor is said to be fully depleted. The behavior of partially depleted MOSFET is very similar to their bulk counterpart, and the neutral zone in SOI, also called body, corresponds to the local well in bulk. The differences are more important when the body is left floating. These effects are undesirable especially for analog circuits. Adding a body contact to partially depleted SOI MOSFET eliminates these undesirable effects and makes it behave like a bulk MOSFET [8].

III. Kink Effect in PD SOI N-MOSFET

The kink effect consists of the appearance of a kink in the output characteristics of an SOI MOSFET working in strong inversion, as shown in Fig. 3. The kink is very strong in n-channel transistors but is usually absent from p-channel devices.

When the transistor is operating in saturation, the hole current linked to impact ionization becomes non-negligible. The holes are pushed back by the transverse and longitudinal electric fields to the non-deserted body area where the potential is lowest. Because of the electrical insulation, these holes accumulate in the body zone throughout their lifespan, see Fig. 3. By increasing V_{DS}, the rate of holes in body zone increases. Linked to this variation of charges in the body zone, its potential increases, and it is given by the following relation [9].

$$I_{holes.gen} = I_{S0}\left(\exp\left(\frac{qV_{BS}}{nkT}\right) - 1\right) \quad (1)$$

where, $\mathbf{I_{holes,gen}}$ is the hole current generated near the drain, $\mathbf{I_{S0}}$ is the saturation current of the source-body diode, V_{BS} is the potential of the floating body, **n** is the ideality factor of the diode.

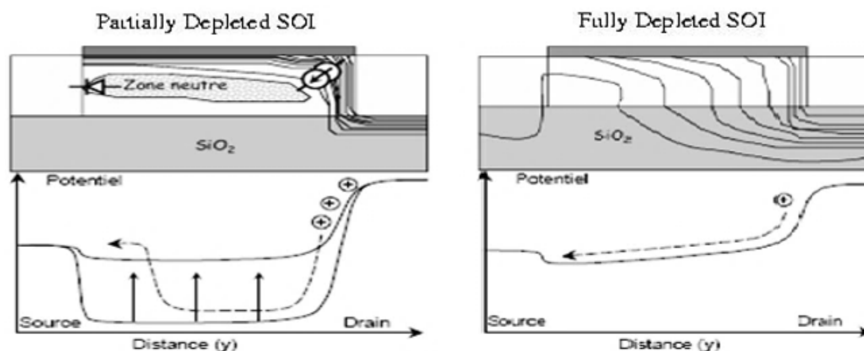

Fig. 3 Potential in neutral region from source to drain in partially depleted SOI and fully depleted SOI Devices [12]

The increase of body potential gives rise to lowering of threshold voltage and source-body potential barrier. More minority carriers are able to flow from source to the channel, thereby causing an excess drain current and producing many more pairs through the avalanche process. This positive feedback results in a sudden increase in I_D or "kink" in output characteristics.

After the establishment of the kink, the source, the body zone, and the drain form a structure comparable to an NPN type bipolar transistor. The base of this transistor is powered by the hole current resulting from impact ionization. When the latter is sufficiently high, the parasitic bipolar transistor becomes conductive, resulting in an increased net drain current, sometimes referred to as second kink [10].

Now, let us consider the case of a thin-film, fully depleted SOI n-channel MOSFET. It has been shown [11] that the electric field near the drain is lower in the fully depleted device than in partially depleted one. As a result, less electron-hole pair generation takes place in the fully depleted device. Also, contrary to the case of a partially depleted transistor, the source-to-body diode is "already forward biased" due to the full depletion of the film, and therefore, holes can readily combine in the source without having to raise the body potential there. This explains why thin film fully depleted n-channel MOSFETs are free of kink effect.

IV. Device Simulation

Fig. 4 shows (a) the schematic view of the PDSOI n-MOSFET, (b) mesh view of PDSOI n-MOSFET and (c) doping profile view of PDSOI n-MOSFET, simulated by using SILVACO Software, where gate oxide thickness T_{ox}=0.017 µm, silicon film thickness T_{Si}=0.3µm buried oxide thickness T_{Box}=0.4µm,drain and source concentration N_D=1x10^{20} cm^{-3}, substrate concentration N_A=1x10^{17} cm^{-3}, channel length, gate length, drain length and source length are about 1 µm.

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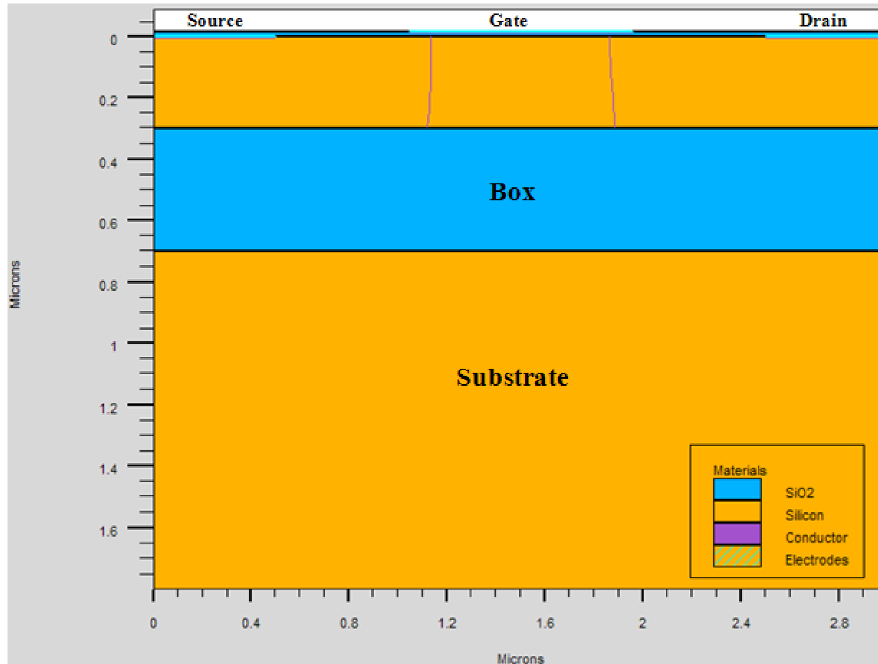
V. Simulation Results and Discussion

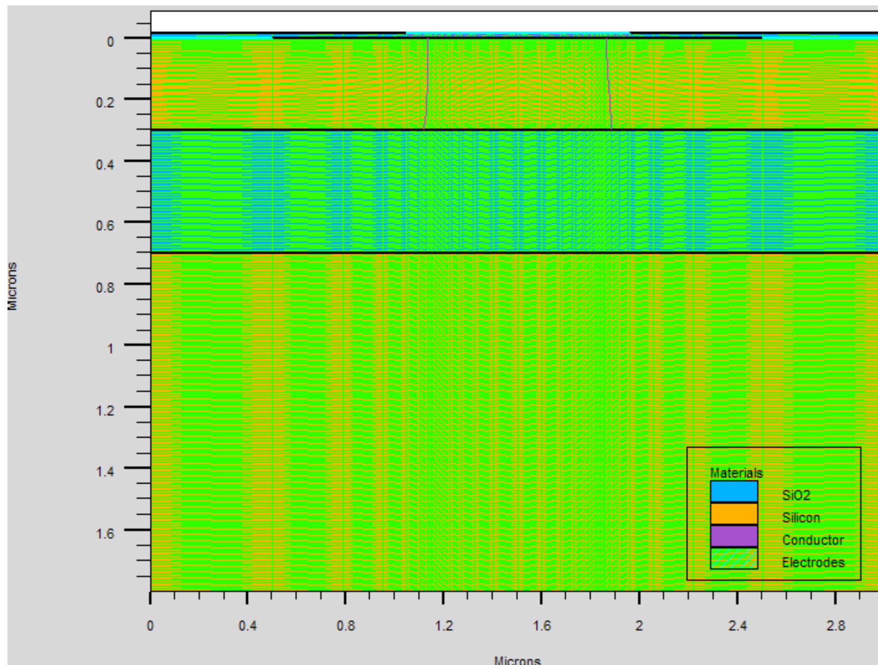
Fig. 5 illustrates the output characteristics I_{DS}-$V_{DS}$with V_{GS} constant, channel length L=1μ m and for gate oxide thickness T_{ox}=0.017 μm.

The "kink" effect is defined as a sudden increase in drain current for a certain drain voltage value, resulting in an increase in the drain conductance g_d and compression of the transconductance g_m, thus degrading the performance of the effect transistors of field and results from the mechanism of impact ionization and the effects of traps.

Fig. 6 illustrates I_{DS}-V_{GS} characteristic of PDSOI n-MOSFET transistor where V_{DS}=0.1 V. We can notice that our transistor is busy starting from a threshold voltage of about 1V.



(a)



(b)

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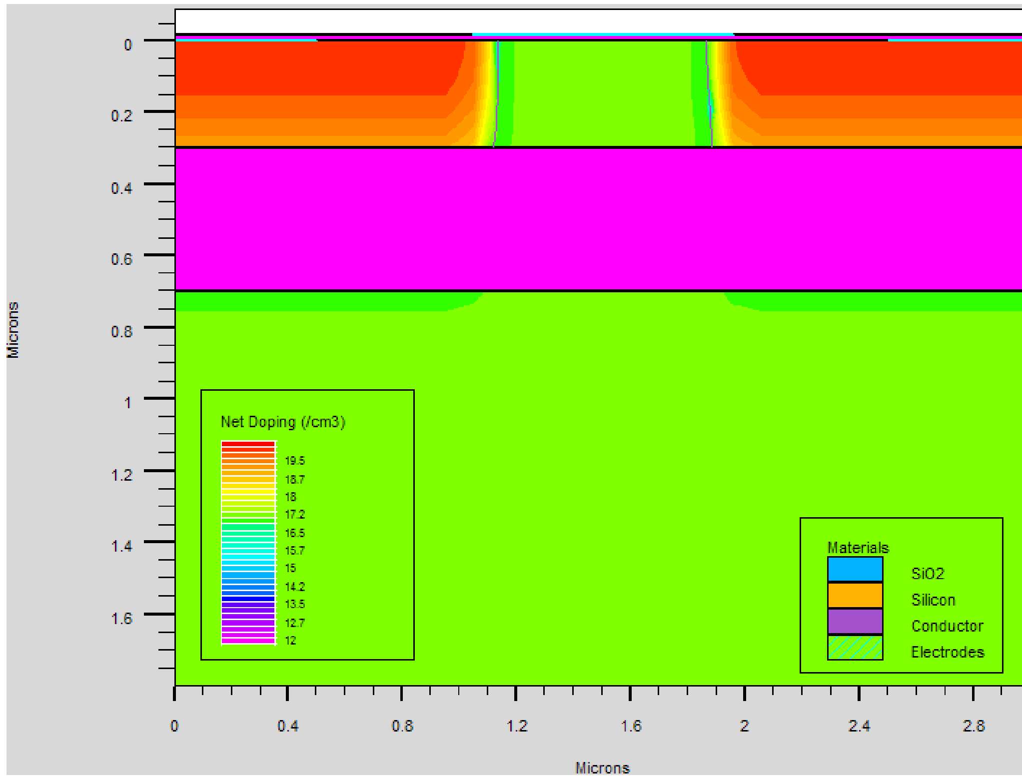

(c)

Fig. 4 (a) Schematic view of PDSOI n-MOSFET, (b) mesh view of PDSOI n-MOSFET, (c) doping profile view of PDSOI n-MOSFET

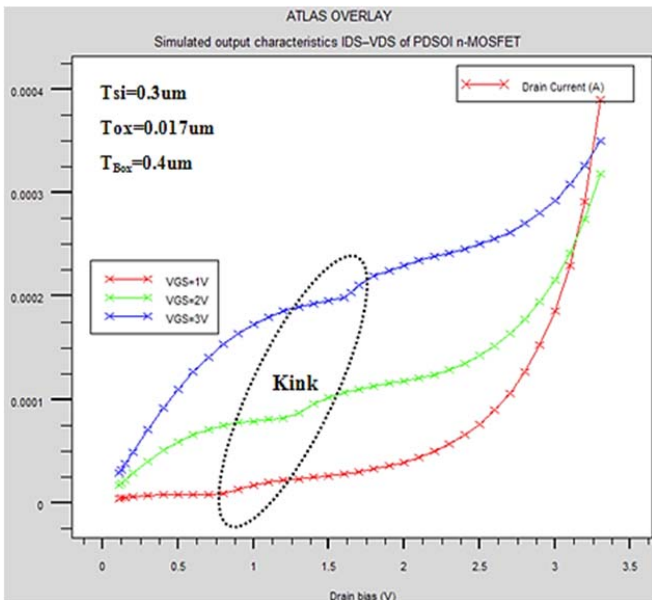

Fig. 5 Simulated output characteristics I_{DS}-V_{DS} of PDSOI n-MOSFET with channel length L=1 μm and for gate oxide thickness T_{ox}=0.017 μm

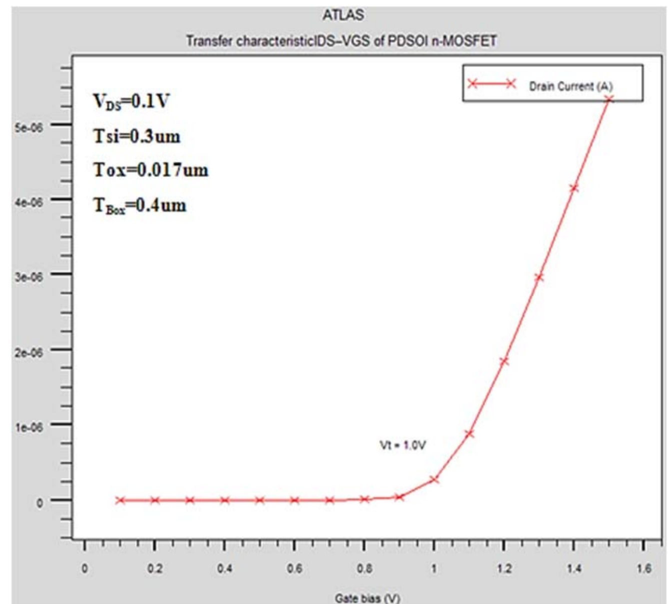

Fig. 6 Simulated transfer characteristics I_{DS}-V_{GS} of PDSOI n-MOSFET with channel length L=1 μm and for gate oxide thickness T_{ox}=0.017 μm

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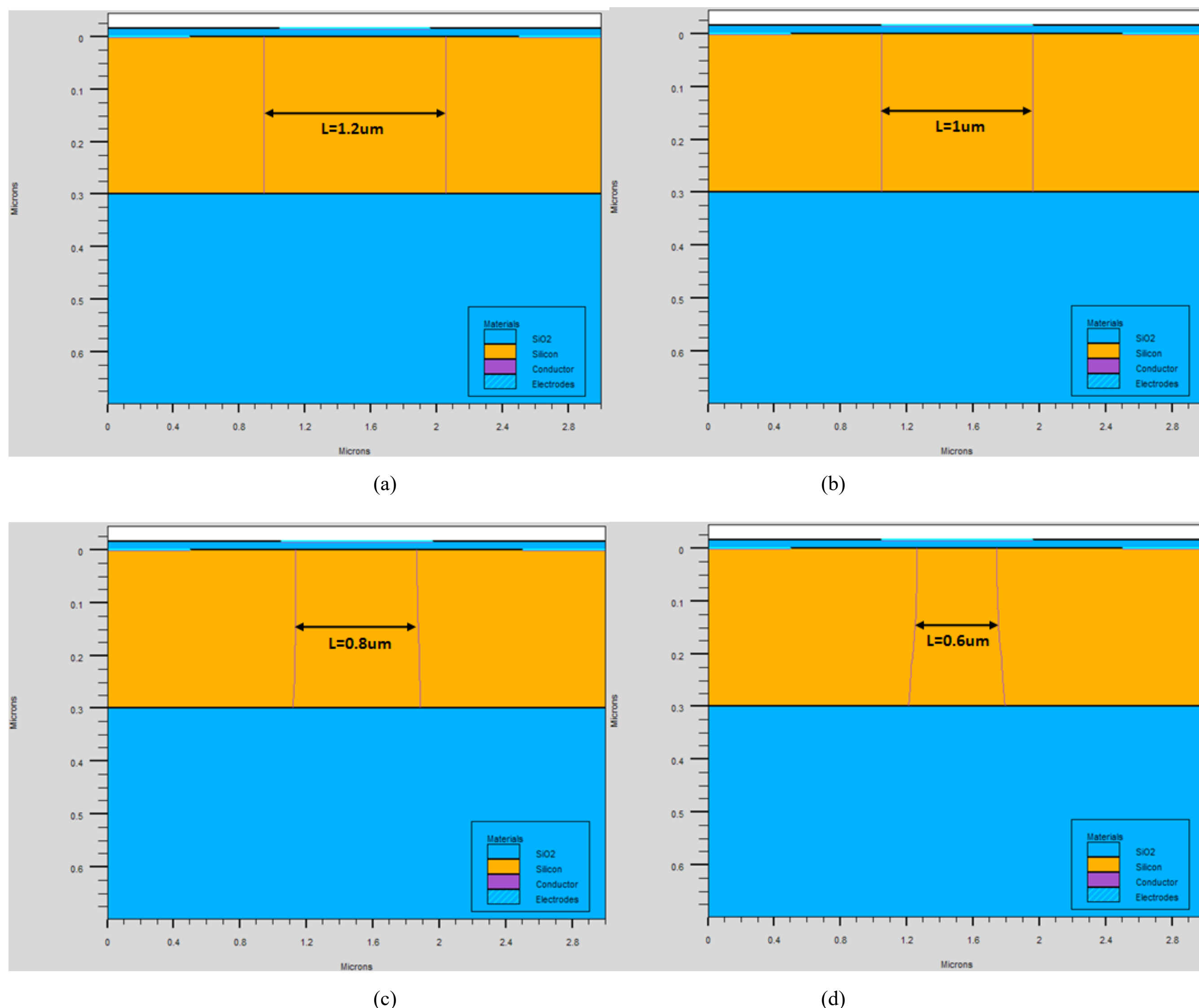

(a) (b)

(c) (d)

Fig. 7 Schematic view of PDSOI n-MOSFET with: (a) channel length L=1.2 µm, (b) channel length L=1 µm, (c) channel length L=0.8 µm, and (d) channel length L=0.6 µm

VI. The Variation Effect of Channel Length L with a Reduction in Gate Oxide Thickness T_{ox} on the Characteristics of the PDSOI n- MOSFET Transistor

Improvement of the performances of the transistors MOS always requires the reduction in its dimensions. However, by reducing the length channel L, it is possible to modify also certain technological parameters such as the gate oxide thickness Tox. This simulation requires the modification of our component geometry and particularly the effective length channel L (Fig. 7).

The reduction of the channel length L with a reduction in gate oxide thickness Tox is a better technique that allows to eliminate some undesirable effects related to the SOI technology such as the Kink effect which also makes it possible to amplify the I_{DS} (Fig. 8).

We notice that for T_{ox} = 0.005 µm, the current I_{DS} is about 10 times larger than the current I_{DS} obtained for T_{ox} = 0.017 µm, that is well confirmed on the simulation results of Fig. 8.

VI. Conclusion

From these simulations results of the structure of the PD SOI n-MOSFET transistor and the variation effect of the channel length parameter with a reduction in gate oxide thickness T_{ox} on the output characteristics (I_{DS}-V_{DS}) and transfer concerning characteristics (I_{DS}-V_{GS}) obtained by using Atlas-SILVACO tool, we could note that the reduction of length channel L with modifying also certain technological parameters such as the gate oxide thickness T_{ox} allows to make improvements on the transistor characteristics.

The reduction of the channel length L with a reduction in gate oxide thickness T_{ox} is the technique that has allowed us to eliminate the kink effect and amplify the current I_{DS}.

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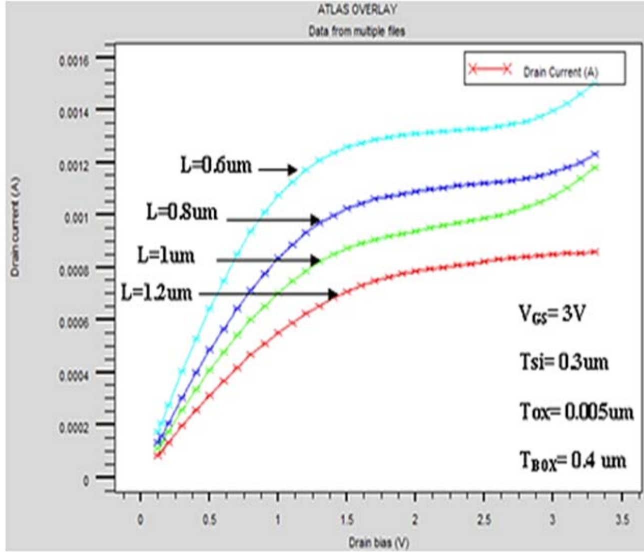

Fig. 8 Simulated output characteristics I_{DS}–V_{DS} of PDSOI n-MOSFET with channel length L=1.2 µm, L=1 µm, L=0.8 µm, L=0.6 µm and gate oxide thickness T_{ox}=0.005 µm

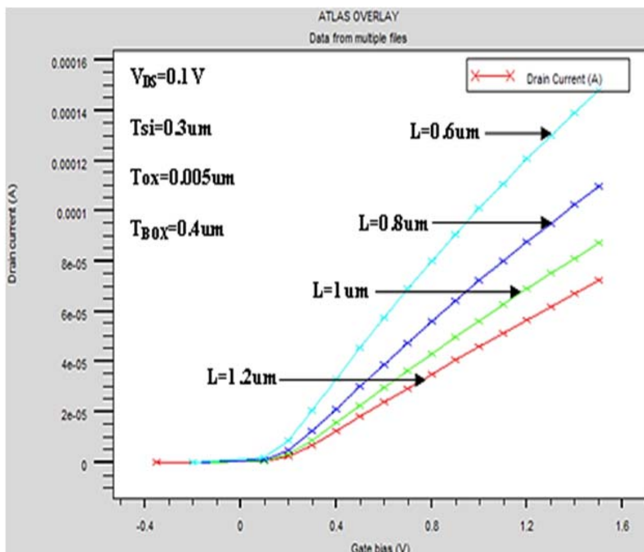

Fig. 9 Simulated transfer characteristic I_{DS}–V_{GS} of PDSOI n-MOSFET with channel length L=1.2 µm, L=1 µm, L=0.8 µm, L=0.6 µm and gate oxide thickness T_{ox}=0.005 µm

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