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A Case Study of Limited Dynamic Voltage Frequency Scaling in Low-Power Processors

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***Abstract*—**Power management techniques are necessary to save power in the microprocessor. By changing the frequency and/or operating voltage of processor, DVFS can control power consumption. In this paper, we perform a case study to find optimal power state transition for DVFS. We propose the equation to find the optimal ratio between executions of states while taking into account the deadline of processing time and the power state transition delay overhead. The experiment is performed on the Cortex-M4 processor, and average 6.5% power saving is observed when DVFS is applied under the deadline condition.

***Keywords*—**Deadline, Dynamic Voltage Frequency Scaling, Power State Transition.

I. Introduction

LARGE power consumption is deadly on portable devices since battery life is limited. Therefore, many power management techniques exist. DPS and DVFS are commonly power management techniques. DPS mechanism is a choice the mode between Idle and power saving. Power mode can be switched according to the processor and the peripherals whether they use or not. DVFS is a technique to change the frequency and/or operation voltage of processors [1].

DVFS techniques are not commonly available in low power processors. When a developer implements DVFS, they need to consider about the trade-off between additional transition overhead and overall power saving, especially if DVFS system is worked in low power processor. Also, power consumption cannot reduce continuously because the deadline is also an important part of work. In this paper, we perform a case study to find optimal power state transition for DVFS in low power processors and propose execution ratio equation. The paper focuses on the relationship between transition overhead and power consumption under the condition of keeping the deadline and establishes the value of using DVFS in low power processors [3].

The rest of the paper is organized as follows: In Section II, related works for power management techniques which are DPS and DVFS are described. Section III introduces scenario of DVFS case studies and proposes the equation for deadline compliance. The ratio of states which are related to deadline and power saving under the deadline condition is reported, and energy consumption with transition overhead is introduced in Section IV. Conclusions are given in Section V.

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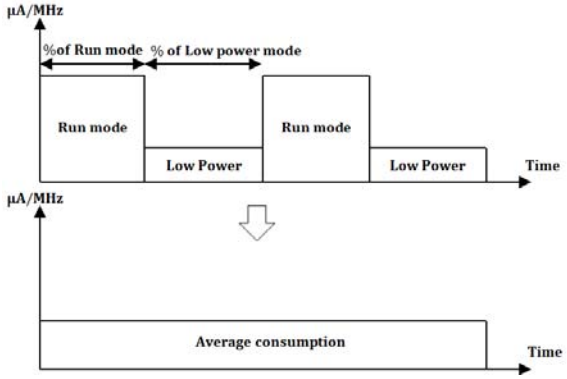

Fig. 1 Power mode switch

II. Related Works

Power management techniques are necessary for the microprocessor. Typically, there are two types of techniques which are static power management and active power management. In a real-time system, dynamic power is important in application processing. The rest of this section introduces dynamic power management technique's benefit and disadvantage.

A. PMS (Power Mode Switching)

Power mode switching reduces the overall average power consumption, as the device keeps low-power mode as much as they can. Fig. 1 from [4] describes power mode switching can reduce overall average consumption. Low power processors commonly feature four low power modes which are standby, sleep, stop, battery. These modes can be switched with the run mode or each other depending on CPU status whether it needs to keep fully active mode or not. Equation (1) introduces calculating total power consumption when power mode switching techniques are applied [4]. Values adding power consumption of four modes are divided by total time.

$$\text{Total Power} = I_{average} * V, with:$$
$$I_{average} = (I_{Run} * Time_{Run} + I_{Standby} * Time_{Standby} + I_{Sleep} * Time_{Sleep} + I_{Stop} * Time_{Stop})/Totaltime \quad (1)$$

Power mode switching is a good way to reduce power consumption. However, it has problems such as wake-up cost and miss-prediction.

B. DVFS (Dynamic Voltage Frequency Scaling)

DVFS is a generalized technique for dynamic power management. DVFS is used for reducing CPU power

consumption, as CPU power consumption has a big portion of total power consumption in a processor. CPU is composed of CMOS semiconductor and (2) is CMOS energy consumption:

$$P_{dyn} = N_{sw} C_L V_{dd}^2 f \quad (2)$$

In (2), N_{sw} is the switching activity, C_L is CMOS circuit output load capacitance, V_{dd} is supply voltage, and f is the operating clock frequency [2]. Following equation is emerged from (2):

$$\text{Power consumption in CPU E} \propto V^2 and\ f \quad (3)$$

Power consumption is proportional to frequency and the square of the supply voltage. Therefore, voltage and frequency scaling can influence on power consumption. A technique which is used in the dynamic process is called Dynamic voltage-frequency scaling. However, the disadvantage of DVFS is transition overhead can be generated when voltage and frequency are scaling.

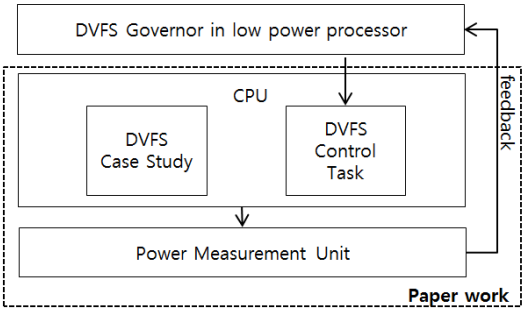

Fig. 2 DVFS System

III. Implementation of DVFS Case Studies Method

DVFS is not commonly used is low power processor, although DVFS is common power management technique. An overall system for implementation of DVFS case studies method is as in Fig. 2. Cases are composed of three elements such as deadline, power saving, and transition overhead. Compliance of deadline is an important element in the overall process schedule. We propose the equation to find the optimal ratio between executions of states to comply with the deadline. Case studies method is implemented in firmware for low power processors.

DVFS control task is a part for scaling dynamic voltage and frequency. For doing it, operating performance points (OPP) need to be fixed. Operating voltage and frequency is dependent on target processors, and common low power processors support two levels of voltage and regular frequency. Table I introduces operating performance points for this paper DVFS algorithm. Scale1 Voltage is 1.2V, and Scale2 is lower than 1.2V [5]. This system is applied in target board, and power consumption measurement is progressed. Feedback of case study information is reflected in DVFS governor from the information measured in power measurement unit as Fig. 2.

In Fig. 3, when the process works in state 1, average power consumption is larger than average power consumption when the process works in other states. The fact that state 3, 4 are a better choice for power saving is clear. However, in this states, total execution time is longer than state 1, 2 and process may not comply with a deadline. Therefore, finding optimal execution ratio between states is important elements. Methodology to find optimal execution is execution ratio equation (4)

$$t_{ps}x + t_{ts}(1-x) + t_{ad} < t_{deadline}\ (0 \le x \le 1) \quad (4)$$

In (4), t_{ps} is present state execution time, t_{ts} is execution time for target state, t_{ad} is average time from overhead delay and x is execution ratio of present state. During dynamic voltage and frequency scaling, transition overheads such as delay and power consumption are generated in DVFS Algorithm. This element has influence on total execution time. Therefore, transition overhead delay time information needs to be reflected with execution ratio equation. Time information is given a data set and already knows from power measurement unit. Transition number is assumed once in (4). This result makes process comply with deadline and DVFS control unit is optimized by this feedback.

IV. Experiments

In this paper, DVFS system is tested on low power processor (Cortex-M4) and target devices STM32F4 series. Power measurement environment is composed of the power supply, multimeter, current probe and oscilloscope as Fig. 4. Case studies are divided into three parts. Benchmark programs are FFT and Bit count.

TABLE I
DVFS Operating Performance Point States

State	Voltage	Frequency [a]
State1	Scale1	200MHz
State2	Scale1	168MHz
State3	Scale2	84MHz
State4	Scale2	42MHz

First experiment part is proving execution ratio equation (4) under the condition of the deadline. Works are calculating x value using (4) and proving this result by using power measurement unit. In this part, the control variable is a limited deadline and time variables are measured in power measurement unit. Table IV shows delay time, and this average value uses for t_{ad}. In FFT benchmark, deadline is 4ms and x value needs to be over 0.496 when state is changed from 1 to 3. In Table II, when execution ratio is 5 to 5, execution time is 3.869ms and it observes deadline. However, in the ratio of 3 to 7, x value is lower than 4.96 and execution time is 4.511ms. In Bit count benchmark, deadline is 2ms and x value needs to be over 0.508 when state is changed from 1 to 3. When execution ratio is 6 to 4, execution time is 1.873ms and it observes deadline. Tables II-V show the result when (4) is applied in DVFS.

Second part establishes implementation of DVFS has an

advantage or not in low power processor under the condition of the deadline. Table III shows average 6.5% power saving exists when the process complies with a deadline in FFT benchmark. In addition, when optimal state change option is chosen, maximum power saving is about 10.5%. In Table VI, average 3.7% power saving is excited in Bit count.

In the third part, experiment for transition overhead is progressed. When states are changed, transition overheads such as execution time delay and energy consumption are generated.

In Table IV, result shows execution time delay and total energy consumption in the whole state changes the situation. From this results, execution time delay is average 0.269ms, and average energy consumption is 10.686 $\mu\mathcal{J}$. In Table VII, execution time delay is average 0.273ms and average energy consumption is 10.456 $\mu\mathcal{J}$. It shows transition overhead affects whole program execution.

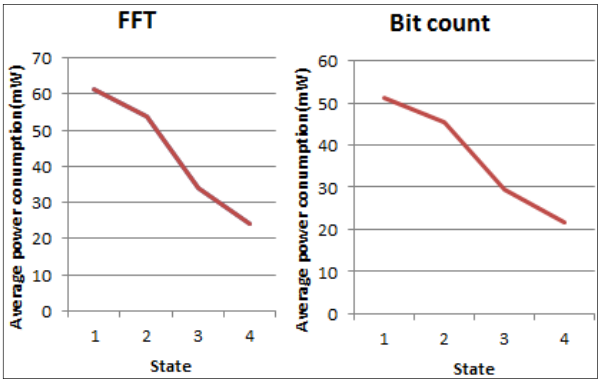

Fig. 3 Average power consumption in benchmark

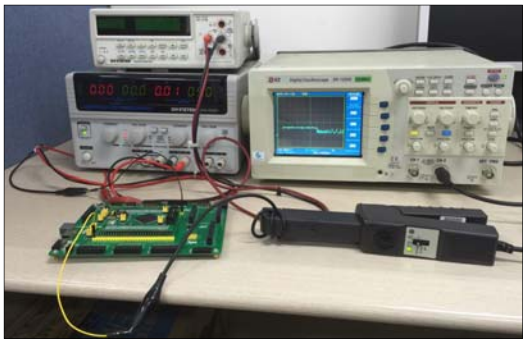

Fig. 4 Power measurement environment

TABLE II
DEADLINE COMPLIANCE ACCORDING TO RATIO OF STATES IN FFT

State Change	Ratio between states	Execution time (mS)	Deadline Compliance
1->3	5:5	3.869	O
	3:7	4.391	X
1->4	9:1	3.395	O
	7:3	5.217	X
2->3	5:5	3.913	O
	7:3	4.782	X
2->4	8:2	3.478	O
	7:3	5.652	X

TABLE III
POWER CONSUMPTION WITH DVFS OR WITHOUT DVFS IN FFT

State Change	DVFS ON	Average Power Consumption ($m\mathcal{W}$)	Power Savings
1	-	28.45	-
2	-	29.865	-
3	-	23.614	-
4	-	23.912	-
1->3	o	26.032	8.49%
1->4	o	27.542	3.19%
2->3	o	26.739	10.46%
2->4	o	28.674	3.98%

TABLE IV
DELAY AND TOTAL ENERGY CONSUMPTION DURING TRANSITION IN FFT

State Change	Delay (mS)	Total Energy Consumption ($\mu\mathcal{J}$)
1->2	0.12	6.721
1->3	0.28	12.099
1->4	0.3	11.634
2->1	0.08	4.48
2->3	0.3	12.421
2->4	0.3	11.139
3->1	0.45	19.445
3->2	0.35	14.492
3->4	0.2	5.462
4->1	0.45	17.451
4->2	0.2	7.426
4->3	0.2	5.462

TABLE V
DEADLINE COMPLIANCE ACCORDING TO RATIO OF STATES IN BIT COUNT

State Change	Ratio between states	Execution time (mS)	Deadline Compliance
1->3	6:4	1.873	O
	5:5	2.012	X
1->4	9:1	1.712	O
	8:2	2.108	X
2->3	7:3	1.977	O
	6:4	2.082	X
2->4	9:1	1.983	O
	8:2	2.386	X

TABLE VI
POWER CONSUMPTION WITH DVFS OR WITHOUT DVFS IN BIT COUNT

State Change	DVFS ON	Average Power Consumption ($m\mathcal{W}$)	Power Savings
1	-	23.74058	-
2	-	25.09697	-
3	-	21.49326	-
4	-	21.63	-
1->3	o	22.615	4.8%
1->4	o	23.318	1.81%
2->3	o	23.65	5.73%
2->4	o	24.398	2.79%

V. CONCLUSION

Power consumption is related to heat generation and battery lifetime. We perform a case study to find optimal power state transition for DVFS and propose equation to find optimal execution ratio between states for deadline compliance.

Experiments prove this equation, and it is feedback for DVFS Governor to optimize the algorithm. This result makes process comply with deadline and DVFS control unit is optimized by this feedback. Also, average 6.5% power saving exists when DVFS is applied in task process from the experiments. The control variable is a deadline in this experiment. When an optimal state change is chosen, maximum power saving is about 10.5%. From this result, DVFS has a good influence on reducing power consumption in low power processor.

TABLE VII
DELAY AND TOTAL ENERGY CONSUMPTION DURING TRANSITION IN BIT COUNT

State Change	Delay (mS)	Total Energy Consumption ($M\mathcal{J}$)
1->2	0.14	6.769
1->3	0.3	14.505
1->4	0.35	12.76275
2->1	0.1	4.835
2->3	0.3	11.2545
2->4	0.25	8.37875
3->1	0.42	20.307
3->2	0.36	13.5054
3->4	0.25	6.4075
4->1	0.4	14.586
4->2	0.21	7.03815
4->3	0.2	5.126

In conclusion, this paper proves DVFS has power saving effect in low power processors. In DVFS, task deadline and transition overhead are important. Execution ratio equation which we propose contributes to keep task deadline including transition overhead element.

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