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Inverter Based Gain-Boosting Fully Differential CMOS Amplifier

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Abstract**—**This work presents a fully differential CMOS amplifier consisting of two self-biased gain boosted inverter stages, that provides an alternative to the power hungry operational amplifier. The self-biasing avoids the use of external biasing circuitry, thus reduces the die area, design efforts, and power consumption. In the present work, regulated cascode technique has been employed for gain boosting. The Miller compensation is also applied to enhance the phase margin. The circuit has been designed and simulated in 1.8 V 0.18 µm CMOS technology. The simulation results show a high DC gain of 100.7 dB, Unity-Gain Bandwidth of 107.8 MHz, and Phase Margin of 66.7° with a power dissipation of 286 µW and makes it suitable candidate for the high resolution pipelined ADCs.

Keywords**—**CMOS amplifier, gain boosting, inverter-based amplifier, self-biased inverter.

I. Introduction

OVER the years, there has been an increase in the complexity of the chips being designed [1]. This has resulted in an increased importance of the efficient implementation of both analog and digital functions using CMOS technology. Operational amplifiers (op-amps) are an important building block in most of these analog and mixed circuit implementations. It is used in many circuits, which includes output buffers, sample and hold circuits and analog-to-digital converter or ADC [2]. Because of being crucial to the circuit operation, the performance of an op-amp significantly influences the system's performance.

Op-amp is a very important component in most analog and mixed signal systems. Therefore, it is very crucial that it matches the requirements of the current trends offered by the industry. In the conventional electronics market, low-voltage operation along with low-power dissipation is an important parameter for all devices. Op-amps are no exception to this. It is important that they also evolve to be compatible in this low-voltage low-power environment. This is the motivation behind the research carried out.

A two-stage fully differential op-amp design has been proposed. Cascading is used to avoid the output swing reduction that results in the case of cascoding. This is important because, in low-voltage operation, the already small swing cannot be further compromised. The cascaded connection of the two stages also ensures an improvement in the gain offered by the device.

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The presented implementation is designed to use an inverter-based first stage. This increases the transconductance of the stage-I, thereby improving the gain offered by the stage. In addition to this, the final gain offered by the circuit has been further enhanced by making use of a gain-boosting circuit. Therefore, the proposed design is the future of op-amp technology. It improves the gain of the device while maintaining its viability as an efficient low voltage component that can be used in the present day's electronics.

II. Proposed Design

A. Self-Biasing Concept

Self-biasing technique not only reduces the area and power overheads but also reduces the sensitivity of the set biasing point to the process variations [3]. As the name suggests, self-biasing does not use any additional devices or biasing voltage sources for biasing purposes. Instead the scheme uses the power rails (V_{DD} and V_{SS}) only. This is the reason behind the elimination of the power and area overheads. Fig. 1 shows the self-biasing concept applied to a fully differential CMOS inverter.

Being fully-complementary circuit has a DC differential mode gain which approximately doubles the gain offered by any other conventional amplifier. The differential mode gain (A_d) is formulated as [9]

$$A_d = \frac{g_{m1}+g_{m2}}{g_o} \quad (1)$$

where g_{m1} is the transconductance of device $M_{1A\text{-}B}$, and g_{m2} is the transconductance of device $M_{2A\text{-}B}$. The amplifier's output conductance is denoted by g_o. Transistors M3 and M4 in Fig. 1 operate in the linear region. Since these two transistors define the two voltages, V_H and V_L and these voltages define the output swing of the amplifier. By setting the value of these voltages close to the supply rails, the output swing of the amplifier can be made approximately equal to the difference between the supply rail voltages.

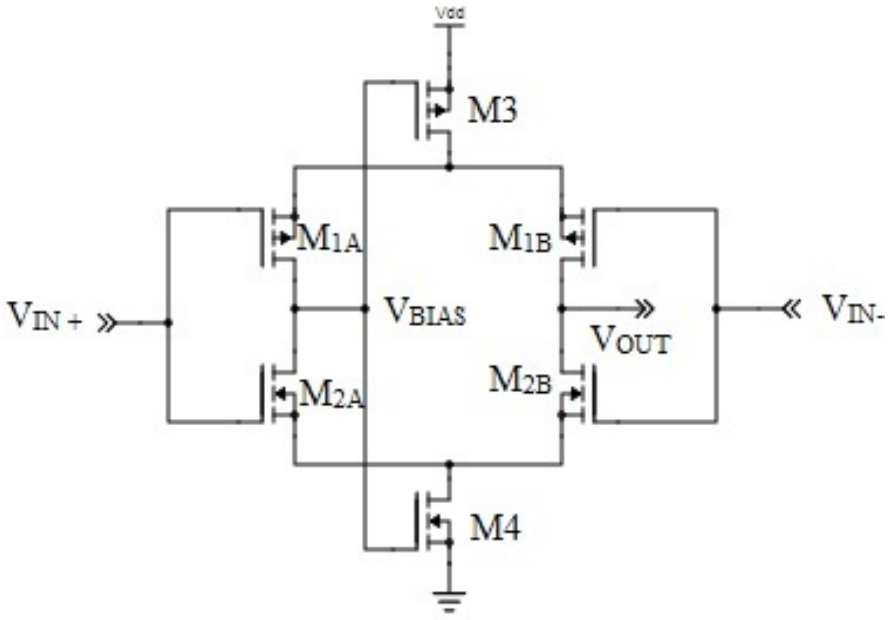


Fig. 1 Self-biased inverter

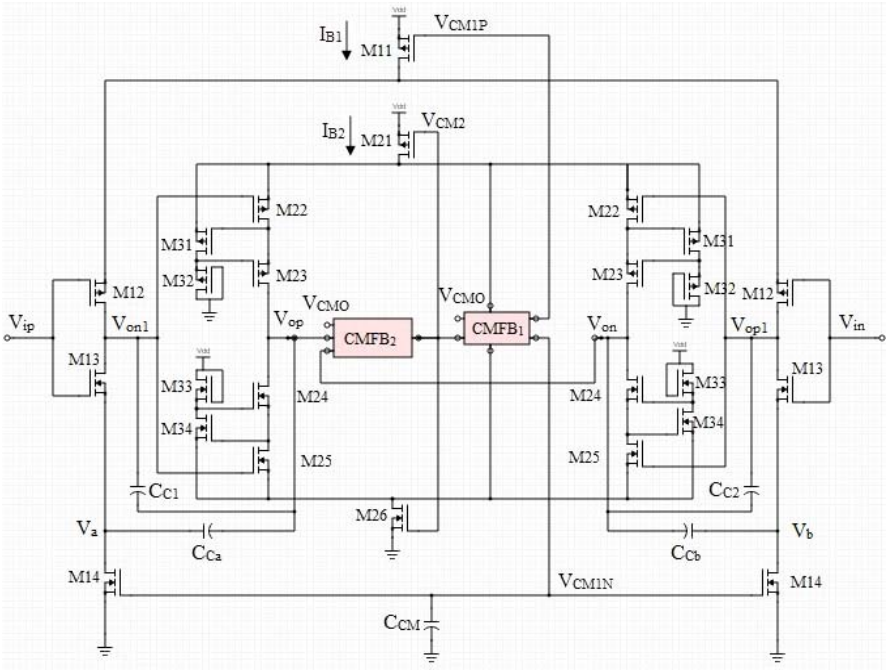


Fig. 2 Proposed gain boosting inverter based op-amp

B. Proposed Circuit

The proposed circuit is a modification to two-stage fully-differential CMOS amplifier that uses inverters with self-biasing concept [4]. The proposed circuit comprises of two self-biased inverter stages, where gain boosting is applied to output stage inverter as shown in Fig. 2. It can be seen that two inverter stages having the similar topology are cascaded. The current sources, M11 and M14, are connected to input-stage inverter pair (M12-M13). These current sources provide the biasing and common-mode (CM) voltage to the input stage. The output stage of the proposed circuit consists of inverter pair (M22-M23) and transistors (M31-M32) which are connected to current sources, M21 and M26, providing biasing voltage and CM output level to the output stage.

Considering the input stage first, R_{op1} and R_{on1} represent the output resistances seen at the output node of the input stage.

The gain A_{v1} of the first stage is given by:

$$A_{v1} = g_{m1} \times (R_{op1} \,||\, R_{on1}) \tag{2}$$

where $g_{m1} = g_{m12} + g_{m13}$, $R_{op1} = r_{o12}$ and $R_{on1} = r_{o13}$.

Now, considering the output stage, the transistors M31-M32 represent a common source amplifier with diode connected pmos load having gain A_{vp}. The transistors M33-M34 represents a common source amplifier with diode connected nmos load having gain A_{vn}. Transistor pairs M31-M32 and M33-M34 act as gain boosting transistors for M22-M23 and M24-M25, respectively. The resistances R_{op2} and R_{on2} represents the output resistances seen at the output node of the output stage and is shown in Fig. 3.

The gain A_{v2} of the second stage is given by:

$$A_{v2} = g_{m2} \times (R_{op2} \,||\, R_{on2}) \tag{3}$$

where, $g_{m2} = g_{m22} + g_{m25}$, $R_{op2} = A_{vp} g_{m23} r_{o23} r_{o22}$ and $R_{on2} = A_{vn} g_{m24} r_{o24} r_{o25}$. Thus, the overall gain is given by:

$$A_v = A_{v1} \times A_{v2} \tag{4}$$

$$A_v = (g_{m12} + g_{m13})(g_{m22} + g_{m25})(r_{o12} \,||\, r_{o13})(A_{vp} g_{m23} r_{o23} r_{o22} \,||\, A_{vn} g_{m24} r_{o24} r_{o25}) \tag{5}$$

The two CM feedback blocks used in Fig. 2 are continuous in nature and used to bias the amplifiers [4], [5]. These continuous-time CM feedback circuits are used to bias the circuit and to provide the CM control voltages to input and output stages. The CM feedback circuit $CMFB_1$ in Fig. 2 compares V_{CM2} with a constant voltage V_{CM0} and generates the voltages V_{CM1P} and V_{CM1N} to bias the input stage. The voltages generated by $CMFB_1$ and $CMFB_2$ are self-biased voltages [4].

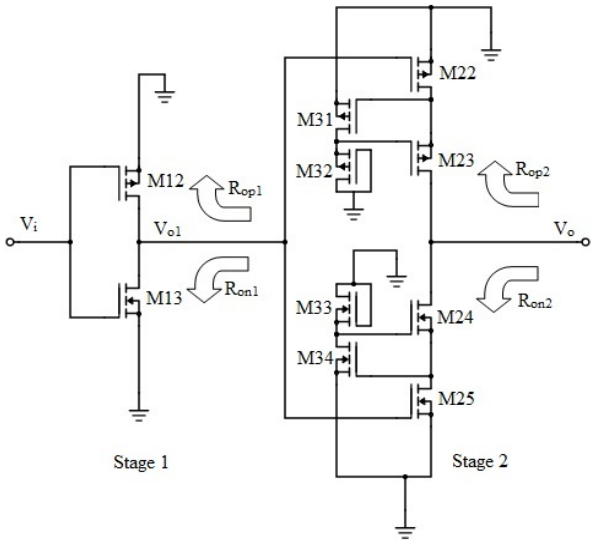
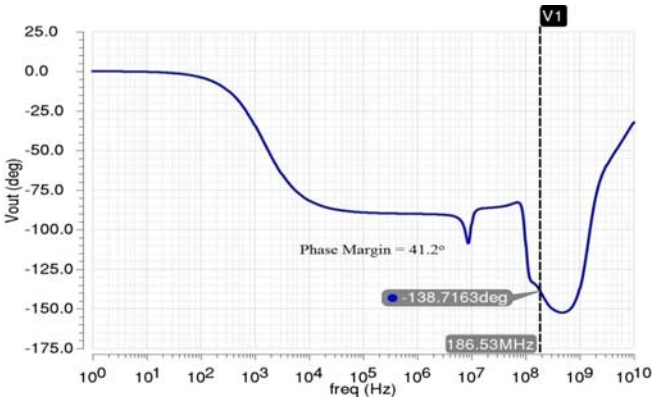


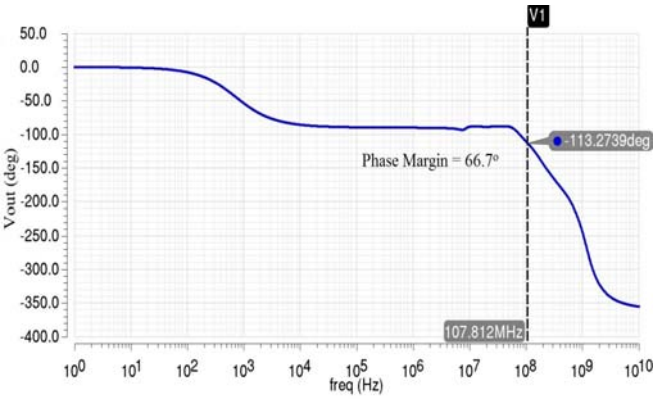
Fig. 3 Output stage of proposed gain boosting inverter based op-amp

There are two high impedance nodes: one at nodes Von1, Vop1 and another at nodes Vop, Von. To remove the effect of unwanted poles and zeroes, the Miller compensation is applied by connecting the compensation capacitor, C_{C1} between the nodes V_{on1} (i.e. output of first stage) and V_{op} (i.e. the output of second stage) and between V_{op} and V_a by using C_{Ca} in the circuit. The addition of compensation capacitor (C_{C1}) firstly increases the effective capacitance shunting R_1 and moves the dominant pole (p_1) towards the origin. Secondly, it moves the second pole, (p_2) away from the origin because of decrease in the output resistance. This technique increases the phase margin of the op-amp.

Fig. 4 shows the increase in the phase margin from 41.2° to 66.7° after applying the frequency compensation as shown in Fig. 2.



(a)



(b)

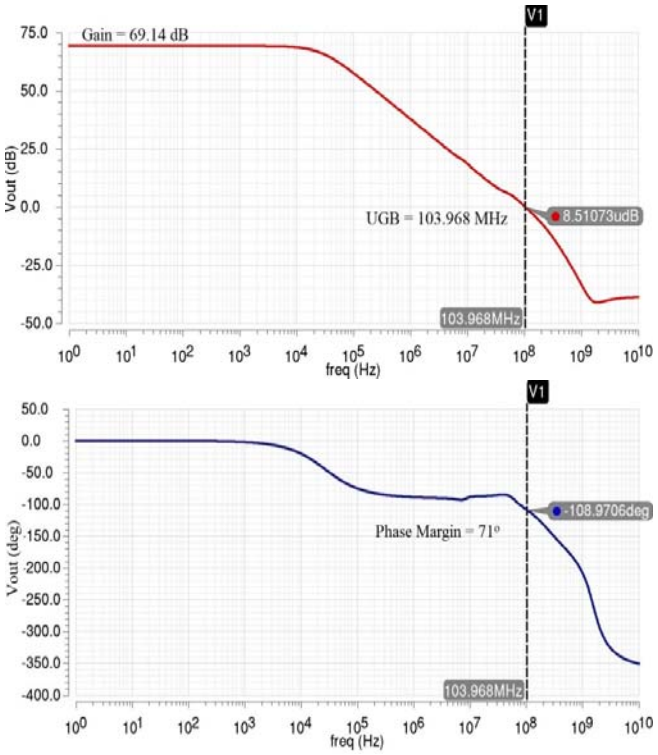
Fig. 4 Phase margin response of gain-boosting amplifier (a) without compensation capacitor (b) with compensation capacitor

III. Results

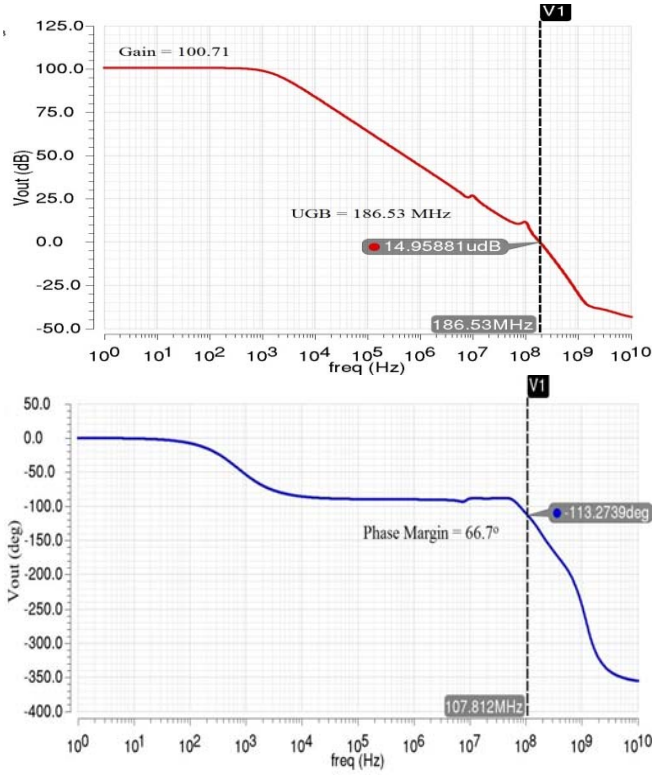
AC Response: The frequency response of two-stage fully-differential inverter based op-amp is shown in Fig. 5. The gain of the op-amp is limited to 69.14 dB which has been increased by applying a gain boosting technique. The bode plot and phase shift plot of the proposed circuit in Fig. 5 (b) shows a gain of 100.71 dB and Unity-Gain Bandwidth (of 107.812 MHz with the phase-margin of 66.7°.

Transient Response: The test bench for the transient response of the proposed amplifier is shown in Fig. 6, and the respective results after applying a step signal are shown in Fig. 7. The slew rate found by calculating the slope of rising edge of the output waveform comes to be 30 V/μs. Figs. 7 (a) and (b) shows the step response when the large signal (0.6 Vp-p) and the small signal (0.1 Vp-p) are applied to the input, respectively.

The slew rate observed is 32.6 V/μs for the large signal and 26.57 V/μs for the small signal.



(a)



(b)

Fig. 5 Gain and phase response (a) without gain-boosting (b) with gain-boosting

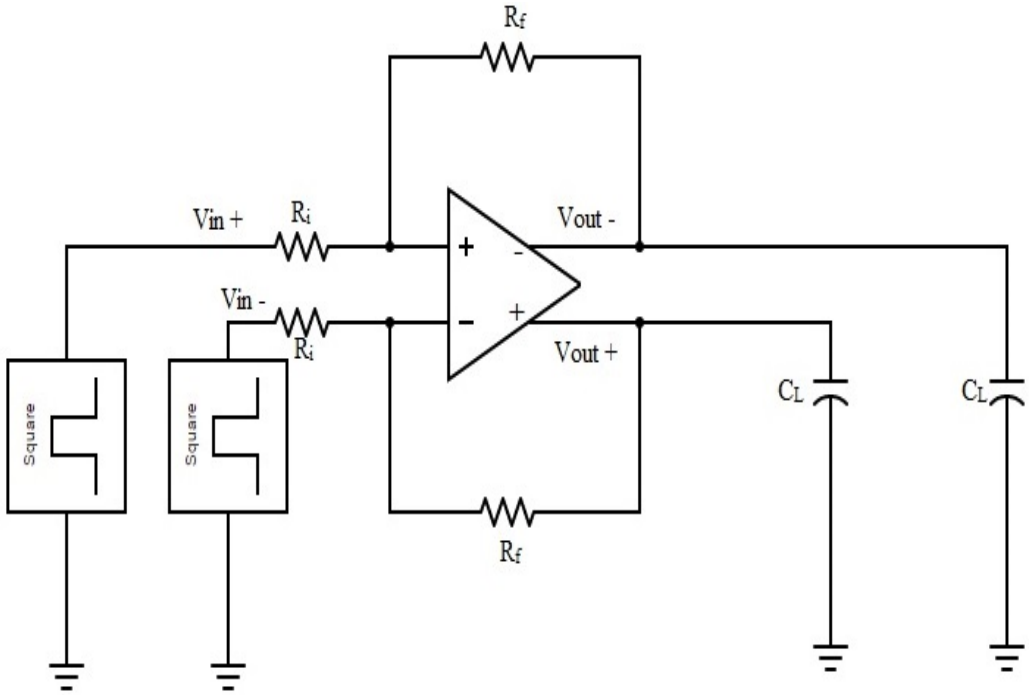
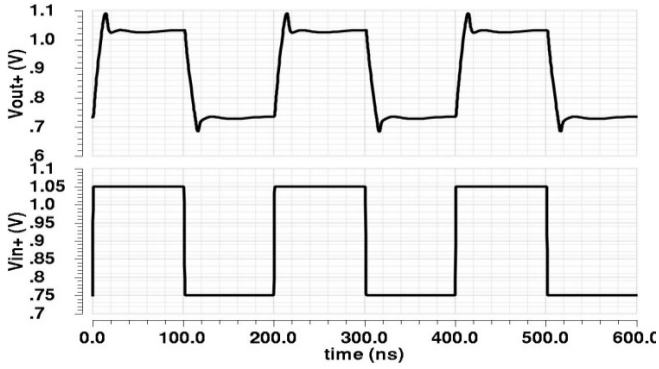
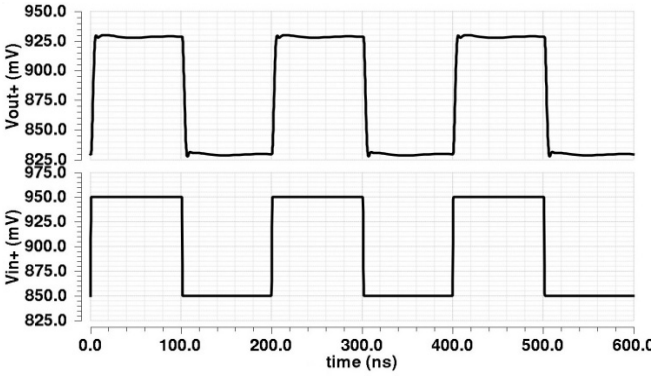


Fig. 6 Test bench for transient response



(a)



(b)

Fig. 7 Step responses (a) large signal (b) small signal

TABLE I
COMPARISON OF KEY PERFORMANCE PARAMETERS OF THE OM-AMP

Architecture	[6] Conventional Fully Differential Two Stage	[7] Recyclic Folded Cascode	[8] Self-Cascode Structure	[4] Self-Biased Inverter-Based	**This Work** **Self-Biased Inverter-Based**
Tech (μm)	0.18	0.18	0.18	0.13	**0.18**
Power Supply (V)	1.8	1.8	1.8	1.2	**1.8**
Open Loop Gain (dB)	74	60.9	96	71	**100.71**
UGB (MHz)	160	134.2	146	35	**107.8**
Power Dissipation (mW)	0.362	1.44	0.720	0.110	**0.286**
SR (V/μs)	26.7	94.1	N/A	19.5	**32.6**
Input Common-Mode Range (Vp-p)	N/A	N/A	N/A	N/A	**1.03**
Output Common-Mode Range (Vp-p)	N/A	N/A	N/A	N/A	**1**
PM (°)	N/A	70.6	70	47	**67**
C_L (pF)	1.75	5.6	15	5	**4**

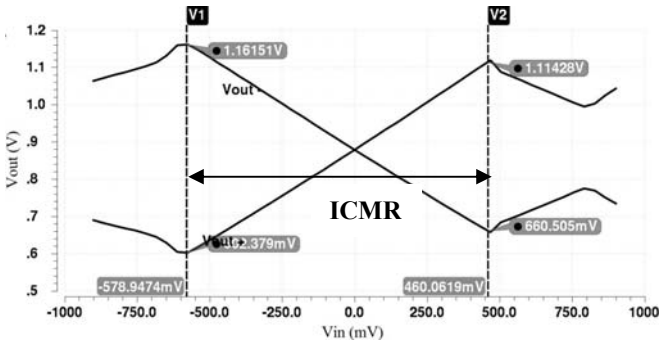


Fig. 8 Input CM range (ICMR)

Fig. 8 shows the input CM range equal to 1.03 Vp-p and output CM range equal to 1 Vp-p. Total power dissipation of the proposed gain boosting amplifier is 286 μW.

Performance Comparison: Table I presents a summary of key measured parameters, as well as, a performance comparison with various single stage and multistage amplifiers available in literature [4], [6]-[8].

IV. CONCLUSION

This work describes a low power two-stage gain-boosted fully differential CMOS amplifier for pipelined ADC. The amplifier uses self-biased inverter stages, thus avoiding any need of biasing circuitry. Different circuit analyses are carried out using Cadence Virtuoso Analog Design Environment in TSMC 180 nm CMOS technology. The proposed circuit shows an improved value of 100.71 dB for DC gain. UGB offered is 107.8 MHz. The improved Phase Margin of 67° results from the compensation applied in the circuit. Therefore, the proposed circuit is capable of offering low voltage, low power operation without compromising the other performance parameters. This makes it a viable and effective option to be used in high resolution pipelined ADC architecture.

ACKNOWLEDGMENT

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