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Single Event Transient Tolerance Analysis in 8051 Microprocessor Using Scan Chain

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***Abstract*—**As semi-conductor manufacturing technology evolves; the single event transient problem becomes more significant issue. Single event transient has a critical impact on both combinational and sequential logic circuits, so it is important to evaluate the soft error tolerance of the circuits at the design stage. In this paper, we present a soft error detecting simulation using scan chain. The simulation model generates a single event transient randomly in the circuit, and detects the soft error during the execution of the test patterns. We verified this model by inserting a scan chain in an 8051 microprocessor using 65 nm CMOS technology. While the test patterns generated by ATPG program are passing through the scan chain, we insert a single event transient and detect the number of soft errors per sub-module. The experiments show that the soft error rates per cell area of the SFR module is 277% larger than other modules.

***Keywords*—**Scan chain, single event transient, soft error, 8051 processor.

I. Introduction

IN the past few years, fabrication technology for integrated circuit (IC) has been evolved rapidly. As a result of downsizing the transistor feature size and operating voltage together, the processor's vulnerability to soft error has increased than past years [1], [2]. If there are no hardening design techniques in IC, the system *Soft Error Rate (SER)* will be proportional to the number of cells in the design [3]. For these reasons, the radiation tolerance testament and hardening techniques become important issues in upcoming IC products.

Previous studies have mainly focused on the radiation hardening techniques. Researchers have found different kinds of radiation hardening techniques, like scaling voltage [4] or radiation hardened by design (RHBD), such as guard ring layout technique [5].

In these days, circuits contain a scan chain to verify the functionality of the designs. By loading the test pattern to the scan chain, circuits can detect the error occurrence during operating process. Using this mechanism, we can verify the soft error tolerance of the design.

In this paper, we present a single event transient tolerance analysis using scan chain. We invoked a single event transient by forcing the transition of the random signal in a scan chain circuit while executing automatic generated test patterns. Then we calculated SER per cell areas and verified the module that needs radiation hardening. By using this mechanism, we can verify the single event transient tolerance of the chip before fabrication process without additional overheads.

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In Section , we briefly explain the definition of SET and scan chain, and single event transient simulation. Section explains the procedures of radiation tolerance testament and analyze experiment results, and finally we conclude results in Section .

II. Background

A. Single Event Transient

Single Event Transient (SET) is a temporary variation in the output voltage that is driven by a heavy ion flow through a device [6], [7]. Fig. 1 is a diagram of SET in AND gate. The output Q goes down to the '0' value when the SET occurs.

SET may propagate through the logic circuit leading to single event upsets, and cause the incorrect outputs [8]. Furthermore, as the fabrication technology evolved, SET from the circuit can be adopted as a normal signal. Machines, like spacecraft or radiation detector, which are used in the high radiation environment, can easily have SET problem, so it has been identified as the circuit's primary failure mechanism [9].

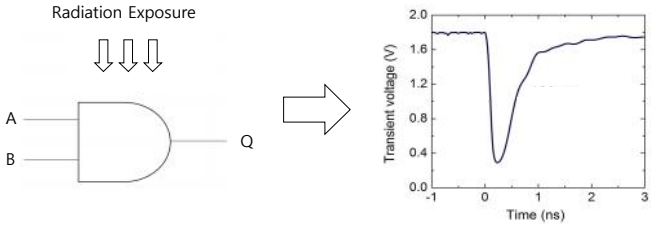

Fig. 1 SET in AND gate

B. Scan Chain

Scan chain is a common design-for-testability technique that observes all flip-flops in the chip to verify the circuit's functionality [10]. Scan chain consists of the scan flip-flops, which transport the test patterns to the right place. A typical scan chain is shown in Fig. 2. If SE (scan enable) signal is '0', the scan flip-flops act as normal flip-flops, so the circuit performs the normal operation. If SE signal is '1', the scan flip-flops load the test pattern, which is generated by automatic test pattern generator (ATPG), through scan in port.

Fig. 3 shows the wave of the test pattern operation. Test pattern operates in two modes. Shift mode checks whether the scan chain works normally, and capture mode tests the glue logic which is connected to the scan cells [11].

C. SET Simulation

In this paper, we present a SET simulation by using scan chain architecture. When a scan chain is in capture mode, we select a random signal in inner logic cell, and inverse the logic

value to simulate the SET environment.

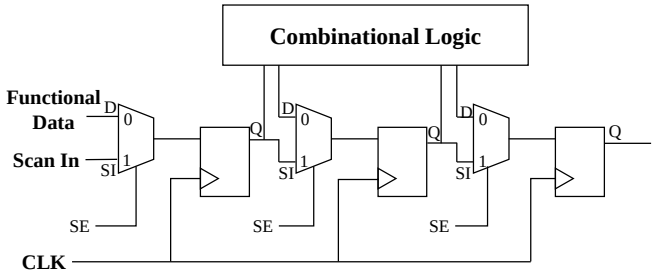

Fig. 2 SET in AND gate

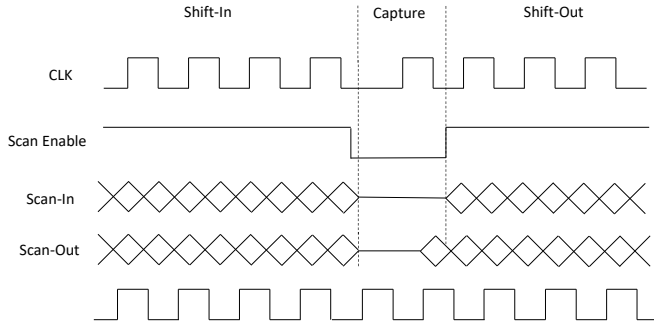

Fig. 3 Waveform of the test pattern operation

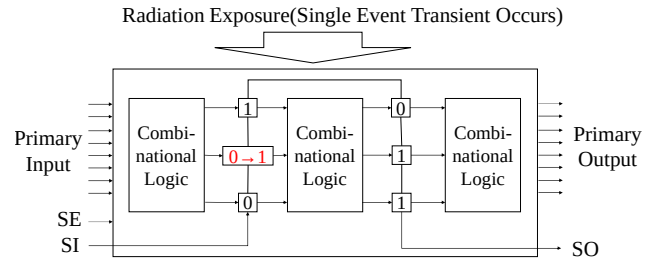

Fig. 4 SET simulation diagram

Fig, 4 shows a diagram of SET simulation. First, set the SE signal as '1' to enter the scan shift mode. Then, transport the test vector through the SI port. When the injection of the test vector is finished, set the SE signal as '0' to enter the scan capture mode. Inverting the signal, which is randomly selected, to invoke the SET. Finally, we can compare the SO signal and primary output value with the expected value. If the value is not equal, report the scan cell number which means the soft error occurred flip-flop. In this approach, functions of combinational logic cells and sequential elements can be accessed by the scan structure so that the off-chip monitor evaluates soft error immunity of entire IC.

D.8051 Microprocessor

For implementing the SET simulation, we used 8051 microprocessor core for testing circuit. The design shares the 8-bit data and address bus line and consists of 8 modules as in Fig. 5. special function register (SFR) is a register set that controls the special registers, like timer, UART, and I/O Ports. Memory Interface module controls the access of internal and external memories.

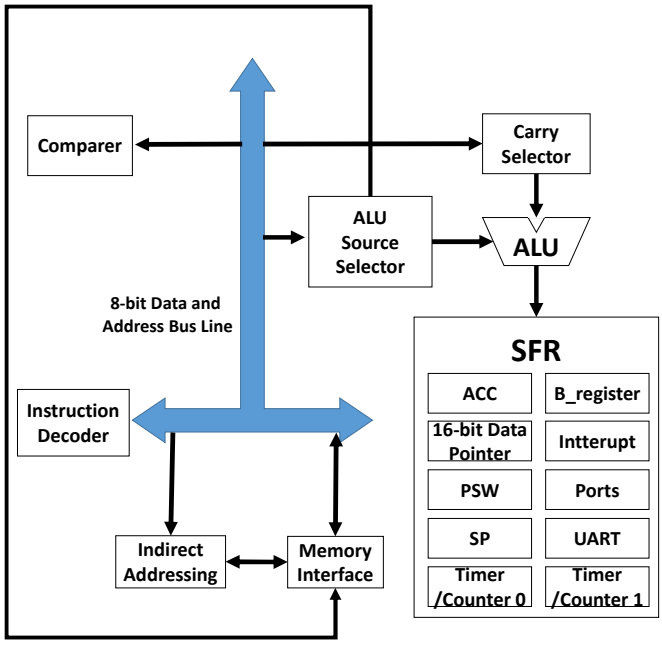

Fig. 5 Block diagram of 8051 microprocessor

III. Results and Discussion

To execute the SET tolerant analysis, first, we inserted the scan chain into the 8051 microprocessor after logic synthesis with a CMOS 65nm technology. Then we generated the test patterns with ATPG program for simulation process. During simulation, the SE signal is set to '1' to apply the test vector on SI port. After applying complete test vector, we set SE signal as '0' to enter the scan capture mode. In scan capture mode, we select the signal randomly and inverse its value to make SET situation. Finally, the SE signal should be set to '0' to enter the scan shift mode and we compared the SO signal and primary output values with expected values to check the soft error occurrence. Fig. 8 shows the flow of this process shortly.

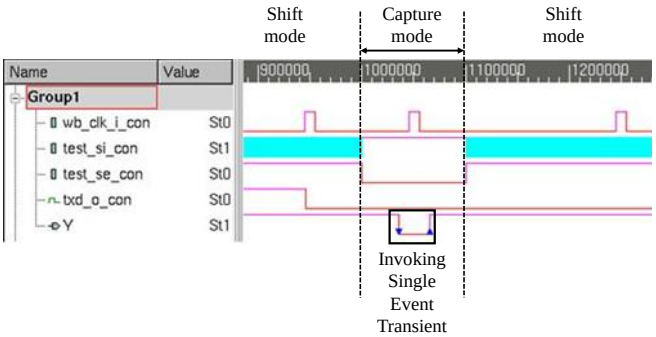

Fig. 6 Waveform of the SET

Fig. 6 shows an example waveform of the simulation process. Randomly selected signal, Y is forced to be changed into '0' value, which means an occurrence of SET. After invoking SET, scan chain enters the scan shift mode and detects the soft error occurrence. The detected errors are reported by the scripts like Fig. 7. By iterating this mechanism for 595 routines with 403 patterns of test vector and counting the number of errors, we

clarify the weakest module of the circuit which needs a radiation hardening. The result is shown in Table I. The soft error count per cell area of SFR module is 277% larger than other modules. It means that SER of SFR module induced by SET is much larger than other modules. Considering the area efficiency and radiation tolerance of the chip, we can conclude that SFR is the primary module that needs radiation hardening techniques.

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Error during scan pattern 86 (detected from parallel unload of pattern 85)
   At T=26140.00 ns, V=262, exp=0, got=1, chain 1, pin txd_o, scan cell 302
   At T=26140.00 ns, V=262, exp=0, got=1, chain 1, pin txd_o, scan cell 303
   At T=26140.00 ns, V=262, exp=0, got=1, chain 1, pin txd_o, scan cell 305
   At T=26140.00 ns, V=262, exp=0, got=1, chain 1, pin txd_o, scan cell 306
   At T=26140.00 ns, V=262, exp=1, got=0, chain 1, pin txd_o, scan cell 308
   At T=26140.00 ns, V=262, exp=1, got=0, chain 1, pin txd_o, scan cell 587
   At T=26140.00 ns, V=262, exp=0, got=1, chain 1, pin txd_o, scan cell 589
   At T=26140.00 ns, V=262, exp=0, got=1, chain 1, pin txd_o, scan cell 608
   At T=26140.00 ns, V=262, exp=0, got=1, chain 1, pin txd_o, scan cell 609
   At T=26140.00 ns, V=262, exp=0, got=1, chain 1, pin txd_o, scan cell 610
   At T=26140.00 ns, V=262, exp=0, got=1, chain 1, pin txd_o, scan cell 612
   At T=26140.00 ns, V=262, exp=0, got=1, chain 1, pin txd_o, scan cell 613
   At T=26140.00 ns, V=262, exp=1, got=0, chain 1, pin txd_o, scan cell 619
   At T=26140.00 ns, V=262, exp=1, got=0, chain 1, pin txd_o, scan cell 621
   At T=26140.00 ns, V=262, exp=1, got=0, chain 1, pin txd_o, scan cell 622
   At T=26140.00 ns, V=262, exp=0, got=1, chain 1, pin txd_o, scan cell 641
   At T=26140.00 ns, V=262, exp=0, got=1, chain 1, pin txd_o, scan cell 642
```

Fig. 7 Soft error occurrence detection script

TABLE I
SOFT ERROR COUNTS PER MODULES

Modules	Cell Area	Number of Errors
SFR	811	172884
Memory Interface	1980	125989
Indirect Addressing	420	22721
Instruction Decoder	944	30364
ALU Source Selector	185	15850
ALU	783	26871
Carry Selector	4	0
Comparer	2	0

Total simulation time is 72,173,500ns.

IV. CONCLUSION

In this paper, we suggested a SET analysis using scan chain mechanism. By inserting the random SET signal in the scan chain and passing through the test vectors, we can check the soft error occurrence in the chip modules. For verifying this algorithm, we used 8051 microprocessor core to simulate the SET situation with 65 nm CMOS technology. We invoked the SET while executing 403 patterns of test vector and check the occurrence of the soft errors. This process offers the verification of radiation hardness of the chip not having any additional overhead, because it uses the architecture of design-for-test circuits like scan chain and scan flip-flops. By using this algorithm, we can verify the radiation hardness of the chip before fabrication process without additional cost and detect the vulnerable module in the chip which needs a radiation hardening technique.

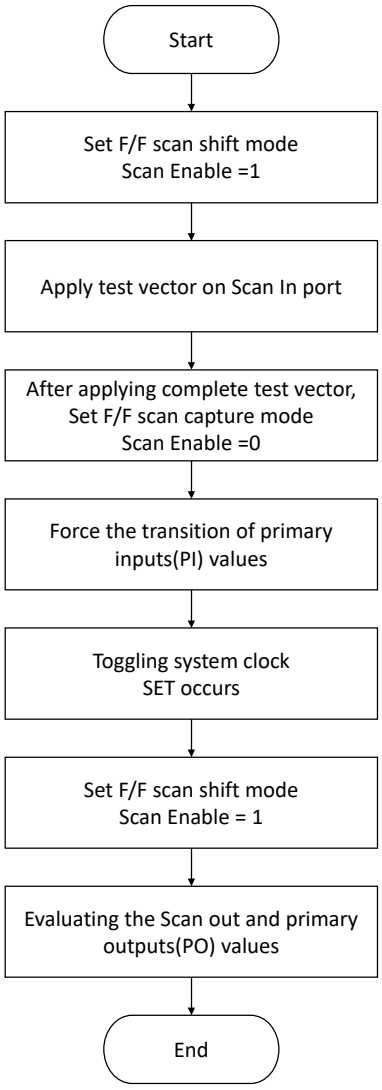

Fig. 8 Flowchart of SET simulation

ACKNOWLEDGMENT

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