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Simulation of Surge Protection for a Direct Current Circuit

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***Abstract*—**In this paper, the performance of a simple surge protection for a direct current circuit was simulated. The protection circuit was developed from modified electric macro models of a gas discharge tube and a transient voltage suppressor diode. Moreover, a combination wave generator circuit was used as source of energy surges. The simulations showed that the circuit presented ensures immunity corresponding with test level IV of the IEC 61000-4-5:2014 international standard. The developed circuit can be modified to meet the requirements of any other equipment to be protected. Similarly, the parameters of the combination wave generator can be changed to provide different surge amplitudes.

***Keywords*—**Combination wave generator, IEC 61000-4-5, Pspice simulation, surge protection.

I. Introduction

POWER surges are characterized by having a fast wave front, followed by a slower fall. They can be caused by switching operations or failures in the electrical network and by the Atmospheric Electrical Discharge (AED) associated effects.

In [1], the 8/20 μs current waveform is defined to simulate the surge associated with AED's secondary effects. In the IEC 61000-4-5:2014 international standard [2], the procedures and levels of testing are set to determine equipment immunity in the presence of a surge. In most of the direct current applications, a protection that ensures immunity according to test level II of [2] is sufficient. However, there are applications where the equipment to be protected is installed outdoors or in places where the induced overvoltages are higher.

The design of a surge protection begins with the identification of the level of immunity to be achieved and specifications of the equipment to be protected. The objective of this work is to simulate the equivalent circuit of a Surge Protection Device (SPD) that complies with the IEC 61000-4-5:2014 test level IV. The aim is to propose a solution that can be re-configurable to model the protection of any DC circuit. The verification of the protection circuit will be made with the simulation tool OrCAD 16.3 PSpice.

II. Conditions for Protection

As equipment to be protected, a circuit with nominal DC voltage of 30 V, maximum supply V_{MAX} = 45 V and purely resistive input impedance of 1.5 kΩ, is considered. With this information and knowing that the protection must comply with test level IV of [2], the parameters that characterize the SPD are determined. Therefore, the withstanding nominal discharge current should be $I_N \geq 2$ kA. The minimum voltage to get into protection state is $V_W > 30$ V, and the level of protection or residual voltage should be $V_P \leq 45$ V.

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III. Surge Simulation

To simulate the energy transient, the electric circuit of Combination Wave Generator (CWG), defined in [2], was reproduced. Fig. 1 presents a variant of the circuit.

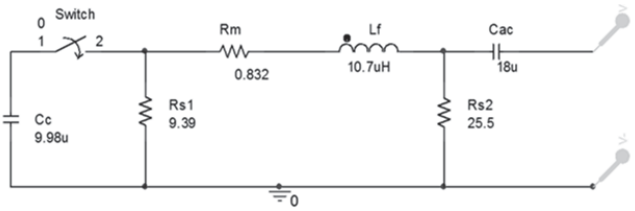

Fig. 1 Circuit combination wave generator

The capacitor *Cc* has an initial charge that provides a voltage of 4252 V between the electrodes. Thus, in the output of the generator, there is a voltage equal to *4* kV. The initial value of capacitor charge *Cc* as the rest of the values of the generator components were deduced from the calculations made in [3].

Simulations were performed to verify that the voltage and current waveforms surges meet the standard requirements. The *Cc* capacitor initial charge was selected to ensure *4* kV peak voltage at the output. Figs. 2 and 3 show the waveforms of the open circuit voltage V_{CA}=*4.04* kV and the short circuit current I_{CC}=*2.09* kA, respectively. Both, voltage and current waveform have a delay in the rising edge, as showed in Fig. 4. The front and duration times of waveforms were observed and compared with the standard requirements. The results are shown in Table I.

IV. Surge Protection Circuit Proposed

The protection circuit must be capable of withstanding current values in the order of kA and, at the same time, ensure a residual voltage lower than the maximum operation voltage of the equipment to protect. Therefore, when the voltage is greater than 30 V, the SPD should get into protection regime and limit the voltage to a level below 45 V.

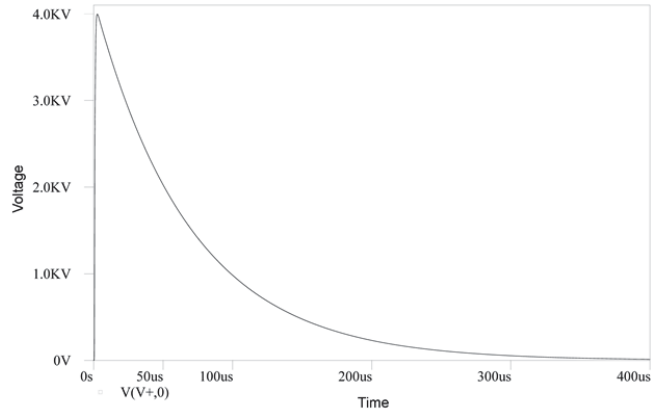

Fig. 2 Open circuit voltage waveform

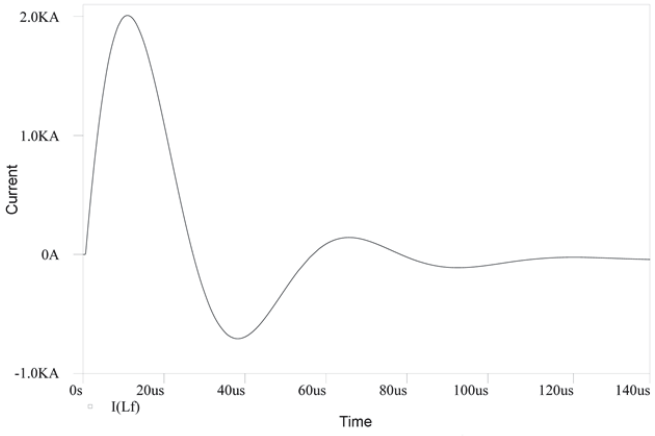

Fig. 3 Short circuit current waveform

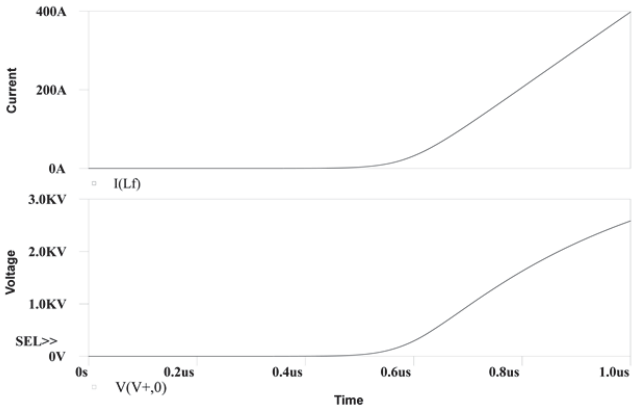

Fig. 4 Voltage and current waveform delay

TABLE I
TIMES OF CWG DEVELOPED MODEL

Parameter	IEC 61000-4-5 Requirement	Simulations result	Percentage error
T_f (V_{CA})	1.2 µs ± 30%	1.23 µs	+2.5%
T_d (V_{CA})	50 µs ± 20%	49.93 µs	-0.4%
T_f (I_{CC})	8 µs ± 20%	8.02 µs	+0.25%
T_d (I_{CC})	20 µs ± 20%	20.17 µs	+0.85%

To meet the above requirements a SPD composed by two protection stages is proposed. Due to its capacity of enduring high currents, a Gas Discharge Tube (GDT*)* will be used in the first stage. However, it has slow response times if compared with the other surge suppressor components.

Because of the GDT limited response time, a Transients Voltage Suppressor diode (TVS) will be employed as the second stage of protection. Although these components can withstand less current than GDT, they have much shorter response times and better features to clamp a stable voltage at their terminals. Fig. 5 shows the presented protection circuit, where the resistor R_L is the input impedance of the equipment to protect.

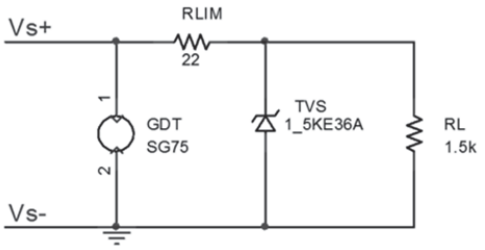

Fig. 5 Protection circuit with R_L load resistor

A. First Stage of Protection

To ensure surges immunity corresponding to test level IV of [2], the current to be tolerated by the SPD must be 2 kA, at minimum. Considering that this current will circulate almost entirely through the primary stage of protection, a GDT with a nominal discharge current I_N equal to or greater than this value must be selected. On the other hand, the DC breakdown voltage for which the GDT enters into conduction mode should be greater than the maximum supply voltage of the equipment to be protected (45 V). However, the impulse breakdown voltage for which the GDT switches to short circuit state should be the lowest possible value. As a result, the second stage protection will dissipate less power. The last parameter to consider is the DC holdover voltage, which must be greater than the maximum voltage supply.

TABLE II
GDT SG75 SPECIFICATIONS

Parameter	Value	Observations
DC Breakdown Voltage	75 V	Typical
Impulse Breakdown Voltage	650 V	(@1 kV/µs)
Insulation resistance	>1 GΩ	(@50 V DC)
Capacitance	<1 pF	
Voltage Holdover	~60 V	
Arc Voltage	~10 V	(@1 A)
Nominal discharge current	2 kA	(x10 @8/20 µs)
Response time	~300 ns	Approx. value obtained from the V-I characteristic curve

Considering the parameters mentioned above was selected the GDT SG75 of Littelfuse [4], which has the characteristics shown in Table II.

The GDT equivalent circuit was developed based on the macro model proposed in [5] and specifications provided in the datasheet. Fig. 6 shows the equivalent circuit.

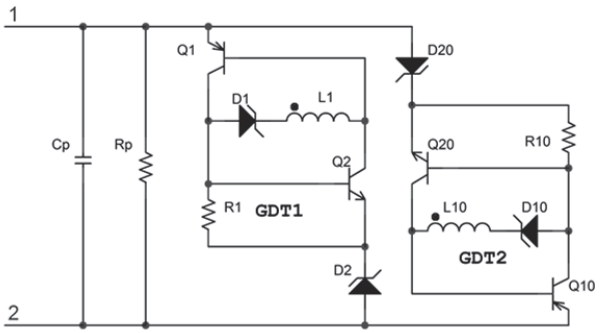

Fig. 6 GDT equivalent circuit

In the previous circuit, the insulation resistance and the device capacitance are modeled by R_P = 1 GΩ and C_P = 1 pF, respectively. Considering that the component has a two-way operation, were modeled two identical circuits, GDT1 for positive bias, and GDT2 for negative bias. Only GDT1 will be analyzed.

The R1 resistor fixes the current required for the transition from the glow region to the arc region. According to the datasheet, this current has value equal to 1 A. Therefore, assuming the base-emitter voltage $V_{BEQ1} \approx 0.7$V, the resistor will be $R1 = 0.7\ \Omega$.

The DC breakdown voltage (V_{DC}) is modeled by the sum of the reverse breakdown voltages of diodes D_1 and D_2, V_{DB1} and V_{DB2}, respectively. V_{DB2} is the arc voltage of approximately 10 V, and knowing that V_{DC} = 75 V, then V_{DB1} = 65 V. The maximum impulse breakdown voltage V_{BDI} = 650 V is given by:

$$V_{BDI} = V_{DC} + L_1 \times \frac{\Delta I}{\Delta t} \quad (1)$$

Therefore, knowing that the maximum current flowing through the GDT will be *2* kA, with an 8/20 µs waveform, the value of L_1 is calculated by:

$$L_1 = \frac{(V_{BDI} - V_{DC}) \times \Delta t}{\Delta I} = \frac{(650-75) \times 8 \times 10^{-6}}{2 \times 10^3} = 2.3 \mu H \quad (2)$$

The 300 ns response time is defined by the parameters T_{F1} = T_{F2} = 150 ns of Q_1 and Q_2 transistors, respectively.

In Fig. 7 is presented the voltage response of the reproduced circuit when subjected to a *4* kV/2kA combined wave, test level IV of [2]. The simulation was carried out by connecting the GDT to the circuit´s output terminals of the Fig. 1.

It is possible to see that when the breakdown voltage reaches the value 388.442 V, the arc voltage is around 12 V. It was verified that the time between the moment the wave surge exceeded the DC breakdown voltage, and the moment where the device fixed it at the arc voltage was 268.034 ns.

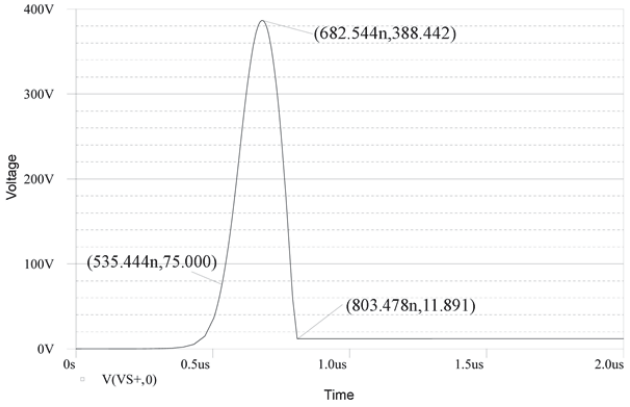

Fig. 7 GDT model voltage response

B. Coordination of Protection Stages

The first stage of protection has a response time close to 300 ns, whereas the TVS present in the second stage has 1 ns typical response time. Therefore, the suppressor diode enters into conduction state before the GDT, circulating through it a large part of the current surge. Considering the restricted diode ability to dissipate energy, it is necessary to introduce a current limiting resistor between the two protection stages. As a result, the TVS will clamp the surge voltage to an acceptable value without risk to its performance, whereas the GDT will get in conduction mode.

As a current limiter, a resistor designed to withstand power surges should be selected. In addition, it should have a low resistance value because it is connected in series with the power line and the drop voltage must be minimal. Therefore, Yageo's 22 Ω resistor SR2512KK-0722RL [6] was selected, represented by *RLIM* in Fig. 5. The power capacity of this component depends on the impulse width to which it is submitted. According to the datasheet specifications, for 10 µs impulse width, it is able to dissipate up to 10 kW.

In order to simplify the analysis, all calculations are made with the peaks values. In the worst-case scenario, the maximum voltage of the GDT V_{BDI} = 650 V and a TVS terminals voltage of 45 V. So, the maximum voltage dropped across the resistor would be 605 V, and the peak current that circulates through it will be:

$$I_R = \frac{605}{22} = 27.5\ A \quad (3)$$

The peak dissipated power will be P_R = 16.64 kW. Because this value is instantaneous and not constant during the 300 ns that takes the GDT to come into operation, there is no contradiction with the information provided in the resistor datasheet.

C. Modeling the Second Stage of Protection

The selection of the TVS is conditioned by the following requirements:

- Residual voltage at its terminals $V_C \leq 45$ V.
- Operating voltage $V_W \geq 30$ V.
- Peak current pulse $I_{PP} \geq I_R$.

From the above parameters Vishay's 1.5KE36A diode [7] was selected, with parameters shown in Table III.

TABLE III
DIODE 1.5KE36A PARAMETERS

Parameters	Value	Observations
V_{WM}	30.8 V	
I_D	1.0 µA	
V_{BR}	36.0 V	Typical
I_T	1.0 mA	
V_C	49.9 V	Maximum (@I_{PP})
I_{PP}	30.1	Maximum
P_{PPM}	1500 W	(@I_{PP} e V_C)

For modeling the TVS, the 1.5KE36 macro model device was used, provided by Vishay [8]. It was modified to obtain the 1.5KE36A model. The changes were made following the information exposed in [9] and specifications from the datasheet. The equivalent circuit is shown in Fig. 8.

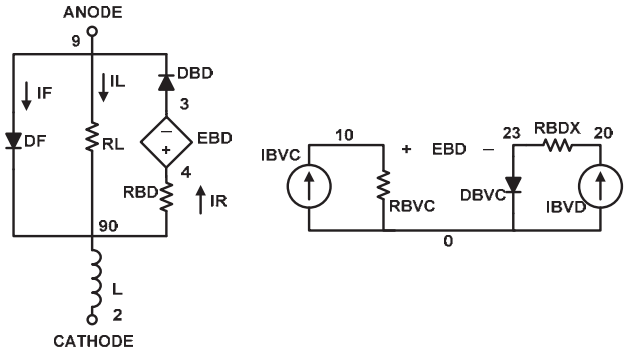

Fig. 8 TVS 1.5KE36A macro model

In the modified circuit, the resistor RL models the ID leakage current and DF the forward work mode. The breakdown voltage (36 V) is defined by the product of current source IBVC = 0.001 A and RBVC = 36000 Ω resistor. The value of the voltage dependent source EBD is modeled by the difference between the breakdown voltage and DBVC diode voltage, including the drop voltage in its series resistance RBDX. Diode DBVC is used to compensate for the drop voltage of the DBD diode, so both diodes are equal and RBDX = RBD.

$$EBD = (IBVC \times RBVC) - (V_{DBVC} + IBVD \times RBDX)\ [V] \quad (4)$$

The current flowing through *DBVC* is defined by:

$$IBVD = I_S \left(e^{\frac{V_{DBVC}}{V_T}} \right) = 0.001\ \text{A} \quad (5)$$

I_S being the diode saturation current, fixed at model equal to *1fA* and V_T thermal voltage, which at ambient temperature is approximately 26 mV. From the above expression, it is possible to calculate the voltage of the diode:

$$V_{DBVC} = V_T \times \ln\left(\frac{IBVD}{I_S}\right) = 0.718\ \text{V} \quad (6)$$

The value of the maximum clamping voltage V_C, specified for the current I_{PP}, is defined by:

$$V_C = EBD + V_{DBD} + I_{PP} \times RBD\ [V] \quad (7)$$

Replacing *IBVD* with the I_{PP} current in (6), was calculated *DBD* diode voltage, being V_{DBD} = 0.9865 V.

Knowing that for the I_{PP} current maximum clamping voltage V_C = 49.9 V, and substituting (4) in (7), was calculated the value of *RBD* = *RBDX* = 0.452888 Ω.

The circuit above is valid for currents lower or equal to I_{PP}. When current exceeds this value, a ΔV_C occurs due to the self-heating of the real device. This behavior is not modeled, neither over current failures.

V. RESULTS

The protection circuit was submitted to power surges originated by the combined waveform generator of Fig. 1. The stimulus amplitude corresponded to 4 kV/2 kA. In Fig. 9, the residual voltage of the circuit protection, as well as the current flowing through the resistor R_L during power surge is shown,

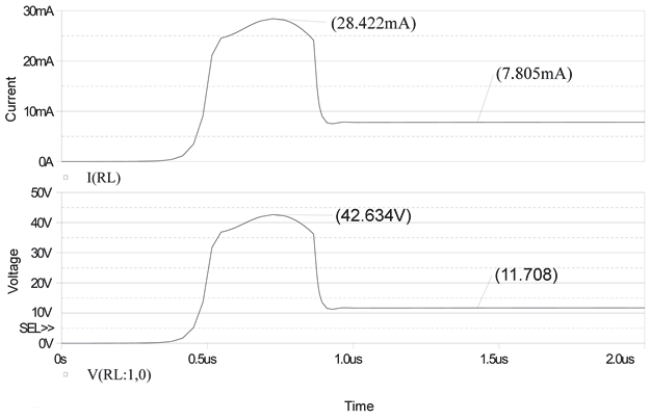

Fig. 9 Current and voltage in the R_L load during the surge

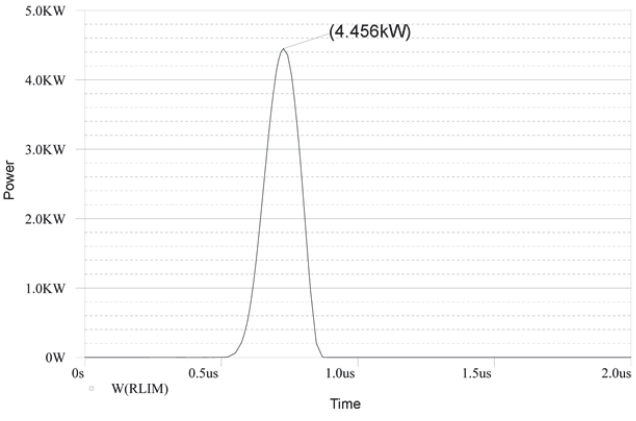

Fig. 10 Dissipated power in the limiting resistor

It is possible to see that in the interval before the GDT enters in conduction mode, the voltage at the load and TVS reached 42.6 V. When the surge is extinguished after several hundred microseconds the voltage and current return to their

initial state. While the peak clamping voltage was 42.6 V, the current through the *TVS* reached 14.232 A, dissipating maximum power of 606.767 W. This same current circulated by the limiting resistor, where the dissipated power was equal to 4.456 kW, as shown in Fig. 10.

When the GDT enter into conduction state, most of the surge current is derived to the earth through it.

VI. Conclusions

The developed protection circuit meets the immunity level IV set in the IEC 61000-4-5:2014 international standard. Voltage in the R_L load resistor terminals did not exceeded the maximum allowed of 45 V, ensuring the protection of the direct current circuit.

The simulations of the proposed solution were successful, although there were differences between the results and the expected ones. The dynamic breakdown voltage of the GDT had lower value than expected. For that reason, the dissipated power in the limiting resistor and TVS were significantly lower too.

The presented model can be re-configured to simulate the protection of numerous DC applications, which is a useful tool before the final project.

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