World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:10, No:10, 2016

Bridgeless Boost Power Factor Correction Rectifier with Hold-Up Time Extension Circuit

Chih-Chiang Hua, Yi-Hsiung Fang, Yuan-Jhen Siao

Abstract**—**A bridgeless boost (BLB) power factor correction (PFC) rectifier with hold-up time extension circuit is proposed in this paper. A full bridge rectifier is widely used in the front end of the ac/dc converter. Since the shortcomings of the full bridge rectifier, the bridgeless rectifier is developed. A BLB rectifier topology is utilized with the hold-up time extension circuit. Unlike the traditional hold-up time extension circuit, the proposed extension scheme uses fewer active switches to achieve a longer hold-up time. Simulation results are presented to verify the converter performance.

Keywords**—**Bridgeless boost, boost converter, power factor correction, hold-up time.

I. Introduction

GENERALLY, a PFC circuit utilizes a full bridge diode rectifier followed by a boost converter, as shown in Fig. 1 (a), which provides an easy way to obtain a high power factor [1]-[5]. However, the conduction loss which reduces the efficiency of the converter is significantly high in the rectifiers.

In order to overcome the shortcoming, the BLB converter, as shown in Fig. 1 (b), is developed to reduce the conduction loss. The conventional BLB topology, as shown in Fig. 2 (a), uses two active switches S_1 and S_2, which are operated in hard switching and causes a large switching loss. There are number of research papers working on the issue of switching loss reduction [6]-[12], Fig. 2 (b) shows a modified version of BLB converter [13], which is also called totem-pole BLB due to the position of the switches.

The hold-up time is the period of time in which the front-end converter can still deliver power for the load after the ac line voltage dropout (in general 20 ms). There are some studies dedicated to minimize the size of the energy-storage capacitor without a decline of efficiency [14]-[17].

The aim of this paper is to present a hold-up time extension technique for the use in a BLB PFC rectifier.

II. The Presented Converter Operation

Fig. 3 (a) shows the presented converter circuit. In the front end of the proposed converter is a bridgeless rectifier (inside the black dotted line as shown in Fig. 3 (a)), while this section is used for the PFC controller to improve the power factor. The rear end of the proposed converter is a hold-up time extension circuit (inside the red dotted line as shown in Fig. 3 (a)). It is noteworthy that proposed hold-up time extension circuit utilizes two capacitors, a large bulk capacitor C_b and a small output capacitor C_o, to extend the hold-up time. In the next section, we will describe the principle of the proposed hold-up time extension circuit (as shown in Fig. 3 (b)), there are two operation modes when the AC line voltage dropouts.

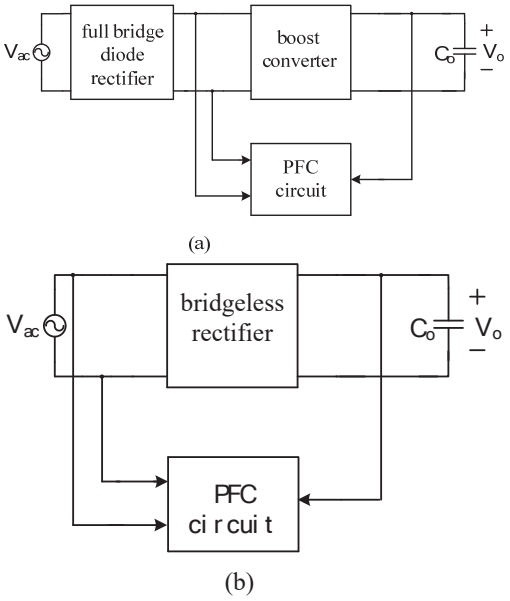
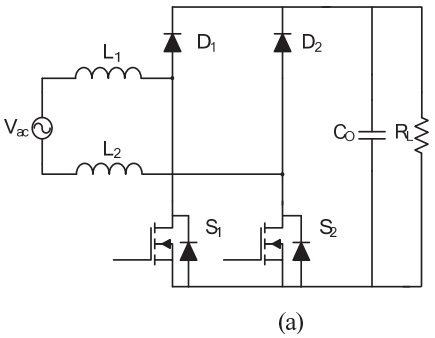


Fig. 1 (a) Block diagram of the conventional PFC converter, (b) Block diagram of the BLB PFC converter



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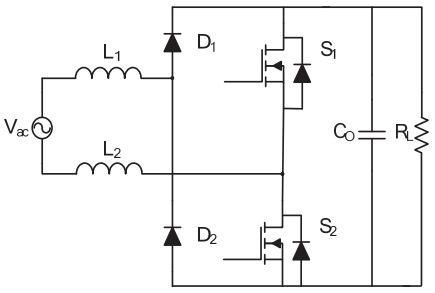
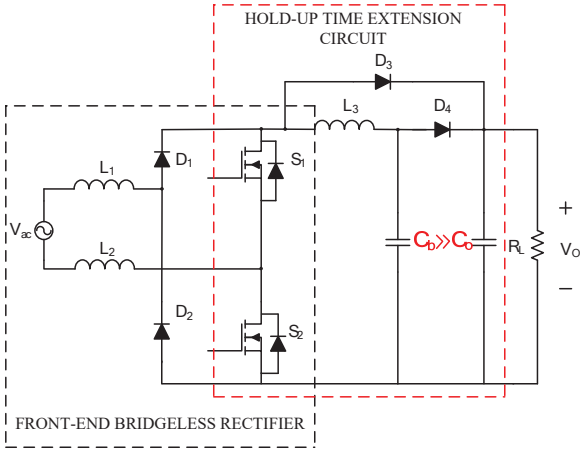
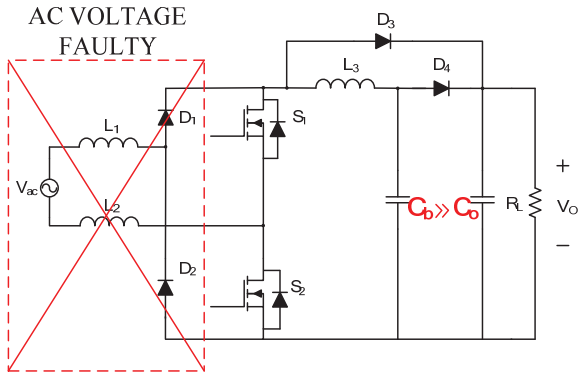


(b)

Fig. 2 (a) The conventional BLB converter topology, (b) The presented BLB converter topology



(a)



(b)

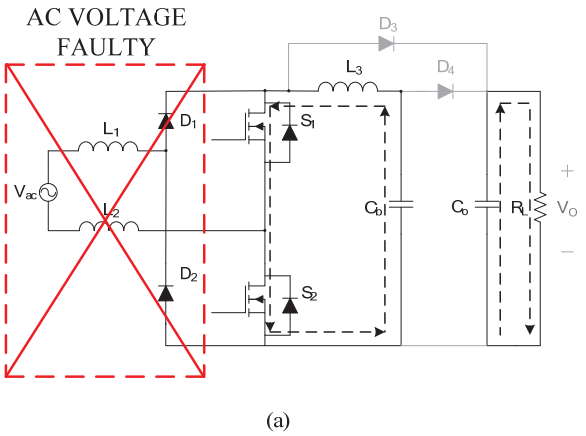
Fig. 3 (a) Circuit of presented converter, (b) Circuit when ac voltage dropout

Mode 1

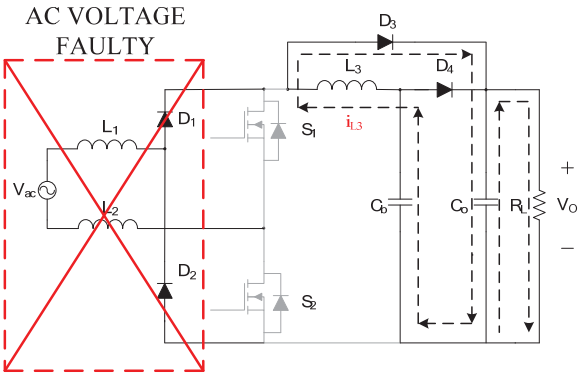
In this mode, the circuit is shown in Fig. 4 (a), power switches S_1 and S_2 are switched on while high capacity capacitor starts discharging, and the current path is L_3-S_1-S_2-C_b.

Mode 2

(Similar to Mode1) In this mode, the operation circuit is shown in Fig. 4 (b), power switching S_1 and S_2 are switched off. Since inductor freewheeling, causes diode D_3 turn on, current path through L_3-D_3-C_o-C_b, the energy of bulk capacitor C_b is delivered to the output capacitor C_o, and this operation is used to extend the hold-up time.



(a)



(b)

Fig. 4 Operating modes of presented circuit (a) Mode1, (b) Mode2

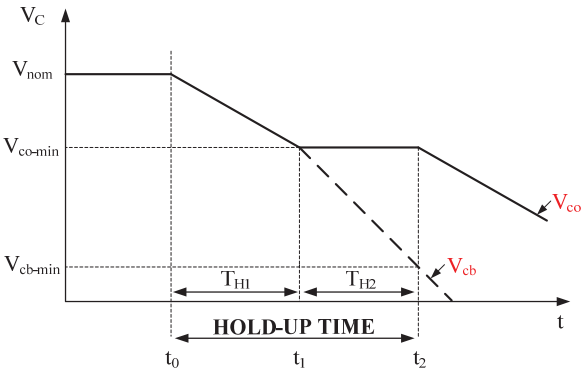


Fig. 5 Waveforms of Vcb and Vco during hold-up time

Fig. 5 indicates the voltage variation of both capacitors during the hold-up time period for the proposed converter. t_o is the time when ac voltage faults, the voltage of bulk capacitor C_b falls from V_{nom} to $V_{co\text{-}min}$, T_{H1} means the hold-up time of PFC converter.

With the presented hold-up time extension circuit, t_1 indicates output capacitor C_o recruit energy from bulk capacitor C_b when $V_{co\text{-}min}$ drop to $V_{cb\text{-}min}$, the hold-up time of this period is T_{H2}, thus the total hold-up time of proposed converter is the summation of T_{H1} and T_{H2}.

III. Simulation Result

The presented BLB converter is simulated using PSIM with the parameters shown in Table I.

Fig. 6 shows the simulated waveforms of V_{cb} and V_{co} for the proposed circuit. The measured values ($V_{co\text{-}min}$ = 250V, $V_{cb\text{-}min}$ = 100V) can be substituted into (1)-(3), and the calculated result shows that the hold-up time is increased.

TABLE I
Parameters of the Proposed Converter Specification

Parameters	Value
input voltage, V_{in}, V_{rms}	85-265
output voltage, V_o, V	400
output power, P_o, W	700
nominal voltage, $V_{nominal}$, V	330
bulk capacitor, C_b, μF	800
output capacitor, C_o, μF	10
switching frequency, f, kHz	100

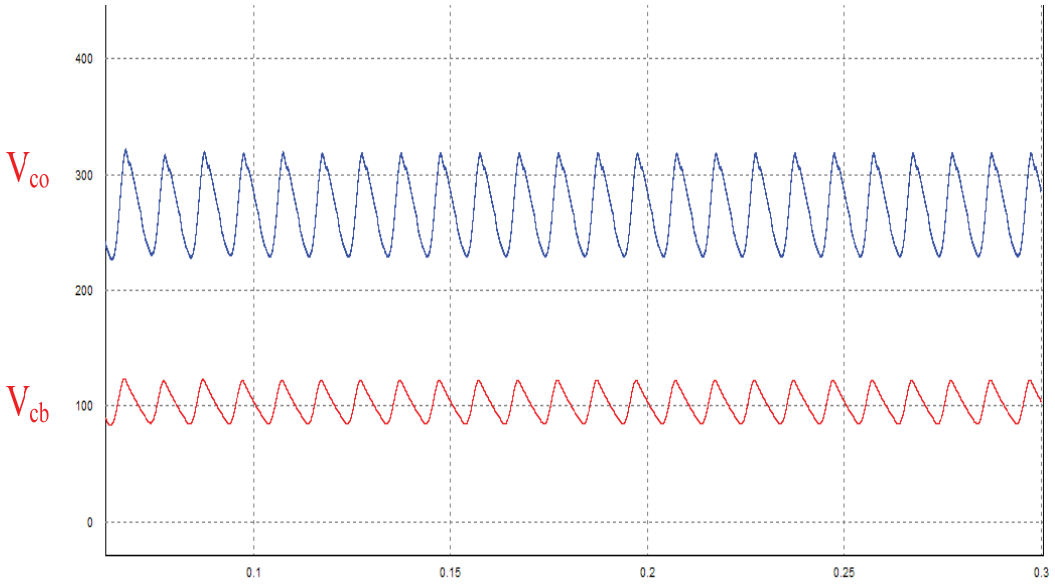


Fig. 6 Simulation result of proposed converter (Vcb and Vco)

The relationship between bulk capacitor C_b and the hold-up time is given by

$$T_{H1} = \frac{C_b\left(V_{nom}^2 - V_{co-\min}^2\right)}{2P_o} \quad (1)$$

The relationship equation of total hold-up time is given by

$$T_{H1} + T_{H2} = \frac{C_T\left(V_{nom}^2 - V_{cb-\min}^2\right)}{2P_o} \quad (2)$$

The relationship between output capacitor C_o and hold-up time is given by

$$T_{H2} = \frac{C_T\left(V_{nom}^2 - V_{cb-\min}^2\right)}{2P_o} - \frac{C_b\left(V_{nom}^2 - V_{co-\min}^2\right)}{2P_o} \quad (3)$$

IV. Conclusion

This paper presents a BLB PFC rectifier with hold-up time extension circuit. Unlike the traditional hold-up time extension circuit, longer hold-up time can be achieved and no additional active switches are needed. Hence, the reliability of the system can be improved because the active switches are not increased. With fewer active switches, the proposed hold-up time extension circuit increases the hold-up time. The simulation results confirm the feasibility and novelty of the presented converter.

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