

# Bridgeless Boost Power Factor Correction Rectifier with Hold-Up Time Extension Circuit

Chih-Chiang Hua, Yi-Hsiung Fang, Yuan-Jhen Siao

**Abstract**—A bridgeless boost (BLB) power factor correction (PFC) rectifier with hold-up time extension circuit is proposed in this paper. A full bridge rectifier is widely used in the front end of the ac/dc converter. Since the shortcomings of the full bridge rectifier, the bridgeless rectifier is developed. A BLB rectifier topology is utilized with the hold-up time extension circuit. Unlike the traditional hold-up time extension circuit, the proposed extension scheme uses fewer active switches to achieve a longer hold-up time. Simulation results are presented to verify the converter performance.

**Keywords**—Bridgeless boost, boost converter, power factor correction, hold-up time.

## I. INTRODUCTION

GENERALLY, a PFC circuit utilizes a full bridge diode rectifier followed by a boost converter, as shown in Fig. 1 (a), which provides an easy way to obtain a high power factor [1]-[5]. However, the conduction loss which reduces the efficiency of the converter is significantly high in the rectifiers.

In order to overcome the shortcoming, the BLB converter, as shown in Fig. 1 (b), is developed to reduce the conduction loss. The conventional BLB topology, as shown in Fig. 2 (a), uses two active switches  $S_1$  and  $S_2$ , which are operated in hard switching and causes a large switching loss. There are number of research papers working on the issue of switching loss reduction [6]-[12], Fig. 2 (b) shows a modified version of BLB converter [13], which is also called totem-pole BLB due to the position of the switches.

The hold-up time is the period of time in which the front-end converter can still deliver power for the load after the ac line voltage dropout (in general 20 ms). There are some studies dedicated to minimize the size of the energy-storage capacitor without a decline of efficiency [14]-[17].

The aim of this paper is to present a hold-up time extension technique for the use in a BLB PFC rectifier.

## II. THE PRESENTED CONVERTER OPERATION

Fig. 3 (a) shows the presented converter circuit. In the front end of the proposed converter is a bridgeless rectifier (inside the black dotted line as shown in Fig. 3 (a)), while this section is used for the PFC controller to improve the power factor. The rear end of the proposed converter is a hold-up time extension

circuit (inside the red dotted line as shown in Fig. 3 (a)). It is noteworthy that proposed hold-up time extension circuit utilizes two capacitors, a large bulk capacitor  $C_b$  and a small output capacitor  $C_o$ , to extend the hold-up time. In the next section, we will describe the principle of the proposed hold-up time extension circuit (as shown in Fig. 3 (b)), there are two operation modes when the AC line voltage dropouts.

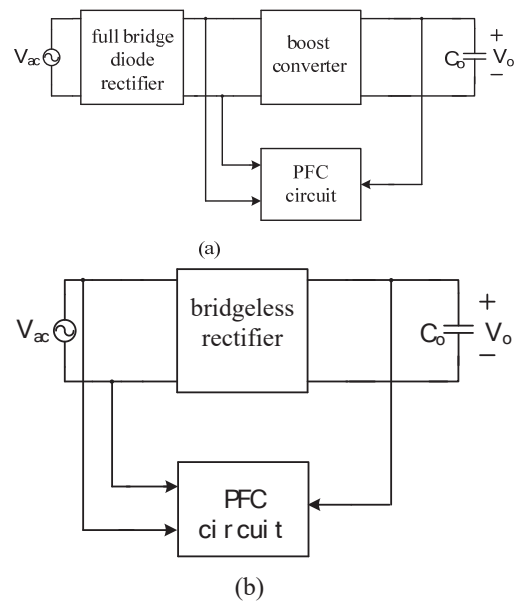
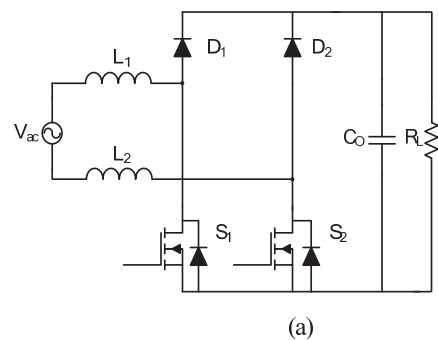


Fig. 1 (a) Block diagram of the conventional PFC converter, (b) Block diagram of the BLB PFC converter



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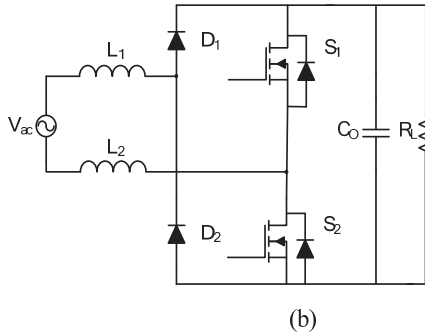


Fig. 2 (a) The conventional BLB converter topology, (b) The presented BLB converter topology

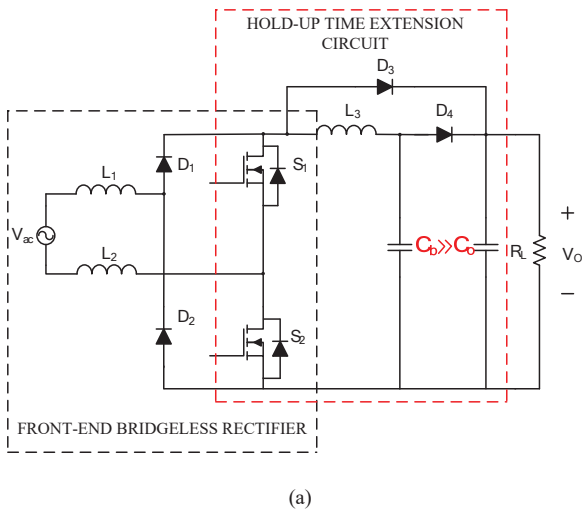


Fig. 3 (a) Circuit of presented converter, (b) Circuit when ac voltage dropout

**Mode 1**

In this mode, the circuit is shown in Fig. 4 (a), power switches  $S_1$  and  $S_2$  are switched on while high capacity capacitor starts discharging, and the current path is  $L_3$ - $S_1$ - $S_2$ - $C_b$ .

**Mode 2**

(Similar to Mode1) In this mode, the operation circuit is shown in Fig. 4 (b), power switching  $S_1$  and  $S_2$  are switched off. Since inductor freewheeling, causes diode  $D_3$  turn on, current path through  $L_3$ - $D_3$ - $C_o$ - $C_b$ , the energy of bulk capacitor  $C_b$  is delivered to the output capacitor  $C_o$ , and this operation is used

to extend the hold-up time.

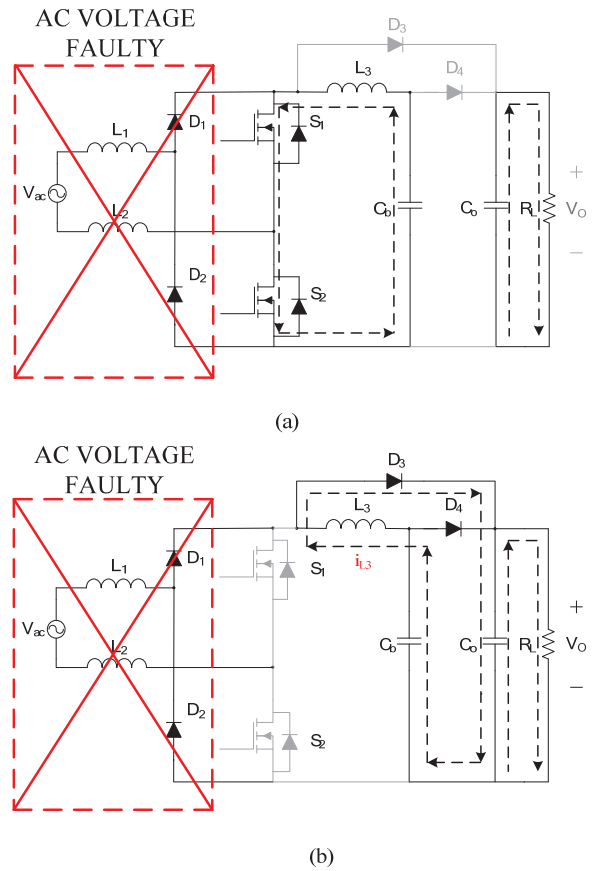


Fig. 4 Operating modes of presented circuit (a) Mode1, (b) Mode2

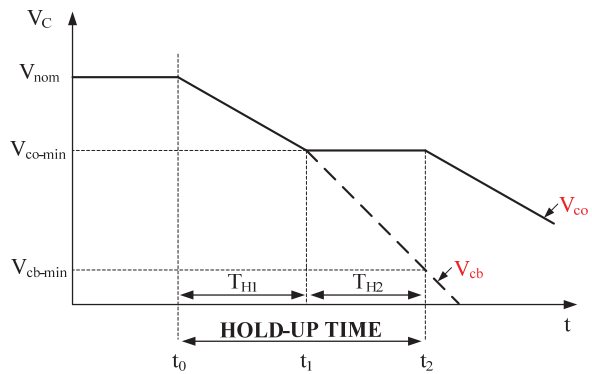


Fig. 5 Waveforms of  $V_{cb}$  and  $V_{co}$  during hold-up time

Fig. 5 indicates the voltage variation of both capacitors during the hold-up time period for the proposed converter.  $t_0$  is the time when ac voltage faults, the voltage of bulk capacitor  $C_b$  falls from  $V_{nom}$  to  $V_{co-min}$ ,  $T_{H1}$  means the hold-up time of PFC converter.

With the presented hold-up time extension circuit,  $t_1$  indicates output capacitor  $C_o$  recruit energy from bulk capacitor  $C_b$  when  $V_{co-min}$  drop to  $V_{cb-min}$ , the hold-up time of this period is  $T_{H2}$ , thus the total hold-up time of proposed converter is the summation of  $T_{H1}$  and  $T_{H2}$ .

### III. SIMULATION RESULT

The presented BLB converter is simulated using PSIM with the parameters shown in Table I.

Fig. 6 shows the simulated waveforms of  $V_{cb}$  and  $V_{co}$  for the proposed circuit. The measured values ( $V_{co-min} = 250V$ ,  $V_{cb-min} = 100V$ ) can be substituted into (1)-(3), and the calculated result shows that the hold-up time is increased.

Parameters	Value
input voltage, $V_{in}, V_{rms}$	85-265
output voltage, $V_o, V$	400
output power, $P_o, W$	700
nominal voltage, $V_{nominal}, V$	330
bulk capacitor, $C_b, \mu F$	800
output capacitor, $C_o, \mu F$	10
switching frequency, $f, kHz$	100

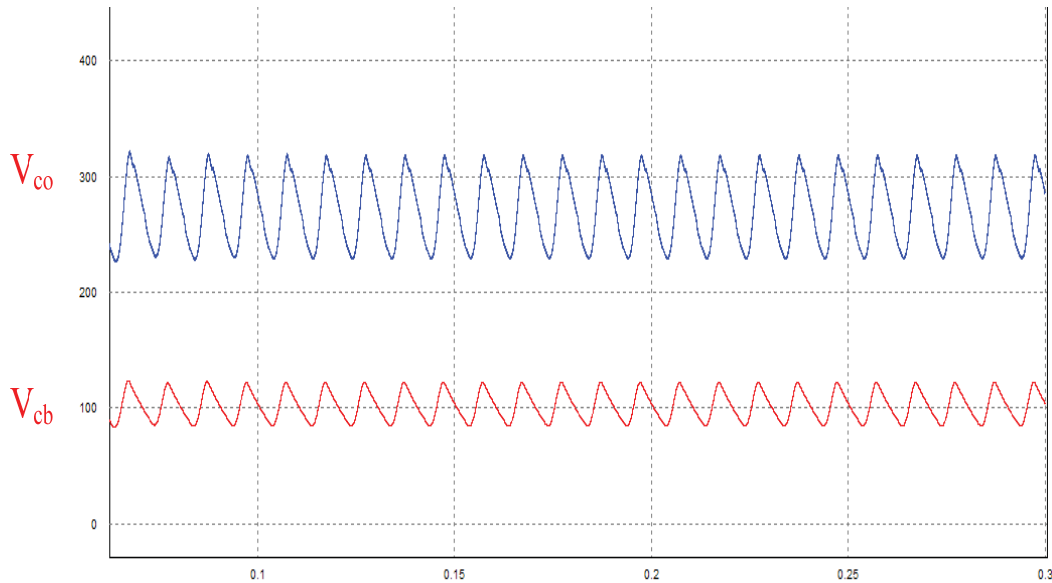


Fig. 6 Simulation result of proposed converter ( $V_{cb}$  and  $V_{co}$ )

The relationship between bulk capacitor  $C_b$  and the hold-up time is given by

$$T_{H1} = \frac{C_b (V_{nom}^2 - V_{co-min}^2)}{2P_o} \quad (1)$$

The relationship equation of total hold-up time is given by

$$T_{H1} + T_{H2} = \frac{C_T (V_{nom}^2 - V_{cb-min}^2)}{2P_o} \quad (2)$$

The relationship between output capacitor  $C_o$  and hold-up time is given by

$$T_{H2} = \frac{C_T (V_{nom}^2 - V_{cb-min}^2)}{2P_o} - \frac{C_b (V_{nom}^2 - V_{co-min}^2)}{2P_o} \quad (3)$$

### IV. CONCLUSION

This paper presents a BLB PFC rectifier with hold-up time extension circuit. Unlike the traditional hold-up time extension circuit, longer hold-up time can be achieved and no additional active switches are needed. Hence, the reliability of the system can be improved because the active switches are not increased. With fewer active switches, the proposed hold-up time

extension circuit increases the hold-up time. The simulation results confirm the feasibility and novelty of the presented converter.

### REFERENCES

- [1] Y. W. Cho, J. M. Kwon, and B. H. Kwon, "Single Power-Conversion AC-DC Converter with High Power Factor and High Efficiency," *IEEE Trans. on Power Electronics*, vol. 29, no. 9, pp.4797 - 4806, Sep. 2014.
- [2] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of three-phase improved power quality ac-dc converters," *IEEE Trans. on Industrial Electronics*, vol. 51, no. 3, pp. 641-660, Jun. 2004.
- [3] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality AC-DC converters," *IEEE Trans. on Industrial Electronics*, vol. 50, no. 5, pp.962-981, Oct. 2003.
- [4] C. da Cunha Duarte and I. Barbi, "A new ZVS-PWM active-clamping high power factor rectifier: Analysis, design, experimentation," in Proc. *IEEE APEC*, 1998, pp.230-236.
- [5] C. Canesin and I. Barbi, "A novel single-phase ZCS-PWM high-power-factor boost rectifier," *IEEE Trans. on Power Electronics*, vol. 14, no. 4, pp.629-635, Jul. 1999.
- [6] L. Huber, Y. Jang, and M. Jovanovic, "Performance evaluation of bridgeless PFC boost rectifiers," *IEEE Trans. on Power Electronics*, vol. 23, no. 3, pp.1381-1390, May 2008.
- [7] K. Muhammad and D.-C. Lu, "Two-switch ZCS totem-pole bridgeless PFC boost rectifier," in Proc. *IEEE PEC on*, Dec. 2012, pp. 1-6.
- [8] C. M. Wang, "A novel ZCS-PWM power-factor preregulator with reduced conduction losses," *IEEE Trans. on Industrial Electronics*, vol. 52, no. 3, pp.689-700, Jun. 2005.

- [9] M. Mahdavi and H. Farzanehfard, "Zero-current-transition bridgeless PFC without extra voltage and current stress," *IEEE Trans. on Industrial Electronics*, vol. 56, no. 7, pp.2540–2547, Jul. 2009.
- [10] H. Y. Tsai, T. H. Hsia, and D. Chen, "A family of zero-voltage-transition bridgeless power-factor-correction circuits with a zero-current-switching auxiliary switch," *IEEE Trans. on Industrial Electronics*, vol. 58, no. 5, pp.1848–1855, May 2011.
- [11] M. Ramezani and S. Madani, "New zero-voltage-switching bridgeless p, using an improved auxiliary circuit," *IET Power Electron.*, vol. 4, no. 6, pp.732–741, Jul. 2011.
- [12] C. C. Hua, Y. H. Fang, and C. H. Huang, "Zero-voltage-transition bridgeless power factor correction rectifier with soft-switched auxiliary circuit," *IET Power Electron.*, vol. 9, no. 3, pp.546–552, Mar. 2016.
- [13] K. S. B. Muhammad and D. D. C. Lu, "ZCS Bridgeless Boost PFC Rectifier Using Only Two Active Switches," *IEEE Trans. on Industrial Electronics*, vol. 62, no. 5, pp.2795 - 2806, May 2015.
- [14] Y. Jang, M. M. Jovanovic', and D. L. Dillman, "Hold-Up Time Extension Circuit with Integrated Magnetics," *IEEE Trans. on Power Electronics*, vol. 21, no. 2, pp.394 - 400, Mar. 2006.
- [15] Y. Jang and M. Jovanović, "Hold-up time extension circuit," *U.S. Patent* 6 504 497B2, Jan. 7, 2003
- [16] Y. Xing, L. Huang, X. Cai, and S. Sun, "A combined front end DC/DC converter," in Proc. *IEEE Applied Power Electron. Conf.*, 2003, pp.1095–1099.
- [17] Y. Yisheng, "A New PFC Converter with Reduced Output Bus Capacitors," *IEEE Conf.*, The 2nd International Symposium on Power Electronics for Distributed Generation Systems., 2010, pp.229-231.