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Analysis of Performance of 3T1D Dynamic Random-Access Memory Cell

Nawang Chhunid, Gagnesh Kumar

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***Abstract*—**On-chip memories consume a significant portion of the overall die space and power in modern microprocessors. On-chip caches depend on Static Random-Access Memory (SRAM) cells and scaling of technology occurring as per Moore's law. Unfortunately, the scaling is affecting stability, performance, and leakage power which will become major problems for future SRAMs in aggressive nanoscale technologies due to increasing device mismatch and variations. 3T1D Dynamic Random-Access Memory (DRAM) cell is a non-destructive read DRAM cell with three transistors and a gated diode. In 3T1D DRAM cell gated diode (D1) acts as a storage device and also as an amplifier, which leads to fast read access. Due to its high tolerance to process variation, high density, and low cost of memory as compared to 6T SRAM cell, it is universally used by the advanced microprocessor for on chip data and program memory. In the present paper, it has been shown that 3T1D DRAM cell can perform better in terms of fast read access as compared to 6T, 4T, 3T SRAM cells, respectively.

***Keywords*—**DRAM cell, read access time, tanner EDA tool write access time and retention time, average power dissipation.

I. Introduction

DYNAMIC Random-Access Memory (DRAM) is widely used in commercial and industrial applications and popularity of DRAM is making it a leading technology driver, with increasing pressure to reduce cost per bit with higher densities, higher speed, and low power dissipation. This also makes DRAM a good candidate to study the technology scaling effects on reliability. As the technology scales down, it results in high performance, but at the same time, it degrades the reliability of the DRAM memory array [5].

On-chip caches depend on SRAM cells. There is a direct impact of scaling on stability, performance, and leakage power. Therefore, it has been seen as a major property for the future SRAMs at nanoscale level because of device mismatch and variations at large scale.

One simple solution for the above problems is to slow down scaling of SRAMs at the expense of lower performance and larger area. However, this would mean the end of Moore's Law scaling of transistor for high density and speed for the future processor designs. To avoid these scaling limitations, recent research has turned to alternative designs that can replace the 6T SRAM cell. One such design is that of 3T1D DRAM, which gives operating speed comparable to that of SRAM without the destructive reads as in the standard 1T1C DRAM cell. Furthermore, 3T1D does not depend on matched transistor strengths, so its reliability is not affected by process variations in the same way that the 6T SRAM cell stability is affected.

Recent research indicates that 3T1D DRAM cell can be used in the place of 6T SRAM cell, such as L1 caches, with negligible performance loss [1]. The term dynamic stands for its leakage phenomenon which degrades the charge stored in the memory cell with the time, i.e. it needs periodic refreshment in order to retain the data. Retention time can be defined as the duration up to which the stored signal can be read from the memory cell. The longer the retention time, the smaller the total leakage current with the memory cell.

In this paper, we have taken three different DRAM cells such as 4T 3T and 3T1D. Read and write operations are performed for storing a single bit in memory. By using T-Spice Tanner EDA tool, analysis of performance DRAM cells are performed and compared at 250 nm technology.

II. The 3T1D DRAM Cell

In 3T1D DRAM Cell, parasitic gate capacitance of gated diode (D1) and that of read device T2 form the storage node capacitance. Data are written to storage node through T1 (write device) and data are read from storage node through T2 (read device) and T3 (read select device).

The gated diode is a semiconductor device which combines the function of a *p-n* junction and a MOS capacitor. The gated diode is characterised by a very high power amplification gain. Considering the high input impedance and low output impedance, the gate-controlled diode acts as a voltage-controlled voltage source. [4]

As shown in Fig. 1, the parasitic gate capacitance of the gated diode (D1) is acting as the storage node capacitor, and it is connected via a writing device (T1) to $\text{Bitline}_{\text{Write}}$ forming the write path. A read device (T2) and a read select device (T3) are connected in series, between the $\text{Bitline}_{\text{Read}}$ and GND, forming the read path. Both read and write paths are decoupled, so operation is independent of the matched transistor ratio as in case of 6T SRAM cell. Data are written and stored in gated diode (D1) as inversion charge for 1-data, and no charge for 0-data. $\text{Bitline}_{\text{Write}}$ and $\text{Bitline}_{\text{Read}}$ form a dual port cell, or they can be tied together for a single port cell.

A. Operation

By raising $\text{WordLine}_{\text{Write}}$ high and holding $\text{WordLine}_{\text{Read}}$ low, data are written into the storage node from $\text{BitLine}_{\text{Write}}$ via T1, by providing 0 V for 0-data and high for 1-data. For reading, $\text{BitLine}_{\text{Read}}$ is previously precharged to high and WordLineRead is pulsed from GND to high. For read 1, the

Gagnesh Kumar is with the National Institute of Technology Hamirpur (H.P.), Himachal Pradesh, India (e-mail: gagnesh78@gmail.com).

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D1 capacitance (Cgs) is large as the channel is on, the storage node voltage (Vstorage) is boosted high and turns T2 on strongly. Then, the voltage at $BitLine_{Read}$ is discharged through T3, T2 to ground. During read 1, gated diode boost the voltage stored at the storage node and helps out in fast reading or reduction in read access time [3]. For read 0, Cgs is much smaller as the channel is off, and voltage at storage node is almost at GND, and T2 remains off [2]-[7].

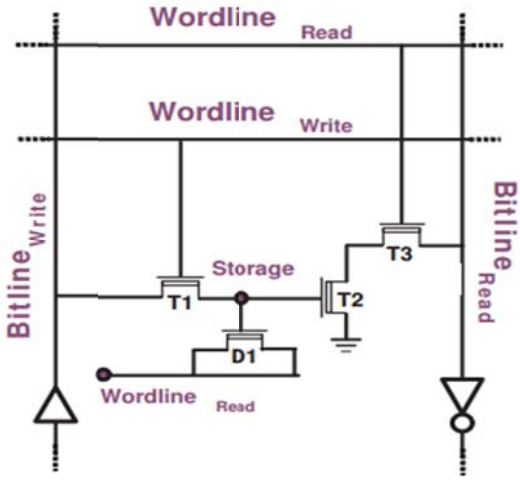


Fig. 1 3T1D-DRAM Cell Schematic

III. Comparative Analysis of 4T, 3T, and 3T1D DRAM Cells

4T DRAM cell consists of four transistors in which cross coupled transistor is acting as storage node, and data are written to and read from the storage node through write/read access transistors.

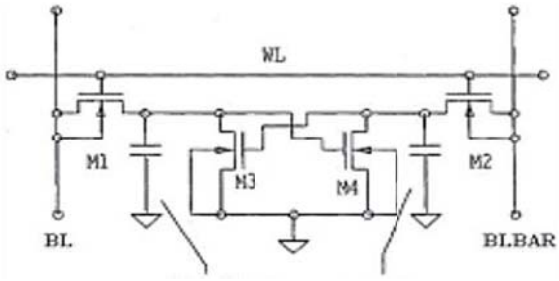


Fig. 2 4T-DRAM Cell Schematic

In 3T DRAM Cell, the parasitic gate capacitance of transistor T_2 acts as the storage node capacitor and read device, and is in series with read select device (T_1).

A. Performance Analysis and Simulation Results

The key parameters which are taken into account to analyze the performance of DRAM cell are read access time, write access time, retention time, and average power dissipation. These are the basic operation related parameters of DRAM to calculate. For the retention time, we simulate this circuit. We write a "1" to our cell and wait for the value of the storage node to decay up to $V_{dd}/4$, then report this interval [6].

a) Write Access Time is calculated when Word line write= $.5V_{DD}$ and Voltage at storage node V(Storage)=$.9(V_{DD}-V_{th1})$
b) Read Access Time is calculated when Word line write= $.5V_{DD}$ and Voltage at $BitLine_{Read}$ falls to V ($BitLine_{Read}$) = $.1\ V_{DD}$
c) Retention Time is calculated when Word line write= $.5V_{DD}$ Voltage at storage node decays to V(Storage) ≈ (V_{DD} /4)

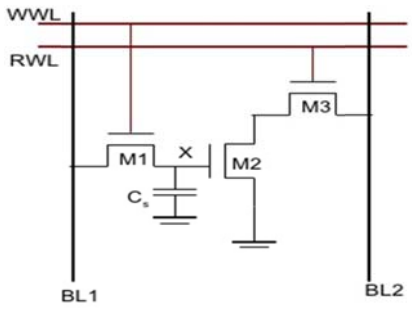


Fig. 3 3T-DRAM Cell Schematic

TABLE I
Write Access Time of DRAM Cells (ps)

V_{DD}(Supply Voltage in volts)	*Write access time(*4T DRAM CELL in *ps)*	*Write access time (*3T DRAM CELL *ps)*	*Write access time (*3T1D DRAM CELL *ps)*
0.7	203.0164	89.6475p	236.4678
0.8	233.1737	119.3147	285.4256
0.9	295.2231	131.1353	332.36
1	338.2089	146.7634	389.7869
1.1	360.1076	177.6707	523.0148

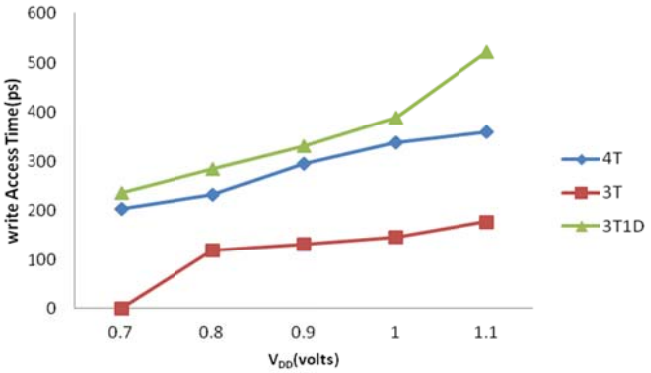


Fig. 4 Write Access Time vs V_{DD}

Write operation is said to be performed when we write '1' at the storage node of the 3T1D DRAM cell. From Fig. 4, it is remarkable that write access time of 3T DRAM cell is the shortest one because the parasitic gate capacitance at storage node has the lowest value as compared to 4T and 3T1D DRAM cell, and write access delay is high at 1.1 V in case of 3T1D, because as we increase V_{DD} delay also increases.

From Fig. 5, it is seen that at low V_{DD} Read access time cannot be determined for 4T DRAM because low V_{DD}(0.7-0.9V) cannot drive the read circuitry. 3T1D has the shortest

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read access time because the gated diode helps out in reading by boosting the storage node voltage.

TABLE II
READ ACCESS TIME OF DRAM CELLS (PS)

V_{DD}(Volts)	4T DRAM CELL *(ps)*	3T DRAM CELL *(ps)*	3T1D DRAM CELL *(ps)*
0.7	---	----	590.6285
0.8	---	888.1687	138.1473
0.9	---	156.752	89.5566
1	105.257	95.3737	70.7436
1.1	76.5633	74.6917	61.954

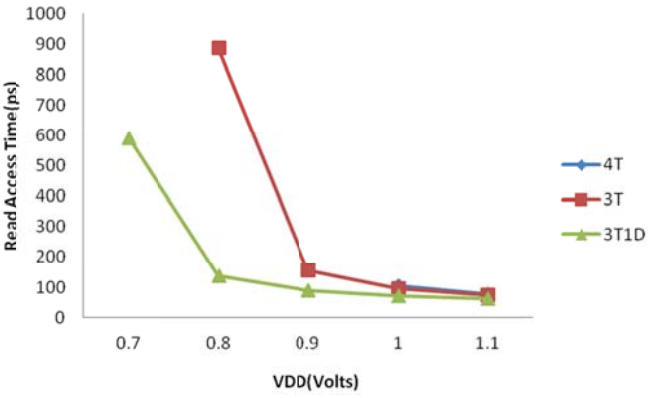


Fig. 5 Read Access Time vs V_{DD}

TABLE III
POWER DISSIPATION (µW)

V_{DD}(Volts)	4T DRAM CELL (*µw*)	3T DRAM CELL (*µw*)	3T1D DRAM CELL (*µw*)
0.7	0.089	0.193	.4363142
0.8	0.145	0.786	.7610046
0.9	0.486	1.168	1.194079
1	1.734	1.696	1.71934
1.1	2.436234	2.381045	2.426245

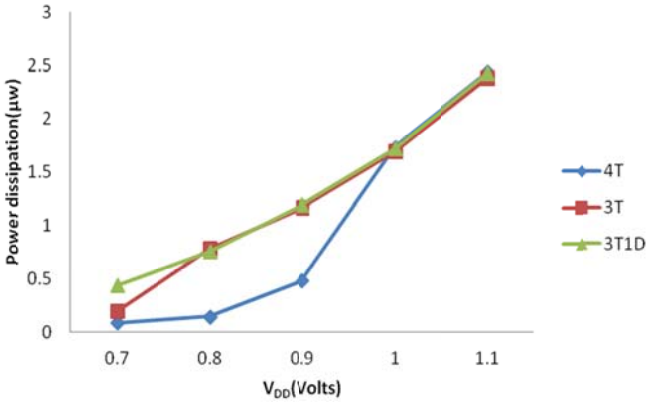


Fig. 6 Power dissipation vs V_{DD}

From Fig 6, it is revealed that 4T DRAM has the lowest power dissipation at low voltages because at these low V_{DD} read operations are not performed.

From Fig. 7, it is clear that 3T1D DRAM has the maximum retention period. Retention period is very important parameter to be taken into account. Due to presence of gated diode with larger (W,L) parameters and boosting property of gated diode result into the large retention period.

TABLE IV
RETENTION PERIOD OF DRAM CELLS(µS)

V_{DD}(Volts)	4T DRAM CELL *(µs)*	3T DRAM CELL *(µs)*	3T1D DRAM CELL *(µs)*
0.7	--	16.5343	27.7
0.8	--	22.6875	38.1349
0.9	--	26.7371	42.7138
1	--	28.07	45.3586
1.1	.742	28.23	48.7345

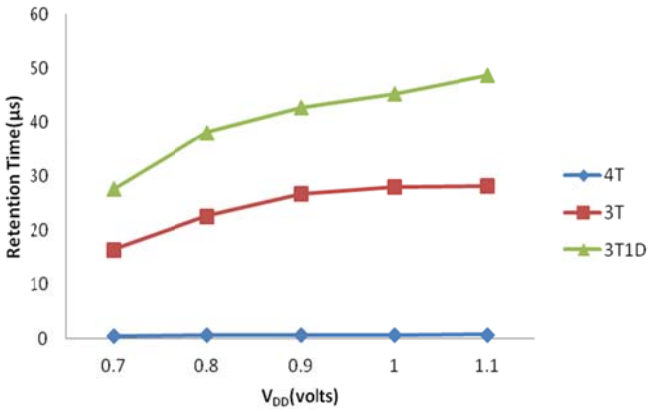


Fig. 7 Retention Time vs V_{DD}

IV. CAUSE OF RETENTION PERIOD DEGRADATION

Retention period of DRAM is the most important key parameter. Retention period can be defined as the duration until the stored signal can be read from the memory cell. The longer the retention time, the smaller the total leakage current with the memory cell. When "1" is stored at node, this results into sub-threshold leakage of T1 and gate tunneling leakage of T2.

For high density and high performance demand of the modern technology gate length is scaled down continuously, which increases the device leakage exponentially across the generation of technology. For DRAM Cell, source of standby power is the leakage current. At nanoscale technology, the most important components of leakage current are the gate tunneling leakage, sub-threshold leakage and reverse bias band to band tunneling junction. Additionally, sub-threshold leakage (T1) is the dominant one affecting the retention period of DRAM cell.

$$I_{ds} = \mu_0 C_{ox} \frac{W}{L}(m-1)(v_T)^2 \times e^{(V_g - V_{th})mv_T} \times (1 - e^{v_{DS}/v_T})$$

where,

$$m = 1 + \frac{C_{dm}}{C_{ox}} = 1 + \frac{\frac{\varepsilon_{Si}}{W_{dm}}}{\frac{\varepsilon_{ox}}{t_{ox}}} = 1 + \frac{3t_{ox}}{W_{dm}}$$

where V_{th} is the threshold voltage, and $v_T = KT/q$ is the thermal voltage. C_{ox} is the gate oxide capacitance; μ_0 is the

zero bias mobility; and m is the subthreshold swing coefficient (also called body effect coefficient). W_{dm} is the maximum depletion layer width, and t_{ox} is the gate oxide thickness. C_{dm} is the capacitance of the depletion layer.

Sub-threshold current is an exponential function of applied gate voltage. Sub-threshold current gets larger for smaller gates (L).

In order to reduce the sub-threshold leakage, we increase the length of the T1 up to an extent so that it does not compromise with the write access time, and parameters of T2 and T3 are varied to improve the read access time as per requirement.

TABLE V
EFFECT OF GATE LENGTH OF T_1 ON RETENTION PERIOD

Gate Length (nm)	L_{T1}=64	L_{T1}=50n	L_{T1}=42n	L_{T1}=32n
Retention Period (μs)	43.3259	33.0854	23.6884	5.0703

Our results indicate that the low retention in 3T1D is primarily due to sub-threshold leakage (T1) due to a weak read access-transistor resulting in majority of the charge flowing into the bit lines. As length of T1 (write access transistor) is increased, there is a substantial decrease in write access time in order to increase the retention time, and at this gate length write access time of DRAM Cell is also acceptable.

V. CONCLUSION

The 3T1D-DRAM cell performance has been analyzed under different variability conditions. First, the device fluctuation analysis has pointed out that the effects of variability on write access becoming critical for cell device reliability. In order to mitigate the observed cell variability several strategies have been presented and (a) resize the width of the write access transistor, T1, has resulted in a relevant improvement of the cell tolerance to the device variability, and (b) environment temperature has shown a cell worsening when is raised up, so, a control and reduction of the cell temperature has to take into account to reduce the device variability impact.

Retention time of DRAM cell is improved by proper choice of (W, L) parameters of transistors T1 and T2, and also by providing body biasing or V_{th} adjustment of write transistor T1.

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