World Academy of Science, Engineering and Technology
International Journal of Chemical and Molecular Engineering
Vol:8, No:9, 2014

Graphene/*h*-BN Heterostructure Interconnects

Nikhil Jain, Yang Xu, Bin Yu

***Abstract*—** The material behavior of graphene, a single layer of carbon lattice, is extremely sensitive to its dielectric environment. We demonstrate improvement in electronic performance of graphene nanowire interconnects with full encapsulation by lattice-matching, chemically inert, 2D layered insulator hexagonal boron nitride (*h*-BN). A novel layer-based transfer technique is developed to construct the *h*-BN/MLG/*h*-BN heterostructures. The encapsulated graphene wires are characterized and compared with that on SiO_2 or *h*-BN substrate without passivating *h*-BN layer. Significant improvements in maximum current-carrying density, breakdown threshold, and power density in encapsulated graphene wires are observed. These critical improvements are achieved without compromising the carrier transport characteristics in graphene. Furthermore, graphene wires exhibit electrical behavior less insensitive to ambient conditions, as compared with the non-passivated ones. Overall, *h*-BN/graphene/*h*-BN heterostructure presents a robust material platform towards the implementation of high-speed carbon-based interconnects.

***Keywords*—**Two-dimensional nanosheet, graphene, hexagonal boron nitride, heterostructure, interconnects.

I. Introduction

INTERCONNECT wire systems need to keep pace with advancements in miniaturization of integrated circuits [1]. The current industry standard for lateral interconnects is copper which has its limitations at aggressively reduced dimensions that are bound to be encountered below the 13 nm node. These limitations include degradation in resistivity and hence increased propagation (RC) delay due to the effect of increased carrier scattering [2]. Another issue that copper interconnects face with reducing the pitch is that of crosstalk [3]. The current density in interconnects is expected to rise beyond the electromigration-induced failure limit of copper (10^6 A/cm^2) [4]. These critical issues while scaling down of copper interconnects are presenting an ever increasing demand for new/hybrid material systems, novel fabrication processes, and innovative integration/packaging strategies for on-chip wiring applications.

II. Research Concept

We explore the possibility of using graphene as an alternative material for interconnects in the post-Cu era. Graphene, a two-dimensional (2D) allotrope of carbon with strong in-plane sp^2 bonding, exhibits several attractive material/electrical properties including long-range ballistic transport, superb thermal conductivity, electromechanical robustness, and high current density [5]. While it was initially obtained by micromechanical exfoliation process which is unsuitable for in-line processes, growth methods have now been developed that yield large-area, high-quality graphene using fab-compatible processes like chemical-vapor-deposition (CVD). This makes graphene an attractive material for on-chip interconnects. However, since graphene is a 2-D material, a thin sheet of carbon atoms with its conductive property arising out of the 2D electron gas (2DEG), the dielectric surroundings of graphene strongly impact its carrier transport properties.

While most of the work on the study of graphene has been limited to using SiO_2 as a substrate material, it has been reported that the amorphous nature of SiO_2 has a strong negative influence on the conductivity of graphene. Indeed significant degradation of carrier transport characteristics has been reported in graphene on SiO_2 substrate [6]. In contrast, graphene on hexagonal boron nitride (*h*-BN) has been shown to retain a much higher percentage of its pristine properties. *h*-BN is an isomorph of graphene with a lattice structure similar to graphene (very close lattice constant, ~1.7% mismatch), it is free of any dangling bonds at the surface and is chemically inert with a bandgap of ~ 5.5 eV [7]. We have previously reported that graphene interconnects on *h*-BN substrate demonstrate improved performance and reliability in terms of key metrics such as sheet resistance, carrier mobility, and breakdown characteristics [8]. However, adsorbates like O_2 and H_2O molecules affect the electrical behavior of uncovered graphene, significantly degrading interconnect performance over time.

Another issue widely known with graphene is the degradation of metal contacts due to oxidation over time. These factors restrict the practical use of graphene as an interconnect material despite its attractive intrinsic material characteristics. Theoretically it has been predicted that *h*-BN can also act as an encapsulating layer preventing the adsorption and oxidation. However, it is critical that such a fabrication scheme doesn't open up a zero-field bandgap in graphene which has been confirmed by DFT calculations, thereby preserving its semi-metal nature [9]. Mayorov *et al.* and Wang *et al.* have have reported ballistic transport in micrometer scale in encapsulated graphene transistors along with high carrier mobility and injection velocity [10], [11]. We have fabricated encapsulated graphene structures in *h*-BN to investigate the key performance and reliability metrics of *h*-BN/graphene/*h*-BN heterostructures in interconnect applications. We envision that the *h*-BN EGIs would pave the way towards the implementation of high-speed interconnect, coupled with growth process enabling high-quality *in-situ* assembly of *h*-BN on graphene and vice-versa using CVD method.

SiO_2-coated Si wafers are the starting point for sample

N. Jain and B. Yu are with the College of Nanoscale Science & Engineering, State University of New York, Albany, NY 12202 USA (phone: 518-956-7492; fax: 518-956-7492; e-mail: byu@albany.edu).

Y. Xu is with the Department of Information Science & Electronic Engineering, Zhejiang University, Hangzhou, China.

fabrication with thin multilayer *h*-BN (Momentive Systems Inc.) transferred on to the surface using micromechanical exfoliation method. Monolayer graphene was grown by CVD method. A copper foil (25 µm thick) was cut into 1 cm × 4 cm strips and dipped in acetic acid (CH_3COOH) for 15 minutes to remove any native oxides and organic impurities. Afterwards, the Cu strips were loaded into the growth chamber and annealed at 1000°C in an Ar (80sccm) + H_2 (4.5 sccm) environment. Graphene is grown using CH_4 (20 sccm) as carbon precursor in Ar (180 sccm) +H_2 (4.5 sccm) at 1000°C for 30 minutes. After cooling-down, the Cu/graphene stack was coated with PMMA in a spin-coater at 2000 rpm for 30 seconds and annealed on a hot plate at 90°C for 3 minutes. Small pieces of Cu/graphene/PMMA stack were cut and placed in iron chloride which etched away Cu, leaving graphene/PMMA bilayer floating on top of the solution. The graphene was cleaned by repeatedly washing in deionized water and then transferred to the target substrate. The PMMA was removed by acetone. CVD grown graphene is then transferred on to the substrate covering *h*-BN flakes, and negative e-beam resist patterning coupled with plasma etching is used to etch away graphene from the regions where it is not covering the *h*-BN flakes. Gold contacts (50 nm thick) are formed on graphene using electron-beam evaporation with a thin Ti interlayer (5 nm) included at the metal-graphene interface to promote metal adhesion on the surface of graphene and SiO_2. The samples are annealed in an Ar + H_2 environment at 300°C for three hours, followed by electrical stress anneal (up to 10 V) to remove adsorbates. This is followed by testing of the samples for pre-encapsulation conditions in a Lakeshore probe station under ultrahigh vacuum.

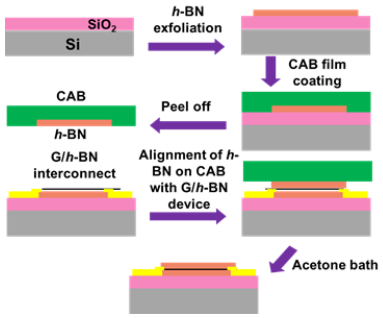

Fig. 1 A schematic representation of the layer-by-layer transfer process used for assembling top layer of *h*-BN on uncovered *h*-BN/Graphene interconnects

The top passivating layer of *h*-BN has been assembled using a novel method of layer-by-layer transfer as shown in Fig. 1. A highly viscous solution of cellulose acetate butyrate (1.5 gm) in ethyl acetate (15 ml) is created by magnetic stirring for 3 hours at 100°C. Micromechanical exfoliation on to a SiO_2/Si substrate yields thin multilayer flakes of *h*-BN on the surface of the substrate which are identified with an optical microscope. This is followed by covering the substrate (which has *h*-BN flakes) with a thick layer of the cellulose acetate butyrate (CAB) solution by spin-coating at 3200 rpm for 1 min. Next the sample is thermally annealed at 90°C for a minute following which the CAB film is peeled off the substrate. The film takes *h*-BN flakes along with itself from the surface of the substrate. This film is then placed on top of the target substrate (with pre-existing *h*-BN/graphene interconnects) and *h*-BN flake on the film is aligned with the uncovered interconnect wire using a high-resolution microscope. A drop of ethyl acetate is used to adhere the film to the surface and subsequently the sample is left in a bath of warm acetone for 60 mins to dissolve the polymer leaving *h*-BN on top of the interconnect wire. This generates graphene interconnect samples encapsulated in *h*-BN which are tested in vacuum as well as ambient conditions without any electrical stress annealing. A schematic and a picture of the actual device is presented in Fig. 2. It can be noted that the top passivating layer of *h*-BN covers not just the graphene strip but also the metal contacts to graphene thereby encapsulating the entire device fully.

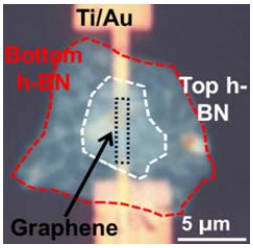

Fig. 2 Top view image of the encapsulated graphene interconnect using optical microscope

III. Results and Discussion

For the encapsulated device, electrical characteristics are measured after thermal annealing of the sample at 300°C for 5 hours in an Ar + H_2 environment. The back-gate voltage (V_{BG}) is scanned from -50 V to 50 V. The samples were tested in ambient conditions before pumping down the chamber of the probe station to vacuum and then the measurements were repeated. After the assembly of the top *h*-BN layer, the sample is again tested for its R-V_{BG} characteristics in ambient conditions and subsequently in vacuum. Annealing of the sample is avoided before electrical characterization post-encapsulation. The obtained results are shown in Fig. 3 (a). For uncovered samples, it is observed that the wire resistance is lower in vacuum as compared with that in air. This change can be attributed to the fact that adsorbed species on graphene act as a source for charged carrier scattering resulting in reduced conduction. In vacuum, many of these impurities get desorbed resulting in a cleaner surface and lower scattering which is seen as higher levels of current passing through the graphene wire. However, once the graphene wire is encapsulated with *h*-BN, not only is the Dirac peak resistance further reduced, but it is also observed that the R-V_{BG} characteristics of the sample do not show much deviation when the measurements are taken in air or in vacuum. This environment insensitivity is a distinct advantage of

encapsulation as carrier scattering through adsorbates can result in currents being an order of magnitude lesser than the expected value.

The contact resistance is estimated from the value of the *R*-V_{BG} curve away from the Dirac peak where it saturates to give the value of series resistance, since graphene's resistance away from the Dirac peak is expected to be negligible. It is observed that the contact resistance is also a function of characterization environment (Fig. 3(b)). For uncovered devices, the contact resistance is lower when the sample is tested in vacuum as compared to when it is tested in ambient conditions. However, post-encapsulation, it is observed that the contact resistance stays constant irrespective of the environment in which the sample is tested. This could be attributed to contact degradation due to oxidation of titanium in the metal-graphene interface for the uncovered devices so when a top passivating layer of *h*-BN is present, these oxidation issues are resolved.

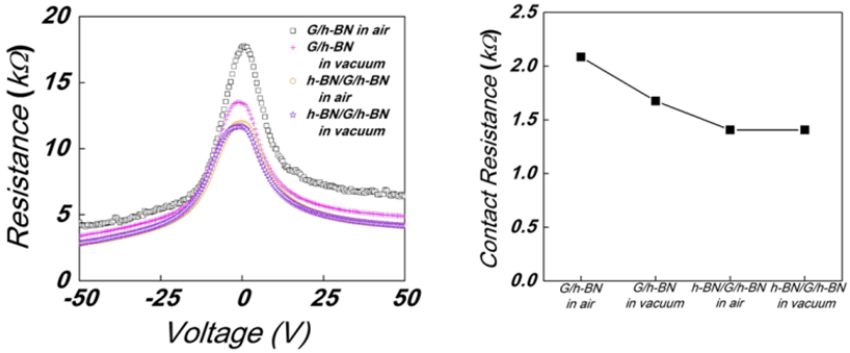

Fig. 3 (a) shows graphene device resistance versus backgate voltage (b) shows the contact resistance for all the cases (G/*h*-BN on air, G/*h*-BN in vacuum, *h*-BN/G/*h*-BN in air, *h*-BN/G/*h*-BN in vacuum)

As earlier mentioned, graphene is immensely sensitive to its dielectric environment and in most reported cases, loss of carrier mobility has been observed in graphene when it is brought in contact with a dielectric. This is the reason why ultra-high values of mobility have been reported in suspended graphene compared to the values observed in graphene on SiO_2 or *h*-BN. However, we observed negligible loss in carrier mobility in graphene sample that is encapsulated with the top *h*-BN layer, as shown in Fig. 4(a). This arises out of the fact that *h*-BN forms a near-ideal interface with graphene as they are both two-dimensional layered materials with nearly identical lattice structure, self-terminating surfaces with weak van der Waals interactions, as well as large optical phonon energy in *h*-BN. This ensures that there is no addition to the RC delay leading to a lagged response of circuit systems, since *h*-BN encapsulation has negligible impact on the carrier mobility.

The structures are also tested for reliability of the interconnect wires by measuring the maximum voltage and maximum current density that the wire can withstand before failure under high level of electrical stress. Voltage across the graphene wire is ramped up and corresponding current in the wire is observed. It can be noticed that the Joule heating induced breakdown limit, in terms of breakdown voltage and current density, is largely increased as compared with the sample without *h*-BN encapsulation, as shown in Fig. 4 (b). Since the breakdown mechanism depends on Joule heating of the samples due to high current values, this improvement can be attributed to the higher thermal conductivity of *h*-BN (30 W/mK) as compared with that of air (0.025 W/mK) as the presence of *h*-BN on both sides of graphene provides better dissipation than air/graphene/*h*-BN system.

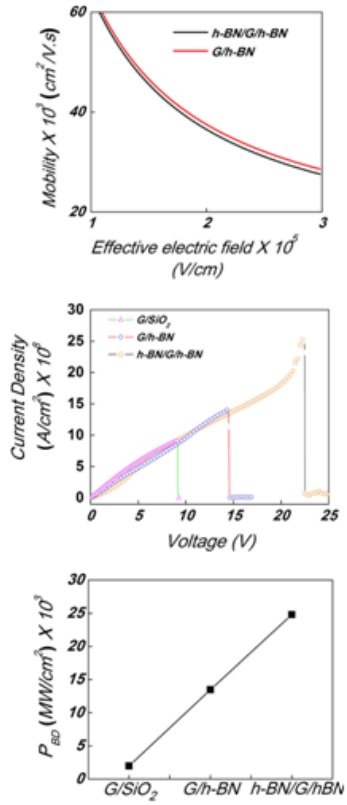

Fig. 4 (a) Mobility in encapsulated graphene interconnects is negligibly less than the uncovered interconnects (b) Current density before breakdown in graphene interconnects (c) Power density required for breakdown in graphene interconnects

The maximum current density observed before permanent breakdown is 2.5×10^9 in the *h*-BN encapsulated graphene

wires. Interconnects are further compared based on the power density required for graphene breakdown. Considerable improvement (~ 100%) can be clearly seen in the breakdown power density in an encapsulated interconnect compared with an open sample as shown in Fig. 4 (c). The breakdown power density is calculated using the relation, $P_{BD} = J_{BD} (V_{BD} - J_{BD}R)$. Here J_{BD} is the current density at breakdown. V_{BD} is the applied voltage that causes the breakdown. R is the total resistance including that of graphene wire and metal contacts.

IV. Conclusion

We have shown that *h*-BN is an excellent dielectric to encapsulate graphene interconnects due to its ability to form near-perfect interface with graphene. This results in increasing the reliability of graphene interconnects with maximum current density before permanent breakdown being in excess of 10^9 A/cm^2 without any loss of carrier mobility as a result of the encapsulation process. Time-dependent shift in graphene's performance has been mostly eliminated as a direct consequence of the encapsulation process as it avoids adsorption of ambient impurities. These results indicate towards the possibility of encapsulated graphene interconnects getting integrated with the current fabrication processes to replace copper in the future generation electronic chips.

Acknowledgment

The research was supported in part by National Science Foundation (CMMI-1162312) and SRC.

References

[1] W. Steinhogl, G. Schindler, G. Steinlesberger, M. Traving, and M, Engelhardt, "Comprehensive study of the resistivity of copper wires with lateral dimensions of 100 nm and smaller," *Journal of Applied Physics*, 97, 023706–023706–7, 2005.

[2] G. Steinlesberger, M. Engelhardt, G. Schindler, W. Steinhögl, A. Von Glasow, K. Mosig, and E. Bertagnolli, "Electrical assessment of copper damascene interconnects down to sub-50 nm feature sizes *Microelectronic Engineering*, 64, 409–16, 2002.

[3] J. A. Davis, R. Venkatesan A. Kaloyeros, M. Beylansky, S. J. Souri, K. Banerjee, K. C. Saraswat, A. Rahman, R. Reif, and J. D. Meindl, "Interconnect limits on gigascale integration (GSI) in the 21st century," *Proceedings of the IEEE*, 89, 305–24, 2001.

[4] P. C. Wang, and R. G. Filippi, "Electromigration threshold in copper interconnects," *Applied Physics Letters*, 78, 3598–600, 2001.

[5] A. K. Geim and K. S. Novoselov, "The rise of graphene," *Nature Mater*ials, 6, 183–91, 2007.

[6] J. H. Chen, C. Jang, S. Xiao, M. Ishigami, and M. S. Fuhrer, "Intrinsic and extrinsic performance limits of graphene devices on SiO2," *Nature Nanotechnology*, 3, 206–9, 2008.

[7] C. R. Dean, A. F. Young, I. Meric, C. Lee, L. Wang, S. Sorgenfrei, K. Watanabe, T. Taniguchi, P. Kim, K. L. Shepard, and J. Hone, "Boron nitride substrates for high-quality graphene electronics, *Nature Nanotechnology,* 5, 722–6, 2010.

[8] N. Jain, T. Bansal, C. Durcan, and B. Yu, "Graphene-Based Interconnects on Hexagonal Boron Nitride Substrate," *IEEE Electron Device Letters*, 33, 925–7, 2012.

[9] X. Zhong , R. G. Amorim, R. H. Scheicher, R. Pandey, and S. P. Karna, "Electronic structure and quantum transport properties of trilayers formed from graphene and boron nitride," *Nano scale,* 4, 5490–8, 2012.

[10] A. S. Mayorov, R. V. Gorbachev, S. V. Morozov, L. Britnell, R. Jalil, L. A. Ponomarenko, P. Blake, K. S. Novoselov, K. Watanabe, T. Taniguchi, and A. K. Geim, "Micrometer-Scale Ballistic Transport in Encapsulated Graphene at Room Temperature," *Nano Letter,* 11, 2396–9, 2011.

[11] H. Wang, T. Taychatanapat, A. Hsu, K. Watanabe, T. Taniguchi, P. Jarillo-Herrero, and T. Palacios, "BN/Graphene/BN Transistors for RF Applications," *IEEE Electron Device Letters,* 32 1209–11, 2011.