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Very High Speed Data Driven Dynamic NAND Gate at 22nm High K Metal Gate Strained Silicon Technology Node

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***Abstract*—**Data driven dynamic logic is the high speed dynamic circuit with low area. The clock of the dynamic circuit is removed and data drives the circuit instead of clock for precharging purpose. This data driven dynamic nand gate is given static forward substrate biasing of Vsupply/2 as well as the substrate bias is connected to the input data, resulting in dynamic substrate bias. The dynamic substrate bias gives the shortest propagation delay with a penalty on the power dissipation. Propagation delay is reduced by 77.8% compared to the normal reverse substrate bias Data driven dynamic nand. Also dynamic substrate biased D3nand's propagation delay is reduced by 31.26% compared to data driven dynamic nand gate with static forward substrate biasing of Vdd/2. This data driven dynamic nand gate with dynamic body biasing gives us the highest speed with no area penalty and finds its applications where power penalty is acceptable. Also combination of Dynamic and static Forward body bias can be used with reduced propagation delay compared to static forward biased circuit and with comparable increase in an average power. The simulations were done on hspice simulator with 22nm High-k metal gate strained Si technology HP models of Arizona State University, USA.

***Keywords*—**Data driven nand gate, dynamic substrate biasing, nand gate, static substrate biasing.

I. Introduction

RESEARCHERS are continuously exploring the ultra low power regions as well as the ultra high speed regions. Also these efforts could be for ultra low power only or for ultra high speed only. One can operate transistor in sub threshold region for low power applications. There have been efforts to go for better circuitry or change the technology to have better result along with smaller size.

In [1], channel length engineering method is illustrated for the standard cell optimization of cells in standard cell library. They have proposed a test structure to explore the operation and leakage current of nand gate with 3 inputs.

Researchers are heading towards organic circuit as well and so a lot more interest is in the organic thin film transistor (OTFT) [2]. As we move into higher and higher (lower nanometre range) technology nodes, there comes the limitations due to short size. The examples of these are short channel effects and high variability. To overcome these, new devices and new technologies are researched into, such as fully depleted-silicon on insulator, nanowire, graphene and also carbon nanotube technology based devices [3], [5]-[7]. There have been reports on Amorphous oxide based semiconductor thin film transistors (TFT). TFT have higher electron mobility compared to organic and silicon technology [7]. There have been reports also that devices with 1xVdd supply voltage tolerance are made to work with 2xVdd supply [8].

In this paper, Part II is the review part on NAND logic gate and includes technical and technological variations and development of logic gates and NAND gate in particular. Part III shows the new NAND gate with higher speed or reduced propagation delay having static substrate biasing and dynamic substrate biasing.

II. Review

In [2], arrays of NAND, NOR, S-R latches and current mirror were fabricated on a cleaned, polyethylene naphthalate substrate. Fig 1 shows all the logic gates that are made and characterized. One may get the inverter function by connecting the two inputs OTFT of NAND to the ground.

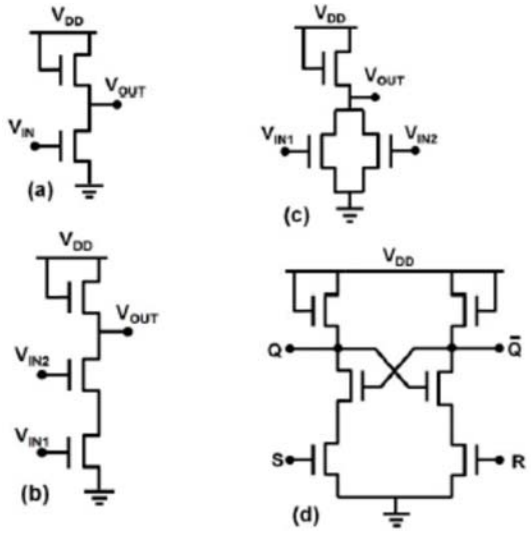

Fig. 1 (a) Inverter (b) NAND (c) NOR (d) S-R latch

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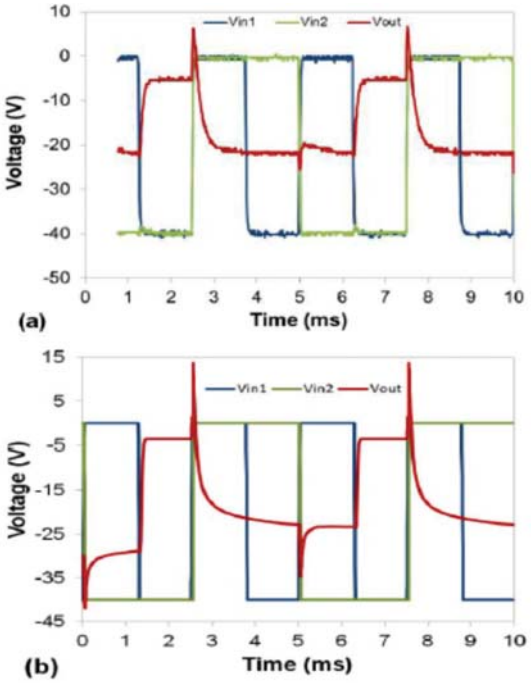


Fig. 2 (a) experimental response (b) simulation response of NAND gate. Vin1 and Vin2 are at 400Hz and 200Hz respectively

Fig. 2 shows the response of NAND gate when the square input signal is given to two input i.e. Vin1 and Vin2. Vin1 is at 400Hz and Vin2 at 200Hz. Output voltage is respecting the truth table. The theoretical and experimental simulations resemble each other. It is demonstrated successfully that NAND made using R2R compatible vacuum-evaporation process, shows a path of fabricating more complex logic circuit.

In [3], they had performed mixed mode circuit simulation of logic gate, to predict dynamic performance of the circuit (Fig. 3). Fig. 3a shows the NAND gate output for the $C_L$in the range from 10^{-16}F to $5X10^{-15}$F. The calculation of delay for nand gate was at 50%Vdd for $C_{L=}10^{-16}$F and is 31ns for following transition and 9.7ns for rising transition. Fig. 3b shows xor gate results for all input configurations and C_L range is same as for the nand gate.

In [4], they have proposed glitch free NAND based digitally controlled delay line and is shown in Fig. 4. In this, gates with D written, represent dummy cells. Dummy cells are added to balance the load. In accordance with the chosen control bit encoding, each delay element may be in any of the three states.

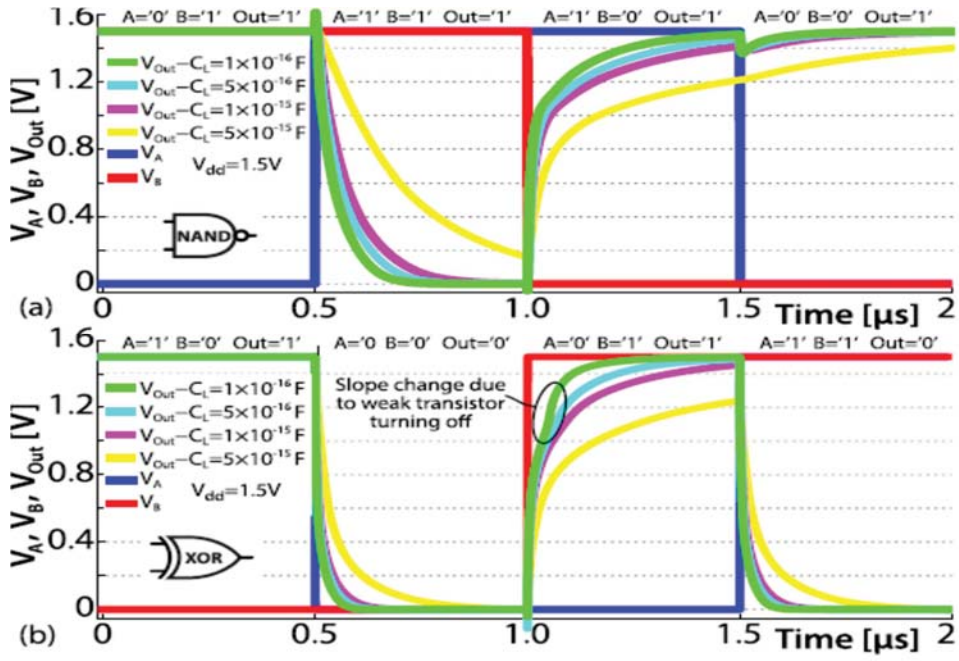


Fig. 3 Four transistor transient simulation (a) NAND gate and (b) xor gates with 1ns input rise and fall times

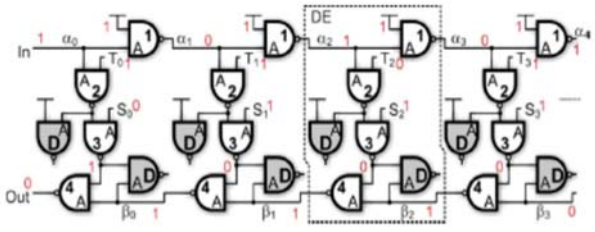
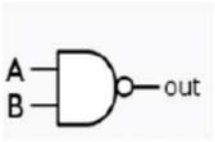


Fig. 4 Glitch free NAND based DCDL (topology-inverting)

In [5], organic NAND gate is fabricated. Transistors fabrication is done on 125 µm thick polyethylene naphthalate substrate. A 30mm gold source or drain layer which is also a first level connection, is fabricated by laser ablation. The fabrication and electrical measurements are done in air. There was no sample conservation. A NAND gate is made and simulations were done by the same technological steps. Fig. 5 (a) is the electrical symbol of NAND gate and Fig. 5 (b) is the truth table of NAND gate.



(a)

A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

(b)

Fig. 5 (a) Electrical symbol of organic nand gate (b) Truth table of NAND gate

Fig. 6 (a) shows the logic diagram and Fig. 6 (b) shows the microscopic image of NAND gate. Pull up network is made of 2 organic transistors in parallel and pull down network is made of N organic transistors in series. The total area of this NAND gate is 4.3X3.0mm^2. To characterize it, electrical DC measurements have been done.

Initially a DC sweep is applied to 'A' input, with Va voltage varying from -20V to +20V with step of 400mv.The V_B (set to '1') is given Vdd voltage. V_B is also given '0' logical voltage which was V_{SS}.

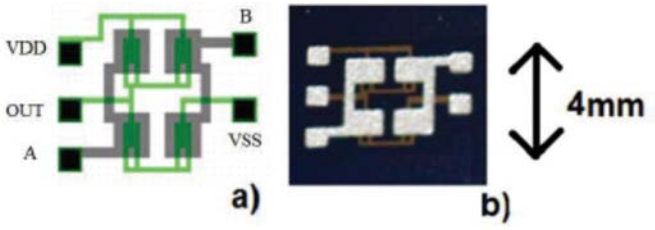


Fig. 6 (a) Layout of organic nand and (b) Microscopic picture of NAND gate

Fig. 7 shows the output voltage when V_A is varying. Fig. 7 shows that the truth table of NAND gate is followed. Good matching is seen between the measured characteristics and simulated one. Simulated and measured offsets are both at 5V. Voltage gain during switch is 27db. In this 100th measurement is compared with the average standard measured curve as shown in Fig. 9 so as to show the reliability of the model and the robustness of the manufactured circuit. In Fig. 9, the input voltage is varied from 0V to 16V so as to focus on switch area.

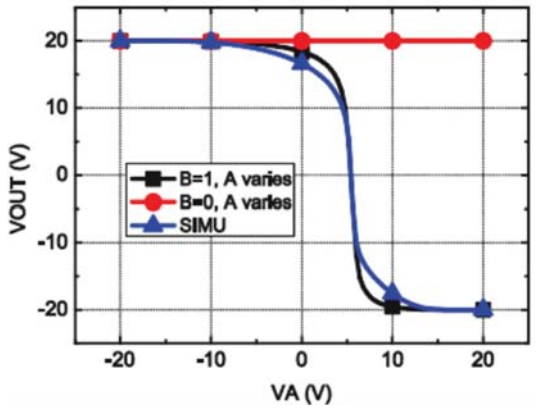


Fig. 7 Transfer characteristics of NAND (organic). Measurement and simulation comparison

Fig. 8 depicts that the 1000th measured offset is shifted a bit when compared to the first measured graph. The offset of 5V is low and the organic NAND respects the truth table even if the 5V offset is increased after many measurements.

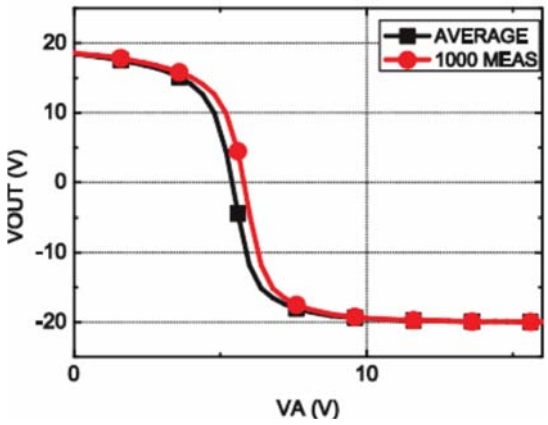


Fig. 8 Comparative analysis between average measurement and 1000th measurement of the transfer characteristic of NAND

In this paper, NAND gate's frequency is also researched. Initially 200Hz square wave is applied, which switches from Vss to Vdd on one of the input of NAND gate. The other input is set to Vdd. Fig. 9 shows the input and output voltages. From the graph, one can see that the output signal is well inverted signal of input voltage. 450Hz was the maximum operating frequency. NAND gate is not very fast for the higher frequency input signal.

In [6], they have reported a high performance printed flexible complementary circuits with p and n type polymer semiconductors. At the semiconductor dielectric interface, P and N type charge transport was controlled by a high –k polymer dielectric blend. Well balanced electron and hole mobility values are shown in both p type and n type organic field effect transistor (~0.5cm^2/V.S) and they have shown a low V_{th}, which resulted in the development of inverters and various gates including NAND logic gate. Fig. 10 shows the out waveforms for given inputs.

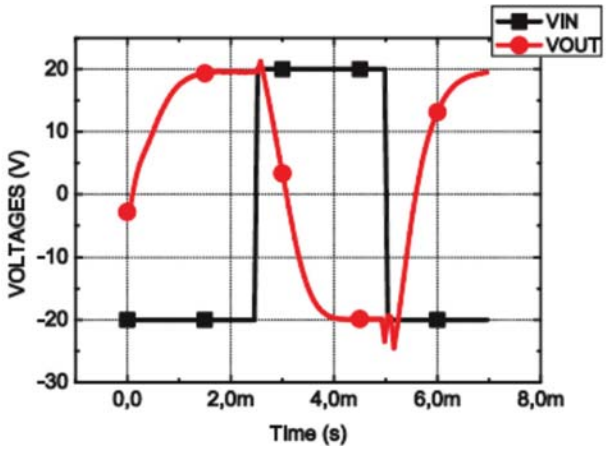


Fig. 9 Square wave input and Nand response

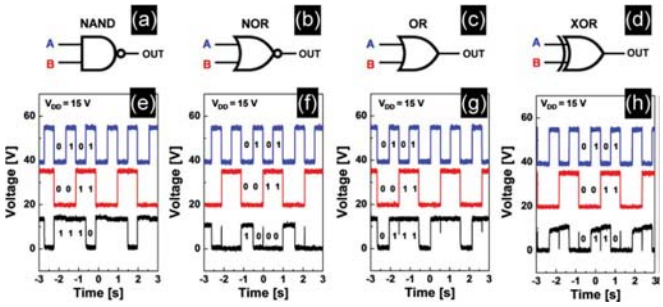


Fig. 10 Output waveform for two inputs (in blue and black) of nand, nor, or and xor gates

In [7] the drain to source voltage of individual transistor is 5V, V_{th} is 0.2V, and 190mv/dec is the subthreshold slope. More than 10^8 is the on/off current ratio and 14cm^2/v.s is the saturation field effect mobility value that was measured. Gate leakage limits the off state current to be less than 1PA.

The NAND gate was fabricated by two series connection of driver transistor and a load transistor. The performance of NAND with DC voltage and dynamic input waveform were characterized. Fig. 11 (a) shows the DC transfer curve for β=40 nand gate. This NAND gate shows the steep transfer characteristic for Vdd from 1V to 20V. According to the truth table also, when one of the input (V_A) is low, the output was at 4.9V. When the input V_A is high by making it equal to V_{DD}, this NAND gate became an inverter.

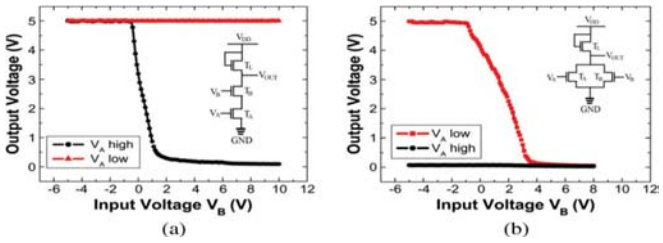


Fig. 11 Schematic and VTC of (a) nand gate w_{drive}/L_{drive}=200µ/20µ and (b) nor gate w_{drive}/L_{drive}=25µ/10µ

It was observed that NAND gate with smaller β shows the transfer characteristics which are shallower. The output voltage drops from 4.9V to a lesser than 1V. For the V_{DD}=5V when L_{drive}/W_{drive}=10µm/25µm and when Ldrive/ W_{drive}=10µm/400µm NAND output voltage goes down from 4.9V to lesser than 0.1V

The overlap of gate source/drain was 2.5 µm and 5 µm respectively. The greater the overlap (5 µm or so), the greater is the input capacitance. This resulted in a shallow transfer characteristic and also resulted in slow response speed comparatively. The dynamic performance of NAND gate was also tested. Input voltages V_a, V_b and supply voltage were given voltage of 10V. The output waveform of NAND gate is observed at frequency 100Hz, 1 KHz and 5 KHz and is shown in Fig. 12 (a).

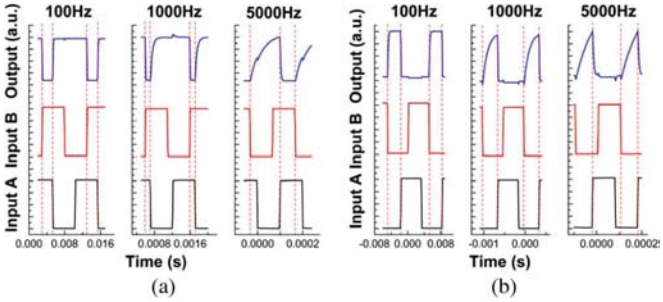


Fig. 12 Supply voltage vdd=10V and o/p waves (a) nand gate w_{drive}/L_{drive}==400µ/10µ (b) nor gate w_{drive}/L_{drive}==100µ/10µ

Operating frequency is at 100Hz, 1 kHz and 5 kHz as shown in Fig. 12. At frequency of 100Hz, the output waveform is steep or sharp with not much difference in rise and fall time. At 5KHz the rise time is 78µS and fall time is 8 µS. This shows that the limitation of circuit at high frequency is rise time or charging time. Charging time can be reduced by increasing the channel width of load transistor. Also by decreasing the capacitance of driver transistor, the charging time can be reduced. It was observed that by reducing the gate source or drain overlap and by decreasing the interconnect resistance, we can reduce RC time constant and hence increase the operating speed.

Fig. 13 [8] shows the NAND gate. This NAND gate can have 2xVdd tolerant capability. The Mp transistor and Mn transistors with Vdd of gate voltage also conduct logic level to the output and hence can avoid overstress issue of gate oxide. Function of logic gate is defined by Mpp1, Mpp2, Mnn1 and Mnn2.

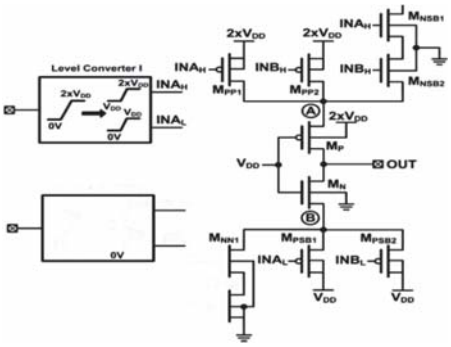


Fig. 13 2xvdd capability of tolerance of nand circuit

When the pull low and pull high path is switched off. Mpsb1, Mpsb2, Mnsb1 and Mnsb2 bias the source voltage of Mp and Mn at a voltage of Vdd. If the logic gates have two or more inputs, the source biasing devices must have complementary structure, in order to have the correct logic operations. With input IN_A and IN_B having opposite logic signals and pull low path is off, node B may be biased to safe voltage V_{DD} by M_{PSB2} or M_{PSB1}. Fig. 14 shows simulated voltage waveform of 2XVdd NAND gate.

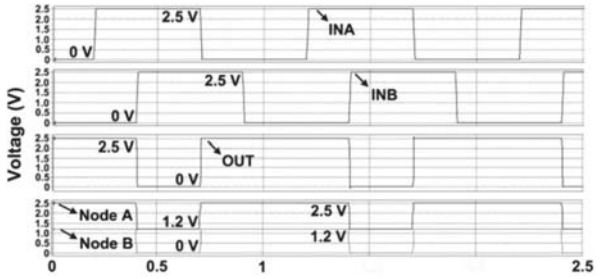


Fig. 14 Waveform of nand simulation with signal level of voltage at 2.5V, which is 2.5xvdd

In [9], four logic gates are used and they are NOT, nand, nor and xor gates. Simulation temperature is set at 27ºC with process in TT region. NOT and NOR gate width is set at 200nm and NAND gate and XOR gate width is set at 400nm.Channel length of MOS transistors are set at 100nm, 200nm, 300nm and 400nm.

When operating voltage is varied from 0.3v to 1v, they design best width of pmos in which transitional voltage is half of operating voltage.

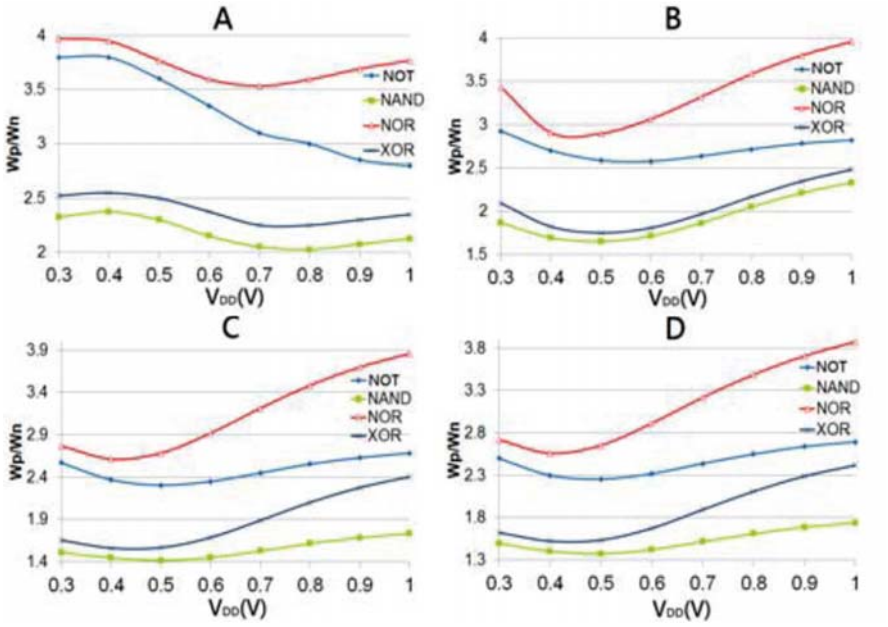


Fig. 15 Wp/Wn of xor, nor, nand and not gates at (A) L=100 μ (B) L=200 μ (C) L= 300 μ (D) L=400μm

Fig. 15 shows the variation in size ratio with variation in supply voltage. So this paper analysis the characteristics of cmos (static) logics and give width size ratio Wp/Wn under PVT variations in 90nm cmos process. Under very low voltages, the threshold voltage of transistor is affected under process, voltage and temperature variations.

This paper [10] shows the time efficacy using feedback control method on NAND and NOR gates. These gates have 2 and 3 fan ins respectively. Using this feedback control technique, the NAND and NOR gates showed the better performance and better power/energy dissipation and consumption. This paper shows an automatic way for building gates. The NAND gate with various fan ins showed the better performance as well as better power/energy compared to traditional ones. In few iterations only the sizing of gates was done. In conventional sizing exhaustive search is done. This gate sizing method could be used for FINFET also.

III. Implementation

Fig. 16 is taken from [11] and Fig. 16 (a) is conventional NAND gate. The nand gate of Fig. 16 (b) is taken and the simulation of this circuit is done with normal reverse substrate biasing. Dynamic circuit operates in two phases. They are precharge and evaluation phase. During precharge, the output of a circuit is precharged to a specified level. When the evaluation of the circuit begins, the output node may stay at the precharged level or go into the opposite level. It is required that the transition between the two level be glitch free as there is dynamic voltage on the output dynamic capacitance. This is opposite to what happens in the static gates, where continuous DC restoration is provided.

In data driven dynamic (D3) logic, precharge and evaluation happen in the same fashion but there is no clock signal. Data signal replaces the clock signal. This data, replacing the clock signal could be single datum or two or more data signals. In the conventional dynamic logic, one of the PUN or PDN is removed. With this circuit inputs go through the certain conditions. In the domino logic, all the inputs must be kept low during precharge phase. So the need of clock signal can be removed, if we can precharge the output node with the help of input signal or combination of input signals. The circuits, in which input data signals precharge the output node, are called data driven dynamic logic or D3 logic. Thus D3 logic is not precharged by clock signal as it happens

in dynamic logic but by input or combination of input signals [11].

For nand gate, the clock of Fig. 16 (a) is removed by one of the input signal as shown in Fig. 16 (b).

Propagation delay is measured at supply/2 voltage level of 0.9V. Supply voltage is 0.9volts. Also average power is measured and the results are put in row1 of Table I.

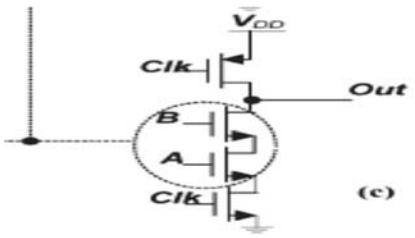


Fig. 16 (a) Dynamic nand

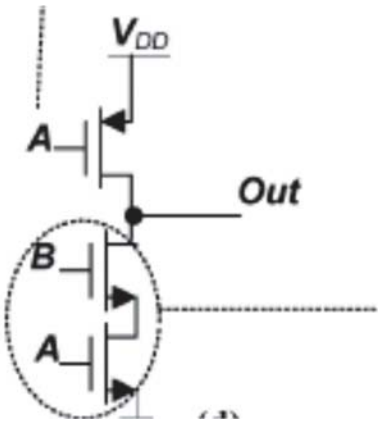


Fig. 16 (b) D3nand

The row2 of Table I shows the same parameter but with static forward substrate biasing of vdd/2. The forward static body biasing results in reduced propagation delay as well as the reduced power delay product. The third row shows the same circuit but with substrate body connected to the input, which results in dynamic body biasing. This dynamic body (substrate) biasing results in shorter propagation delay although the average power is increased. Hence this data driven dynamic NAND gate finds its application, which requires high speed with a penalty of high power consumption but no increase in area.

TABLE I
PROPAGATION DELAY AND AVERAGE POWER OF D3NAND GATE

	Propagation delay (10^{-10}Sec)	**Average power (watts)**
D3nand with normal reverse body bias	2.9535	$1.6064X\ 10^{-6}$
D3nand_static substrate bias of Vdd/2	2.4881	$1.4850X\ 10^{-6}$
D3nand_dynamic substrate bias	2.1755	$7.2788X\ 10^{-3}$

IV. CONCLUSION

The data driven dynamic NAND gate with dynamic substrate bias has the shortest propagation delay time and is reduced to $2.1755\ x10^{-10}$ Sec compared to propagation delay with normal reverse body bias of $2.9535\ x10^{-10}$ Sec. Also it is reduced from $2.4881\ x10^{-10}$ Sec of propagation delay with static forward body bias to a value of propagation delay of $2.1755\ x10^{-10}$ Sec where dynamic substrate biasing is applied. Hence, dynamic body biasing of data driven dynamic (D3) NAND gate finds its application where power penalty is acceptable for a high speed with no change in the area. D3 nand itself has low area compared to static NAND and dynamic nand. The 22nm HP ptm models are taken from Arizona State University, USA and hspice simulations were done.

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