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# Monitorization of Junction Temperature Using a Thermal-Test-Device

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***Abstract*—**Due to the higher power loss levels in electronic components, the thermal design of PCBs (Printed Circuit Boards) of an assembled device becomes one of the most important quality factors in electronics. Nonetheless, some of leading causes of the microelectronic component failures are due to higher temperatures, the leakages or thermal-mechanical stress, which is a concern, is the reliability of microelectronic packages.

This article presents an experimental approach to measure the junction temperature of exposed pad packages. The implemented solution is in a prototype phase, using a temperature-sensitive parameter (TSP) to measure temperature directly on the die, validating the numeric results provided by the Mechanical APDL (*Ansys* Parametric Design Language) under same conditions. The physical device-under-test is composed by a Thermal Test Chip (TTC-1002) and assembly in a QFN cavity, soldered to a test-board according to JEDEC Standards. Monitoring the voltage drop across a forward-biased diode, is an indirectly method but accurate to obtain the junction temperature of QFN component with an applied power range between 0,3W to 1.5W. The temperature distributions on the PCB test-board and QFN cavity surface were monitored by an infra-red thermal camera (Goby-384) controlled and images processed by the *Xeneth* software.

The article provides a set-up to monitorize in real-time the junction temperature of ICs, namely devices with the exposed pad package (i.e. QFN). Presenting the PCB layout parameters that the designer should use to improve thermal performance, and evaluate the impact of voids in solder interface in the device junction temperature.

***Keywords*—**Quad Flat No-Lead packages, exposed pads, junction temperature, thermal management, measurements.

## I. Introduction

THERMAL design of PCBs in electronic systems is an important concern for designers, because the more power a device consumes more heat it generates. A dilemma for designers is how to fit in all the market demands without exceeding power budgets and maintain device operating temperatures below the specified limits [1]. Furthermore, the IC geometries are shrinking and densities increasing, with power management being increasingly difficult [2]. With a large number of devices dissipating power in many of today's electronic systems, detailed numerical simulations can predict the temperature rise using CFD-based (Computational Fluid Dynamics) tools that became essential in thermal management [3]. Although the predictions from full-field CFD simulations are accurate, the computational cost and model generation time can be fairly high. Sometimes, it is preferable to use a quick estimation tools to design a preliminary layout of a PCBs with specific heat-dissipating components [2], [4]. Currently, the numerical simulations performed during thermal analysis demonstrate that an increase of 10°C degrade the performance of electronic components (IC) by more than a third. Therefore, it is desirable to observe the heat transfer phenomena in the design of optimized solutions for cooling and before a production process [3], [5]. The plastic packages with exposed pad form an important class of packages with the ability to dissipate higher-levels of power, requiring only a well-designed PCB for thermal management [6]. So, junction temperature depends on the copper coverage area available in the PCB, which presents lower temperatures when larger areas and free-air natural convection is available [7]. An economically efficient management of thermal properties is among the main priorities in the engineering of electronic components, with capacity to produce circuits with high functional characteristics and promoting heat dissipation, simultaneously [2], [7]. The inclusion of materials with better thermal conductivity will allow adequate heat dissipation.

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### *A. Junction Temperature*

Junction temperature is an important issue on the operation and reliability of an IC. Through the characterization and qualification, the manufacturers of components are able to understand the limitations of the component's performance and provide guidance to the user with the operating specifications [4], [8]. Each component is unique in its composition and function, thus the junction temperature ($T_J$) is the specification for maximum operation and this is critical, since semiconductor lifetime is inversely related to operating junction temperature [9]. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. Experimentally there are three methods for measuring thermal parameters in the die (silicon). The most reliable method requires a pro-active design to measure the junction temperature directly in the die, and includes a circuit with a temperature sensitivity element (TSP) in a known operation range [10].

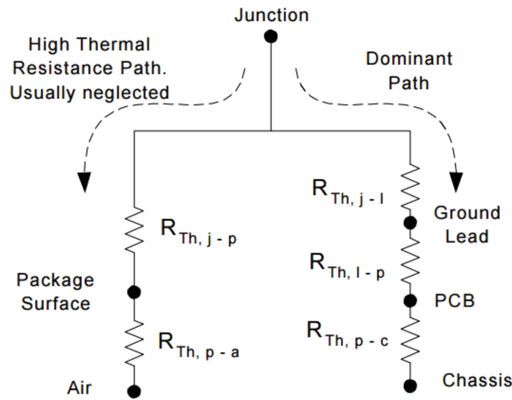


Fig. 1 Equivalent circuit for thermal resistance [11]

Fig. 1 illustrates heat being transported through two paths, the first path through the mold compound by conduction, and then to the air surrounding the package by convection. Most of the die's thickness is to provide mechanical support for the very thin layer of active components on its surface. The second path, the heat flows from the junction of the device through the lead and through the PCB, into the chassis by conduction and finally to the air surrounding [11]. However, major of heat generated in the device transports through second path. This model assumes that the die's temperature is uniform across its top surface, ignoring the fact that x-axis and y-axis thermal gradients always exist and can be large during high power conditions. Furthermore, analyzing gradients at the die level always requires modelling tools or very special empirical technique [10].

### *B. Pro-Active Design for Real-Time Measurements*

As mentioned, the most reliable method is measure the junction temperature directly in the IC, displaying the temperature during operation using a *thermal test chip* – from TEA. The method for semiconductor thermal measurements relies on the ability to measure the TSP element of device-under-test (DUT), with a parasitic device (e.g. substrate isolation diode, input protection diode, output steering diode, among others) [4], [9]. The temperature affects every semiconductor device, and diodes are no exception.

The electrical test method for diode thermal measurements uses a three-step sequence of applied current levels ($I_M$) to determine the voltage ($\Delta V_F$) changes in a p-n junction. Since, the junction temperature ($T_J$) starts decreasing immediately at the exact of applied power ceases. Such diodes make excellent temperature sensors at low values of forward current ($I_M$), with the junction forward-voltage [$V_F$] correlation which is linear to the second order. Thus, junction temperature produces a corresponding change in junction forward-voltage obtained by [13]:

$$K = \frac{\Delta T_J}{\Delta V_F} = \frac{T_{high} - T_{low}}{V_{high} - V_{low}} \qquad [^{\circ}C/mV] \tag{1}$$

where, the correlation factor ($K$) is highly dependent on the forward-bias current of the diode $I_M$. The value is typically in the range of 0.4 to 0.8°C/mV. Thus, $T_J = T_{Ji} + \Delta T_J$, wherein $T_{Ji}$ is the initial temperature at the junction of the diode [10]. According to JEDEC [13], the thermal resistance of a diode for a specific set of environmental and time conditions is obtained by: $\theta_J = \left[\frac{K \times \Delta V_F}{I_H \times V_H}\right] = \left[\frac{\Delta T_J}{I_H \times V_H}\right]$, with $\Delta V_F$ the changes in diode voltage when biased, and $I_H$ the heating current applied and corresponding voltage applied $V_H$. Measurements can be adjusted during tests. Choosing a low value ($I_M$) will cause problems in measurement repeatability for a specific diode and potentially large variations between devices. On other hand, too large values of $I_M$ will cause significant self-heating within the diode junction area and give rise to a potentially large temperature measurement errors [14]. The difference across the p-n junction ($v$) operate within its linear region, at different forward currents which changes with temperature described in two different ways [14]:

$$v = \frac{k_b T_J}{q} \ln\left(\frac{I_M}{I_s}\right) \tag{2}$$

$$T_J = m.v + T_0 \tag{3}$$

where, $m$ is the slope equation of junction temperature as function the diode forward-voltage ($v$), that is read and recorded once the environment temperature has stabilized, which occurs when neither the diode voltage nor-environmental temperature measurements show any significant fluctuations. Furthermore, the average value and standard deviation of $K$ values provides a measure of sample uniformity. If the ratio of standard deviation to average $K$ is less than 0.03, then industry practice dictates that the average $K$ can be used for all the devices [13].

### *C. Heat Dissipation in Exposed Pad Packages*

An integrated circuit consists of a small block (die) of a semiconductor material (silicon), in which the desired functionality is implemented. This block is integrated in a body (package) that provides mechanical integrity and interface (e.g. leads) that allows its link with other electronic components through the printed circuit board (PCB). In turn, die pins are connected to the terminals of the package through the small wires (bond wires) with very low heat resistance [2], [15] (Fig. 2).

Due to excellent thermal and electrical characteristics, the packages with exposed pad were introduced in the late 80s. Comprising an integrated circuit bonded to a metal pad and exposed on the bottom face of the package. Subsequently, the assembly is encapsulated in a polymeric material - mold compound. Despite its advantages, such packages suffer major thermal and mechanical problems related to reliability problems. These problems are mainly due to differences in thermal and mechanical characteristics of the various materials involved, such as thermal expansion coefficient differences

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among others [17]. The amount of heat dissipation needed for a design depends on the IC dissipated power and densities, the ambient temperature, on the PCB geometry and their material properties, and finally in the amount of airflow or forced air.

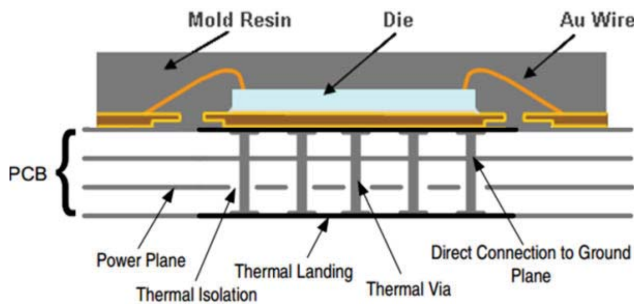


Fig. 2 Cross Section of a QFN Package and PCB [16]

The power consumed by an integrated circuit is dissipated on the surface of its die in the form of heat, rising up the semiconductor junction temperature. For a semiconductor device, thermal resistance indicates a steady state that increase of semiconductor junction temperature over a given reference, for every unit of energy (heat) dissipated on the surface of its die ($P_{diss}$) [18]. Thus, the junction-to-ambient equivalent thermal resistance can be expressed as [10]:

$$_{\text{JA}} = \frac{\Delta T_{JA}}{P_{diss}} = \frac{\left(T_j - T_A\right)}{P_{diss}} \quad (4)$$

*D.Impact of Voiding Phenomena and PCB Design on Thermal Efficiency*

The maximum junction temperature is a limiting worst case that should not be exceeded, which should be guaranteed by ensuring a significant margin of safety. With regard to the relationship between the junction temperature and the useful life of the component, this can be exemplified as a particular case in which a junction temperature that is 15°C higher results in a FIT rate (failure in time) increased to double [18]. In the market there are cost-efficient solutions, and optimal thermal characteristics.

The exposed pad at the welding has to find a compromise with respect to the solder volume, as large volumes facilitate the heat conduction, which translates into a short-circuit increase. However, for low volumes of solder, the short circuits are eliminated but cast doubts on the heat dissipation efficiency or reliability (fatigue caused by thermal cycling, vibration and shock). The optimization process is to define the parameters that maximize the transfer phenomena, which gives a proper system configuration that is thermally and reliability improved. Same methodologies are presented and compared by [3]. Husain and Kim also used the methodology based on GA (Genetics Algorithms) to search the optimal solutions and avoid numerical costs [5].

JEDEC has recently established a set of standards for measuring and reporting the thermal performance of IC packages. These standards fall under the EIA/JESD Guidelines [19]. Since $\theta_{ja}$ (junction-to-ambient thermal resistance) is not a constant, but it is critical to determine the standards that were used to measure $\theta_{ja}$ before attempting a comparison.

The chip or die pad inside a package can perform the same function as a heat spreader if the chip or pad is large enough. The function of the heat spreader is two-fold. First, it spreads energy from the hot-spot of the chip over a wider area on the package's surface, thereby increasing convective energy loss. Second, it increases heat transfer from the pad to the lead fingers or to the package balls, which then conduct the heat to the PCB [4], [7]. Since the density, viscosity, and heat capacity of air change with temperature, so it should not be surprising.

The surface temperature of the device drives both convection and radiation energy loss from the package. The hotter the package surface gets, the more efficient convection and radiation heat loss to the ambient environment. Therefore, it is not surprising to note that $\theta_{ja}$ improves by about 3% when a package's power is doubled. For very low power dissipations, $\theta_{ja}$ is sometimes found to be two or three times higher than at rated package power levels [12], [13].

Exist several types of package with different geometric configurations, and impacts on the thermal performance. These can include the distance between the tips of the lead in the package and the die pad as shown in Fig. 3.

According to information provided by the EIA/JEDEC Standard, are considered the following factors impact on thermal resistance ($\theta_{ja}$) that lead to an increased thermal efficiency [10]:

- PCB Design: 100%
  - The increase of PCB layer (FR-4) leads to a decrease in thermal resistance ($R_{JA}$);
  - The increase of the copper layer (%) leads to a decreasing of thermal resistance ($R_{JA}$);
  - The decrease of PCB (FR-4) thickness leads to a decrease of thermal resistance ($R_{JA}$).
- Chip dimension or Pad: 50%
- Configuration package of internal geometry: 35%
- Altitude: 18%
- External Temperature: 7%
- Power dissipation: 3%

## II. Measurements of IC Junction Temperature Using a TTC

The aim of this paper is to give a short overview about standard thermal solutions, related to voiding phenomenon which occurs within solder interface underneath exposed pad of BTC (Bottom Terminated Components), such as QFN (Quad Flat No-lead) and an experimental way to measure junction temperature. The discontinuity in solder interface under exposed pad caused by voiding raises concerns related to reliability of a final product. In terms of thermal dissipation efficiency, there is no established acceptance criterion, since critical voiding level is application dependent, and is a topic of some speculations and discussions. There are situations for which acceptance criterion appears to be too much restrictive, but without benefits, causing unjustified production rejections.

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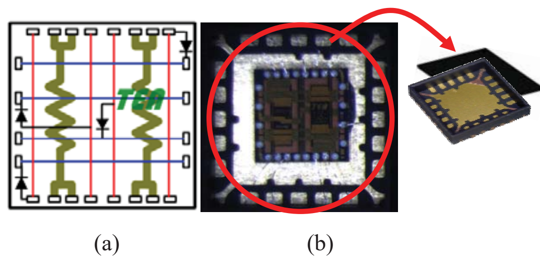
Within this motivation, was decided to conduct a study of the impact of solder discontinuity area and PCB design options in thermal efficiency.

*A. Assembly a QFN Test-Device and PCB Test-Board Configuration*

To understand the limitations of the component's performance is important measure the junction temperature at maximum operation. Experimentally there are three methods to measure the thermal parameters in a die (IC). The most reliable method is measure the junction temperature directly in the IC, displaying the temperature during operation using a thermal test chip (TTC-1002) as presented in Fig. 3 (a). QFN test device were created through a die attach and wire-bond process between the die (TTC-1002) and the inner surface of the pad exposed.



(a) (b)

Fig. 3 (a) Schematic of Thermal Test Chip (TTC-1002) used to create QFN test-device [20], (b) Wirebond and die attach process between the QFN cavity and TSP element (TTC-1002) cover with a flat after a cure process

The experimental tests were performed using a TSP (temperature-sensitive parameter) element as a direct measure of the temperature semiconductor, which is located at the die center (TTC-1002, from TEA), at opposite corners and in the middle of one side. Each thermal test chip has 2.54x2.54 mm, developed from the wafer of 152 nm and a thickness of 625 µm that possess Al-Si pads with dimensions of 166 µm [20]. Simultaneously, the thermal test chip allows control the dissipated power by the use of two power resistors (7.6Ω±10%) located near the center of the TSP, as can be observe in Fig. 3 (a). The assembled QFN test-device is composed by a TTC-1002 and a QFN open cavity (M-QFN20.65) with dimension of 5,0 x 5,0 mm, attached with thermal conductive adhesive (CW2000 - a nickel conductive pen). Connecting the QFN and TTC-1002 die pads with an aluminum alloy (AlSi-1%) bond-wires of 30 µm diameter [21]. And proceed with the junction temperature monitoring. Allowing an output of 6W individually when applying a potential of 6V and 1A at terminals, however the typical fusing limit current for each bond-wire is proximally 400 mA. We are able to control the power dissipation, and thus evaluate the junction temperature with four diodes existing in the QFN test-device. The final step, is cover the QFN cavity with an adhesive (LCA3000X) on the lid surface, through a curing process - during 60 minutes at 150°C and an applied pressure equal to ½ Lbs per square inch of bond area.

As shown in Table I, QFNs test-devices were solder in three different PCBs, each with a relative area of voids in solder interface, namely 10%, 40% and 70% of the device exposed pad area. The solder interface area was controlled using a solder mask layer over the copper layer of exposed pad: 3,25 x 3,25 mm in the PCB. After the solder process, an x-ray inspection was performed to all test-boards to determine the real percentage of voids induced in the solder interface. Obtaining values of: 17,6%, 51,5% and 75,8% for each case, as shown in Fig. 4.

TABLE I
PCB DESIGN AND VOIDS IN SOLDER INTERFACE

| PCB | Characteristics (PCB design) | Solder interface voids (%) | QFN Package Size (mm) |
|---|---|---|---|
| 1 | Top/bottom layer (copper): 60,7mm Exposed pad: 3x3mm with 4 thermal vias | 10 | |
| 2 | | 40 | 5 x 5 |
| 3 | | 70 | |

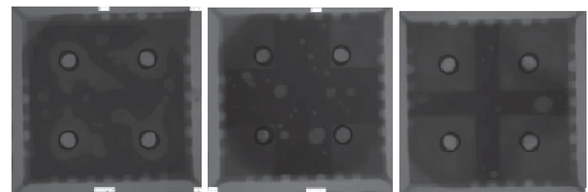
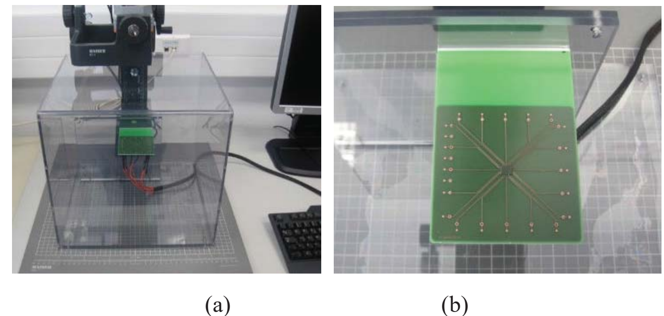


Fig. 4 X-ray inspection for solder interface between PCB and the QFN test-device (exposed pad) of three configurations of voids area in solder interface (10%, 40% and 70%)

In Fig. 5 is observed a PCB test-board and test enclosure used in experimental measurements of junction temperature ($T_J$), according to JEDEC Standard Guidelines. As a basic configuration, with a low effective thermal conductivity board is considered with four thermal vias, described in JESD51 [22].



(a) (b)

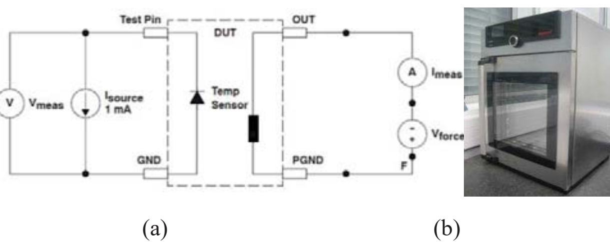
Fig. 5 (a) The test enclosure, fixture assembly and IR camera for thermal measurements and b) PCB test-board with a QFN test-device, according to JESD51 Guidelines

The enclosure is a box with nominal dimension of 305 x 305 x 305 mm as shown in Fig. 5 (a). Sealed to ensure no airflow through the enclosure and shelf-constructed of low conductivity material (polycarbonate - 0.11 W/mK). The package is positioned in the geometric center of the chamber by adjusting the position of the support structure constructed also in a low thermal conductivity material (less than 0.5 W/m.K). Furthermore, the increase the size of the box should be considered, if ambient temperature rise above the initial ambient temperature is 10% or more of the rise in junction

temperature during the test ($\Delta T_j$). Additionally, if the room in which the testing occurs suffers drastic temperature changes (> ±3ºC) a large box over the test enclosure should be considered. No structure above the package and board that is being tested to avoid disturbing the convection (< 2% change in the measured thermal resistance). The board is horizontal within ± 5 degrees and thermally insulated from the board. Considering a thermocouple placed 25 ± 5 mm below the bottom plane of PCB test board and 25 ± 5 mm from the side wall. The room ambient temperature is according to JESD51 (conducted in an environment between 15ºC and 30ºC) during thermal measurements [22].

*B. Experimental Set-Up for Junction Temperature ($T_J$) Measurements*

Experimentally there are three methods to determine the thermal parameters of an IC. However, the most reliable method is measure the junction temperature ($T_J$) directly in the die (silicon part of IC). Requiring a proactive design, that includes a circuit die with temperature sensitivity element in a known range of operation (Fig. 6 (a)). This setting allows one to display temperature during operation.




(a) (b)

Fig. 6 (a) Schematic for a direct measure of junction temperature using a TSP element and (b) Memmert UN55 oven used to obtain the correction factors of the p-n junction.

As shown in the above scheme, the diode acts as a temperature sensor - monitoring the voltage drop across the p-n junction ($v$) when directed polarized with a saturation current ($i_s$). Through the Shockley equation, we are able to determine the diode current as a function of temperature [13]:

$$i = i_s\left(e^{\frac{v}{nV_t}} - 1\right) with\ V_t = k_b / qt \tag{5}$$

with $V_t$ the thermal voltage having a typical value of 25.85 mV at room temperature, which varies depending on the temperature ($t$) of the p-n junction with $k_b$ - Boltzmann's constant, and ($q$) the elementary charge of electron and ($n$) the emissivity coefficient, which depends on the manufacturing process and the semiconductor material (typically n = 1). Since the saturation current is given by:

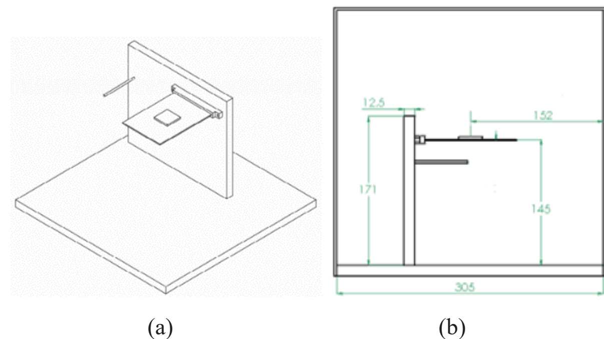
$$i_s = qA\left(\sqrt{\frac{D_p}{p}}\frac{n_i^2}{N_D} + \sqrt{\frac{D_p}{n}}\frac{n_i^2}{N_A} + \right) \tag{6}$$

with ($A$) the interface area, $D_p$ and $D_n$ are the diffusion coefficients of the positive and negative charges respectively, with $N_D$ and $N_A$ the donors and acceptor concentrations in the $n$ and $p$ side of the semiconductor material. Assuming an intrinsic concentration of the charges ($n_i$) with $\tau_p$ and $\tau_n$ the charge lifetimes.

Additionally, measuring the temperature at the package (case) surface allows estimate the junction temperature during operation. In this context, the temperature in the case can be measured using an infrared camera (IR) Gobi-384, depending on the accuracy required. When the component is measured at the top, the junction temperature can be calculated using (7) [10]:

$$T_J = T_C + \Psi_{JT} * P_{diss} \tag{7}$$

where $T_j$ and $T_c$ is the junction temperature and temperature at the top center of the package. And $\Psi_{JT}$ is the junction-to-top center-of-package thermal characterization parameter. Where $\theta_{JT}$ assumes that all devices are dissipating power from the top of the package, but in fact most of the power is conducted to the PCB, according to JEDEC standards.




(a) (b)

Fig. 7 Test enclosure and fixture assembly for diode for measurements (JESD51).

To determine the correction factor of the p-n junction - the TSP element, was need to impose different temperature conditions to the device using a *Memmert* UN55 oven in the laboratory tests (Fig. 6b). Enabling a constant and stable temperature to monitorize the junction temperature in different environmental conditions, namely up to 100°C. Thus, measurements were carried out to find the linear correlation coefficient between the p-n junction voltages subjected to a temperature range between $T_{amb}$ = 25°C and $T_{max}$ = 100°C. Applying to the diode a constant current, equal to 1 mA and measure the voltage drop for a stable temperature reached in the Memmert-UN55, considering different levels of temperature, namely 25ºC, 50ºC, 75ºC and 100ºC. The oven as a *setpoint* resolution between 0.1 and 99,9ºC and with dimensions of 40x40x33 cm of steel, has a Pt100 temperature sensor (DIN class A 4-wire-circuit) and thermal behavior calibrated up to 160°C.

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*C. Numerical Analysis Tool for Thermal Evaluation of QFN Devices*

The present article shows a study of thermal behavior components with exposed pad, depending on printed circuit board (PCB) design and solder interface between the exposed pad and PCB. For this propose, a simulation tool developed by our group is used to evaluate the thermal behavior of QFN components [24]. This cost effective tool can be adopted by PCB developers as a day-to-day support tool requiring a minimum of learning effort by the user, and provides simulation results in a short time. The implemented simulation model is based on commercial finite element method, through creation of ANSYS Parametric Design Language (APDL) script and optimized in terms of trade-off between speed and accuracy. It is fully parameterized, which allows the user modify the PCB and component dimensions, number of copper layers and their thickness, number and dimensions of thermal vias, voiding level in solder interface, among others.

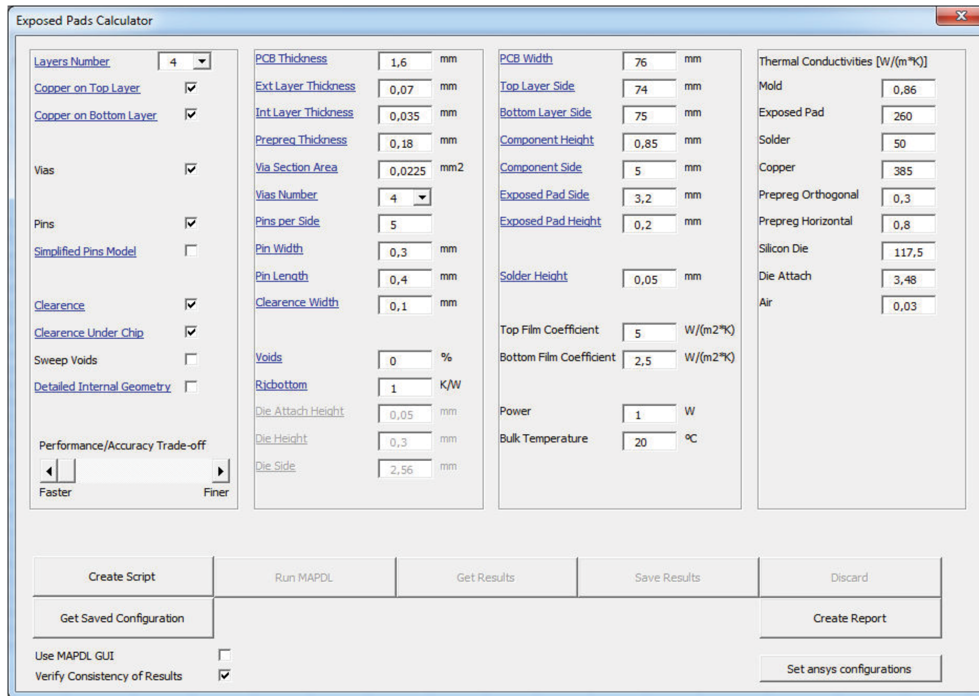


Fig. 8 A user-friendly interface in *VBA*

The implemented solution is experimentally validated. The APDL script allows its parameters to be defined from an external tool through a graphical user interface (GUI) implemented using Excel Visual Basic (*VBA*) programming language. Hide the complexity of a finite element simulation process, and allow the introduction of the parameters in a convenient and secure way. The created model comprises a regular QFN component, a solder interface and a PCB. The QFN component is in the center of a square PCB, and taking advantage of the symmetry model only a quarter of the model is simulated, making the simulation process faster.

The mathematical model and the respective simulation process are defined and controlled through a set of parameters grouped into five subsets. The largest subset consists of chip dimensions of PCB, quantities of thermal vias and copper layers, etc. The same subset also defines the test and boundary conditions. Enabled the construction of geometric model or introducing the thermal parameters, the assignment of materials, the definition of density of finite element mesh and mesh creating. The properties of materials are also defined in a separate group of parameters.

The heat is generated inside electronic component (Joule effect) and it is transferred to the environment through dissipation paths. The heat transfers by conduction in solids and by convection from the top and bottom of the PCB towards the environment, with heat generation rate [W/m$^3$] applied to the silicon die. The convection coefficients and room temperature are defined on the top and bottom sides of the PCB. Additionally, the post-processing step consists of the extraction of results to be sent to GUI (written to the file results.txt), with the temperatures of the nodes located at the point which for used border conditions must contain the highest temperature.

The numerical simulation input parameters are presented on the configuration interface, Fig. 8. It was considered a QFN20-5x5x0.85 mm component with an exposed pad of 3.2x3.2x0.85 mm. The PCB has a thickness of 1.6 mm, with four copper layers and 76mm wide. For the parametric study, a thermal resistance $R_{JC\text{-}Bottom}$ = 1ºK/W was considered and a power dissipation equal to 1W. No voids were considered in the PCB with a solder interface height equal to 0.05 mm in a temperature environment of 20°C.

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## III. Results and Discussion

Mount a device package on either a JEDEC JESD51 or SEMI standard thermal test boards, provides a tool for validation of package thermal models. The uniform mounting configuration is used for comparing thermal data between measurements made with the same device package or comparing thermal performance for different relative area of voids in solder interface with numeric results.

The challenge is study a practical case; reproduce the test-conditions and present an experimental way to characterize the thermal behavior of QFN package submitted to different power levels. As well as, make comments on relevant statements, based on the knowledge and experience acquired during tests and parametric studies. Presenting a short overview about standard thermal solutions related to voiding phenomenon and impact of PCB design options through a parametric study.

### *A. Comparison of Experimental and Numeric Results*

The air flow in natural convection is unstable, and more when the device surface is at high temperatures and power levels. The junction temperature measurements ($T_J$) were performed in the both QFN test-device, which are suitable to validate simulations due to known internal geometry, its uniform power dissipation (through resistors) and with diode(s) specially positioned in different location. Finally, is easily to put in functional conditions, monitoring in real-time the junction temperature. After reach the steady state, the TSP values were recorded, namely the heat voltage ($V_H$), the current ($I_H$), the time needed to reach the stationary state ($t_{Hss}$), and the ambient temperature at the end of experimental tests ($T_{Ass}$). Wherein the junction-to-ambient resistance is described by [25]:

$$\theta_{JA} = \frac{\left(T_{A0} + \Delta TSP \times K\right) - T_{Ass}}{P_H} \qquad (8)$$

with $T_{A0}$ the initial air-temperature before apply the heating power and $T_{Ass}$ the final air-temperature after steady state is reached. Additionally, the thermal dissipation analysis for different scenarios was also created by a simulation tool, reproducing the experimental conditions and assessing the impact on junction temperature for different contact areas between the exposed pad and PCB test-board.

As previous mentioned, test-boards were created with different configurations - inducing different percentages of voids, namely 10%, 40% and 70%. Thus, it is possible evaluate experimentally the impact of voiding phenomenon that occurs during the welding process. Start to describe the methodology used and the procedures for experimental measurements directly on the die - monitoring the voltage drop across the forward-biased diode according to the tests set by IC manufacturers (EIA / JESD 51-1) [23]. The procedures include the following steps to measures of $T_J$:

1. Carry out the thermal analysis in QFN test-devices considered that the package contains a die - thermal test chip (TTC-1002), allowing the power dissipation and junction temperature measurement on a printed circuit board according to the JEDEC Guidelines. To evaluate the worst-case heat flow condition;
2. The temperature in the thermal test chip/TSP element is calibrated and/or known;
3. QFN test-devices are submitted to a temperature-controlled environment - still air ($\theta_{JA}$). A sealed one-cubic-foot enclosure is used for this measurement, to insure that only natural convection cooling occurs;
4. The power dissipation in the QFN test-device is controlled and known. Obtaining an indirect reading of the temperature versus current applied to the device, or by controlling the current applied to the dissipation resistor will be possible to assess the diode voltage drop for the respective temperature, ensuring that the current through the diode remains constant during the monitoring;
5. Reaching a steady state, at the low temperature [$T_{low}$], near room temperature the junction temperature is measured, to check the linearity factor. After temperature is increased to a higher value [$T_{high}$] up to 100ºC, the stabilization is allowed occur. The heat generated internal to the semiconductor die propagates from the heat-producing junction, through the die, into the package, and finally into the test environment;
6. The difference between room temperature compared to the junction temperature measurement is determined, dividing by the power dissipated, giving the $\theta_{JA}$ value in °C/W. Thus a change in junction temperature produces a corresponding change in junction forward voltage obtained by: $\Delta T_{JA} = K.\Delta V_F$, where the correlation factor (K) is highly dependent on the value chosen for $I_M$. The units of K are in °C/mV and the value is typically in the range of 0.4 to 0.8°C/mV;

QFN test-devices are mounted in the test fixture into the temperature–controlled environment, which is connected to the measurement system, with QFN package positioned in the geometric center of the chamber by adjusting the position of the support structure. Once the heat generated internally matches the heat leaving the package (for some extended period of time - $t_H > 240$ seconds), a steady-state condition occurs and the heating curve flattens out. For most packages (≤40 mm square), $t_H$ is in the range of 3,0 seconds and usually adequate.

Fig. 9 shows high linearity between the temperatures applied to QFN test-devices and the diode p-n junction voltage for PCBs with different area of voids, presenting a diode temperature sensivity parameter around 0.56°C/mV.

The linearity factor is higher than one due to negative slope of the cooling curve, and the magnitude of the correction factor depends on the DUT, the test fixture and the inductance in the wires connecting the PCB test-board to the system.

The ratio of standard deviation to average *K* is less than 0.03, then industry practice dictates that the average *K* can be used for all the devices. Additionally, a low $I_M$ value will cause problems in measurement repeatability for a specific

diode and potentially large variations between devices. On other hand, too large values of $I_M$ will cause significant self-heating within the diode junction area and give rise to potentially large temperature measurement errors. For that reason, we apply a constant current of 1 mA across the forward polarized diode, which is recommended either by JEDEC and TEA. The diode forward voltage is read and recorded once the environment temperature has stabilized, which occurs when neither the diode voltage nor-environmental temperature measurements shows any significant fluctuations.

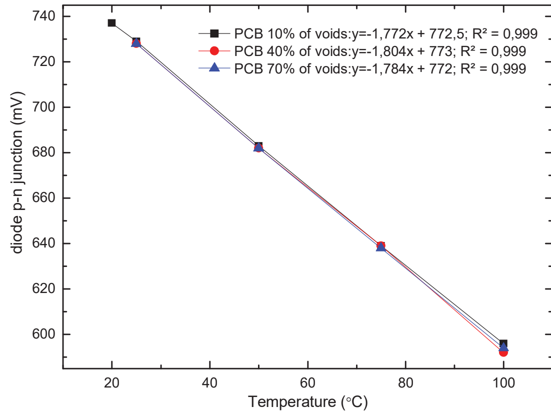



Fig. 9 Linearity of the correction factor (K) obtained for p-n junction of PCBs, submitted to temperature between 25ºC and 100ºC and a diode forward current equal to 1mA

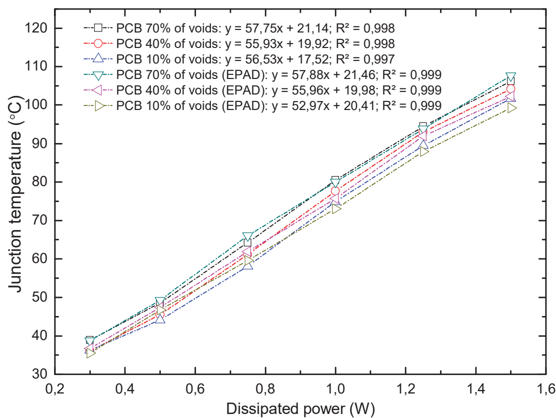



Fig. 10 Junction temperature obtained by QFN test-devices and simulated by the Exposed Pad Calculator for PCBs with 70%, 40% and 10% of voids

Fig. 10 presents the experimental and numeric results for junction temperature as function of power levels applied to QFN test-devices. Voiding phenomenon has no significant effect for areas smaller than 70%, as can be observed. A small temperature difference (less than 9ºC) is obtained between a PCB-1 with 17,6% and other with 75,8% (PCB-3) of voids in solder interface. Thus, we should beware these limits and considering the importance of the thermal paths, with the number of thermal vias and PCB copper layers, according to the PCB developer needs.

The offset value is obtained for each PCB which is related with the voiding level in solder interface, increasing the junction temperature (TJ) as the area of voids increases. A p-n junction has an inherent temperature dependency with diode forward-voltage ($\Delta v$), which provide a base for determine the junction temperature ($T_{JA}$) only while the diode is operating within its linear region and described by (9) [23]:

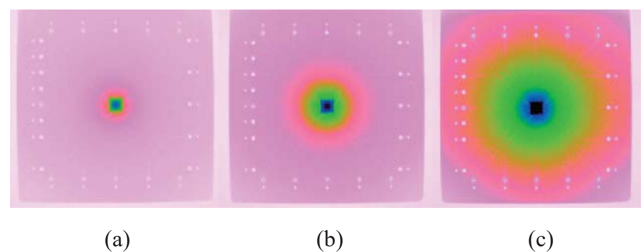
$$T_{JA} = q.\frac{v}{nk_b \ln\left(\frac{I_M}{I_s}\right)} \tag{9}$$

The diode forward-voltage ($v$) is read and recorded once the environment temperature has stabilized, which occurs when neither the diode voltage nor-environmental temperature measurements shows any significant fluctuations.

### *B. Thermal Measurements on QFN Test-Device Surface*

The temperature on the device surface is performed using an infrared camera (Gobi-384), as a function of the dissipated power controlled by a source current. The Gobi-384 camera allows detect temperature differences of 0.05 ºC during real-time image analysis calibrated to environmental conditions from -20°C to 120°C. With a minimum interest 32x32 pixel window (pitch of 25µm) and AD converter of 16 bits, a system that does not require thermoelectric cooling (TEC-less) and uses a lens with a focal length of 18 mm in the spectral window between 8 µm to 14 µm. This infrared camera is able to operate in an environment between 0°C to 50°C, capable of image processing through emissivity map corrections of the surface material. Although not required by the JEDEC standard, it sometimes advisable to monitor the thermal test board temperature either on the side-center package lead or on the board just at edge center of the package perimeter. The temperature can be used to compute a new thermal metric, $\Psi_{JL}$ (lead) and $\Psi_{JB}$ (board), which can be useful in estimating junction temperature for the chip/package combination in application environments.

Fig. 11 shows the measurements performed by an infra-red thermal camera for PCB-1 (with 10% of voids in solder interface) and images processed by the *Xeneth* software**.** The QFN test-device is submitted to power range between 0,3W and up to 1,5W, which reaches the steady-state. The enclosure environment is around 24ºC during the junction temperature ($T_J$) measurements.



(a) (b) (c)

Fig. 11 Thermal measurements performed by infra-red thermal camera (Gobi-384) on the PCB-1 surface during $T_J$ for a dissipated power of 0,5W, 1,0W and 1,5W respectively.

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As can be observed in Fig. 12, the temperature in the corner of the PCB-1 increases between 29,7ºC up to 42,2ºC when the temperature in the centre of QFN test-device changes between 41,9ºC, 70,4ºC and 93,6ºC, for each power level applied to QFN test-device. Comparing with the numeric values obtained for a case: 1) with a power level of 1,0W the junction temperature reach 72,1ºC and PCB corner temperature achieve 37,5ºC, 2) with a power level of 1,5W the junction temperature reach 99,3ºC and PCB corner temperature achieve 44,4ºC.

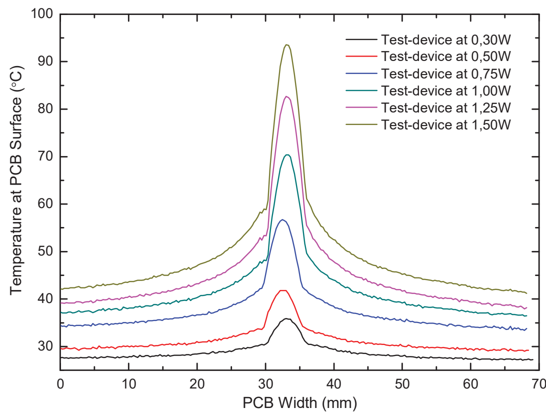



Fig. 12 Temperature profile obtained by infra-red thermal camera (Gobi-384) on PCB-1 surface for different power dissipated in the QFN test-device

*C. Parametric Study Using a Numeric Analysis Tool - Impact of Voids and PCB Layout*

To evaluate the impact of PCB layout parameters and voids presence in solder interface, a parametric study was performed using the "Exposed Pad Calculator" developed by our group and used to evaluate the thermal behavior of QFN components. The numerical simulation input parameters are presented on the configuration interface (Fig. 8).

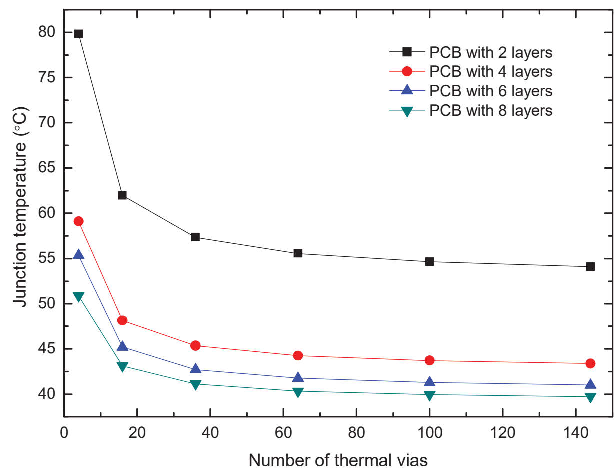
It was considered a QFN20-5x5x0.85 mm component with an exposed pad of 3.2x3.2x0.2 mm. The PCB has a thickness of 1.6 mm, with four copper layers and 76 mm wide. For the study, a thermal resistance $R_{JC\text{-}Bottom}$ = 1ºK/W was considered and a power dissipation equal to 1W. No voids were considered in the PCB with a solder interface height equal to 0.05 mm in a temperature environment of 20°C. With the increasing number of thermal vias, the dissipation path is optimized through the exposed pad into the PCB, leading to a decrease in the junction temperature and package surface. As shown in Fig. 13 (a), there is a reduction of 50% in junction temperature between a case with a PCB of two copper layers and 4 thermal vias under exposed pad and a PCB with eight copper layers and 64 thermal vias.

The influence of PCB width on thermal efficiency is observed in Fig. 13 (b), where is possible to compare the junction temperature with the PCB width, for a PCB without thermal vias and one with 16 thermal vias. Showing that number of thermal vias underneath the exposed pad has more impact in junction temperature than the increase of a square PCB between 55 mm to 135 mm.

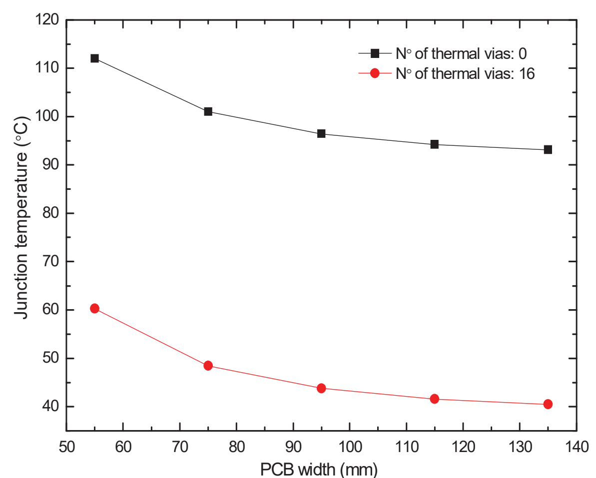
The parametric study is also focused on the assessment of thermal efficiency as a function of the sectional area of thermal vias (Fig. 14).

Considering a PCB with four layers and with 4 thermal vias, it is possible to optimize the thermal efficiency in 32% by increasing the sectional area from 0.006 to 0.067 mm$^2$. Compared with a PCB with 16 thermal vias the maximum optimization is around 20%.

As can be observed in Fig. 15, the impact of voids phenomenon that occurs during the welding process can be minimized by adopting thermal vias. The junction temperature analysis was performed for different areas of voids in solder interface - namely 0, 25, 36, 49, 64, 81% of area under the exposed pad by selecting the "void sweep" functionality. Considering a PCB with 16-thermal vias occur a thermal optimization of 18% and with 36-thermal vias the improvement is approximately 24% compared with PCB with 4-thermal vias. Shown a temperature increase of 3ºC when the percentage of voids reaches 81% of the area.




(a)




(b)

Fig. 13 (a) Junction temperature ($T_J$) as a function of thermal vias number for different PCBs and (b) influence of the PCB width in junction temperature

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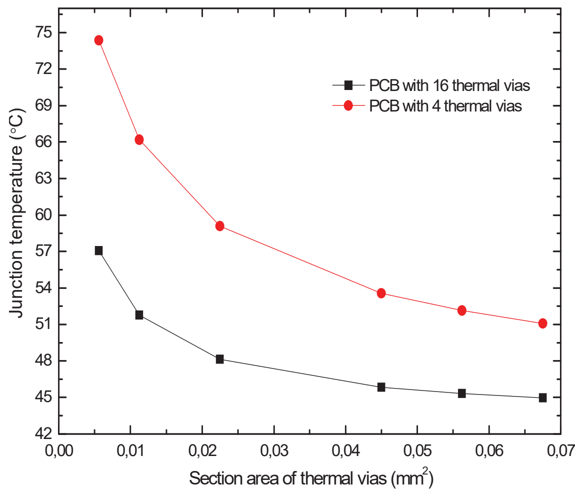


Fig. 14 Junction temperature ($T_J$) depends with the section area of thermal vias - for PCBs with 4 and 16 thermal vias

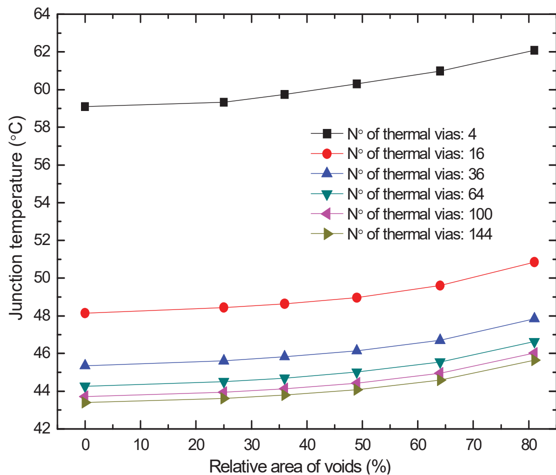


Fig. 15 Junction temperature ($T_J$) depending with relative area of voids in solder interface, considering cases with different thermal vias in the exposed pad area

## IV. Conclusion

This article presents an experimental method to estimate the junction temperature of exposed pad packages (i.e. QFN), provides a maximum of flexibility for thermal characterization of semiconductor packages.

The implemented solution is composed by a *Thermal Test Chip* (TTC-1002) into a QFN cavity that, is able to measure temperature in real-time and directly on the die and controlling the device power. Describe the method and technique that the designer should use to achieve optimum thermal performance, and demonstrate the effect of system-level constraints on the thermal performance of the design. The solution is experimentally validated (according to the JEDEC Standards) through a numeric analysis tool provided by the Mechanical APDL (Ansys Parametric Design Language) under same conditions. Nowadays, thermal management is an important issue in reliability of electronics systems. Since the amount of heat dissipation needed for a design depends on the IC dissipated power, the ambient temperature, airflow, the PCB designs and material properties, etc. With so much parameters, thermal simulations could be a difficult task for engineers and PCB designers to assess thermal efficiency without an experimental analysis.

## Acknowledgment

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