

A Comparative Analysis of Multicarrier SPWM Strategies for Five-Level Flying Capacitor Inverter

Bachir Belmadani, Rachid Taleb, Zinelaabidine Boudjema, Adil Yahdou

Abstract—Carrier-based methods have been used widely for switching of multilevel inverters due to their simplicity, flexibility and reduced computational requirements compared to space vector modulation (SVM). This paper focuses on Multicarrier Sinusoidal Pulse Width Modulation (MCSPWM) strategy for the three phase Five-Level Flying Capacitor Inverter (5LFCI). The inverter is simulated for Induction Motor (IM) load and Total Harmonic Distortion (THD) for output waveforms is observed for different controlling schemes.

Keywords—Flying capacitor inverter, multicarrier sinusoidal pulse width modulation, space vector modulation, total harmonic distortion, induction motor.

I. INTRODUCTION

INVERTERS are widely used in modern power grids; a great focus is therefore made in different research fields in order to develop their performance. Three-level inverters are now conventional apparatus but other topologies have been attempted this last decade for different kinds of applications. Among them, Neutral Point Clamped (NPC) inverters, flying capacitor inverters also called imbricated cells, and series connected cells inverters called cascaded H-bridge inverters [1]-[3].

The cascaded multilevel inverters have more advantages than other topologies, because it does not require any balancing capacitors and diodes. Cascaded inverters need separate DC sources for each H-Bridge, so there is no voltage balancing problem, but isolated DC sources are not readily available, this is the main drawback of this topology. In this paper Flying Capacitor Inverter is controlled with the Level Shifted scheme of Sinusoidal PWM, i.e., Phase Disposition (PD), Phase Opposition Displacement (POD) and Alternative Phase Opposition Displacement (APOD). The inverter is simulated for Induction Motor (IM) and THD for output waveforms is observed for different controlling schemes. The THD for the output waveforms is observed and the technique with least THD is selected for further simulations.

II. FLYING CAPACITOR STRUCTURE

The capacitor clamped inverter alternatively known as flying capacitor was proposed by Meynard and Foch in 1992 [4]. The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes,

the inverter uses capacitors in their place. The flying capacitor involves series connection of capacitor clamped switching cells. This topology has a ladder structure of DC side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. Fig. 1 shows the Five-Level Flying Capacitor Inverter (5LFCI).

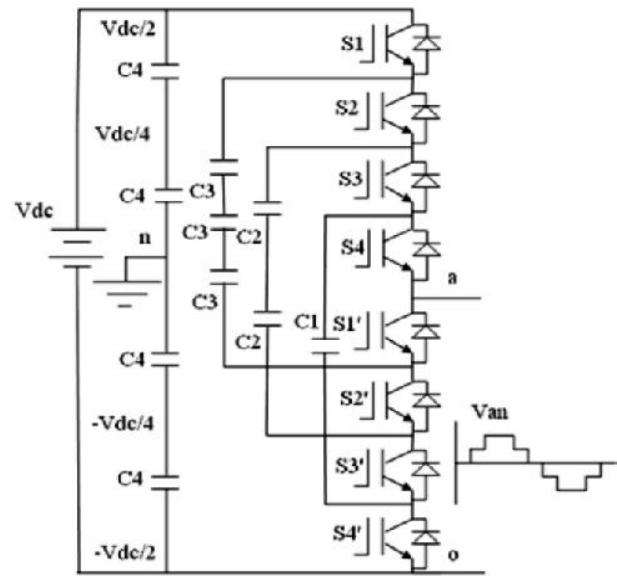


Fig. 1 Five-Level Flying Capacitor Inverter (5LFCI)

A. Operation of Flying Capacitor

In the operation of Flying Capacitor Multilevel Inverter (FCMLI), each phase node (a, b, or c) can be connected to any node in the capacitor bank (V_1, V_2, V_3). Connection of the a-phase to positive node V_3 occurs when S_1 and S_2 are turned on and to the neutral point voltage when S_2 and S_1' are turned on. The negative node V_1 is connected when S_1' and S_2' are turned on. The clamped capacitor C_1 is charged when S_1 and S_1' are turned on and is discharged when S_2 and S_2' are turned on. The charge of the capacitor can be balanced by proper selection of the zero states. In comparison to the three-level diode-clamped inverter, an extra switching state is possible. In particular, there are two transistor states, which make up the level V_3 . Considering the direction of the a-phase flying capacitor current I_a for the redundant states, a decision can be made to charge or discharge the capacitor and therefore, the capacitor voltage can be regulated to its desired value by switching within the phase. As with the three-level flying capacitor inverter, the highest and lowest switching states do not change

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the charge of the capacitors. The two intermediate voltage levels contain enough redundant states so that both capacitors can be regulated to their ideal voltages.

Similar to the diode clamped inverter, the capacitor clamping requires a large number of bulk capacitors to clamp the voltage. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, an N level converter will require a total of $(N-1)(N-2)/2$ clamping capacitors per phase in addition to the $(N-1)$ main dc bus capacitors.

Unlike the diode clamped inverter, the flying capacitor inverter does not require all of the switches that are on (conducting) in a consecutive series. Moreover, the flying capacitor inverter has phase redundancies, whereas the diode clamped inverter has only line-line redundancies [5]-[7]. These redundancies allow a choice of charging/discharging specific capacitors and can be incorporated in the control system for balancing the voltages across the various levels.

The voltage synthesis in a five level capacitor clamped converter has more flexibility than a diode clamped converter. Using Fig. 1 as the example, the voltage of the five level phase leg "a" output with respect to the neutral point n (i.e. V_{an}), can be synthesized by the following switch combinations:

1. Voltage level $V_{an} = V_{dc}/2$, turn on all upper switches S_1 and S_4 .
2. Voltage level $V_{an} = V_{dc}/4$, there are three combinations:
 - a. Turn on switches S_1, S_2, S_3 and S'_1 ($V_{an} = V_{dc}/2$).
 - b. Turn on switches S_2, S_3, S_4 and S'_4 ($V_{an} = 3V_{dc}/4$).
 - c. Turn on switches S_1, S_3, S_4 and S'_3 ($V_{an} = V_{dc}/2$).
3. Voltage level $V_{an} = 0$, turn on all upper switches S_3, S_4 and lower switches S'_1, S'_2 .

4. Voltage level $V_{an} = -4V_{dc}/4$, turn on all upper switches S_1 and lower switches S'_1, S'_2 and S'_3 .
5. Voltage level $V_{an} = -V_{dc}/2$, turn on all upper switches S'_1, S'_2, S'_3 and S'_4 .

B. Features of Flying Capacitor

The major problem in this inverter is the requirement of a large number of storage capacitors. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, an N level converter will require a total of $(N-1)(N-2)/2$ auxiliary capacitors per phase leg in addition to $(N-1)$ main dc bus capacitors. With the assumption that all capacitors have the same voltage rating, an N level diode clamp inverter only requires $(N-1)$ capacitors.

In order to balance the capacitor charge and discharge, one may employ two or more switch combinations for middle voltage levels (i.e., $3V_{dc}/4, V_{dc}/2$, and $V_{dc}/4$) in one or several fundamental cycles. Thus, by proper selection of switch combinations, the flying capacitor multilevel converter may be used in real power conversions. However, when it involves real power conversions, the selection of a switch combination becomes very complicated, and the switching frequency needs to be higher than the fundamental frequency. In summary, advantages and disadvantages of a flying capacitor multilevel voltage source converter are as follows.

III. MULTICARRIER SINUSOIDAL PWM TECHNIQUES

Multicarrier PWM techniques entail the natural sampling of a single modulation or reference waveform with carrier signals, typically triangular waveforms [8]-[10]. They can be categorized as follows:

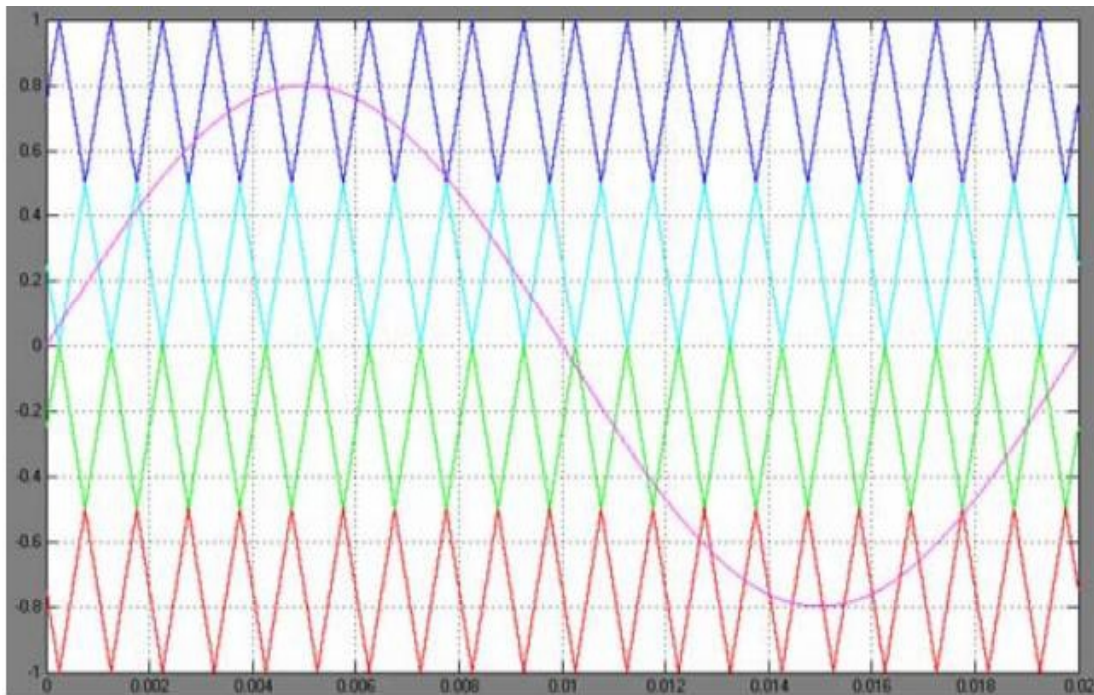


Fig. 2 APOD carriers' waveform for 5LFCI

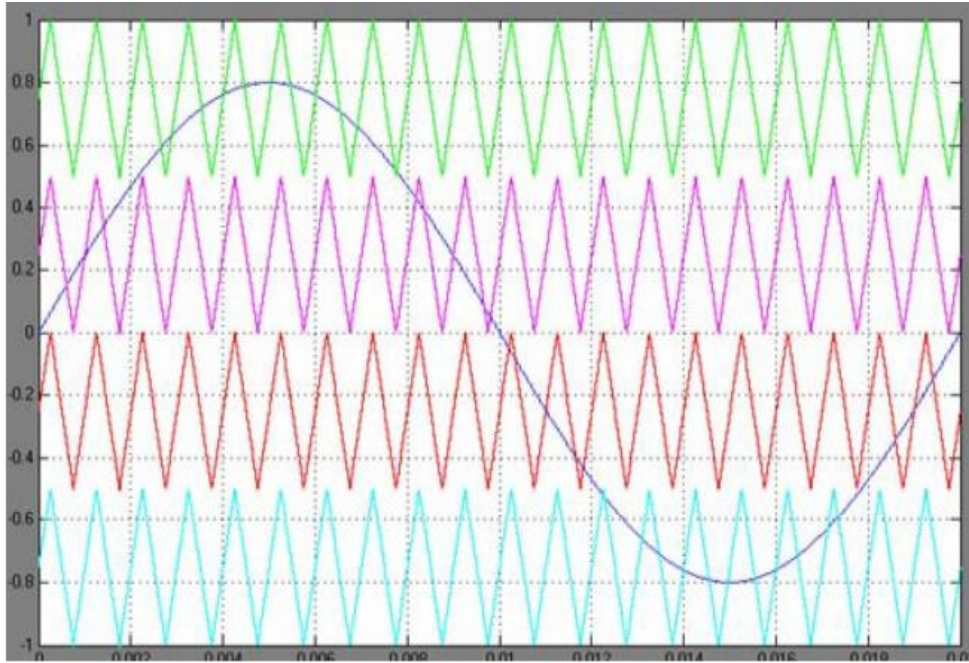


Fig. 3 PD carriers' waveform for 5LFCI

A. Alternative Phase Opposition Disposition (APOD)

This technique requires each of the $(N-1)$ carrier waveforms, for an N level phase waveform, to be phase displaced from another by 180 degree alternatively as shown in Fig. 2.

B. Phase Disposition (PD)

This technique is similar to APOD, except the carriers are in phase as shown in Fig. 3.

C. Phase Opposition Dispositions (POD)

The carrier waveforms are all in phase above and below the zero reference value, however there is a 180 degree phase shift between those above and below zero, Fig. 4.

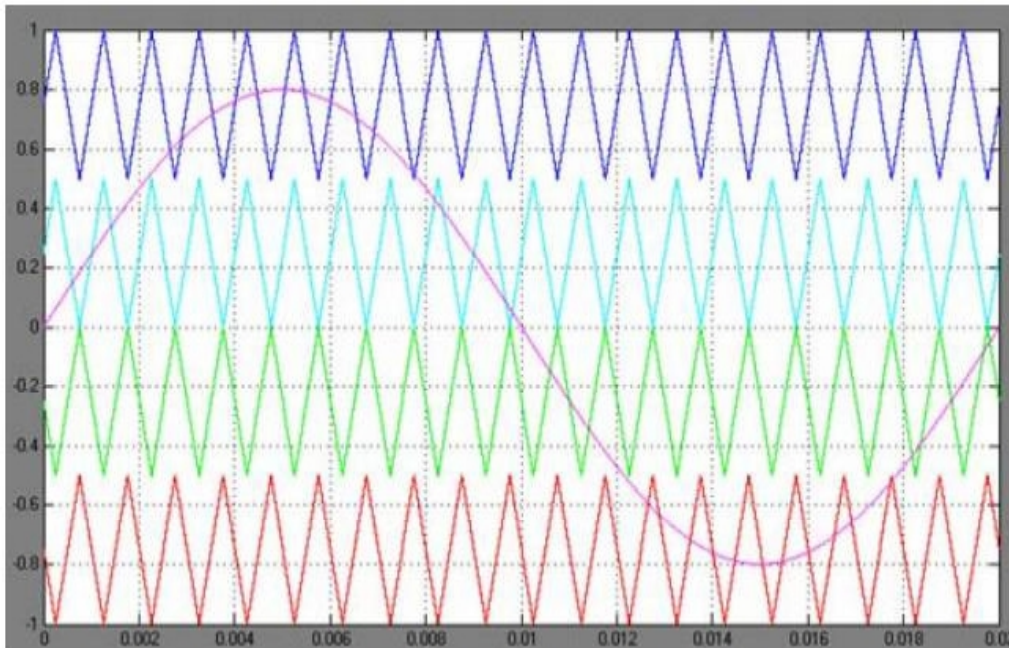


Fig. 4 POD carriers' waveform for 5LFCI

IV. SIMULATION RESULTS

The three phase Five-Level Flying Capacitor Inverter (5LFCI) is modeled in MATLAB-Simulink environment. Simulations are performed for different values of modulation index m (0.8, 0.9, 1) and the corresponding %THD are measured using the FFT block and their values are shown in Table I. Figs. 5 to 10 show the simulated output voltage of 5LFCI fed IM (1.5kW) and their harmonic spectrum and torque characteristics of IM with above strategies but for only one sample value of $m = 0.9$. Table II shows the oscillation band of electromagnetic torque (ΔT_e) of chosen 5LFCI.

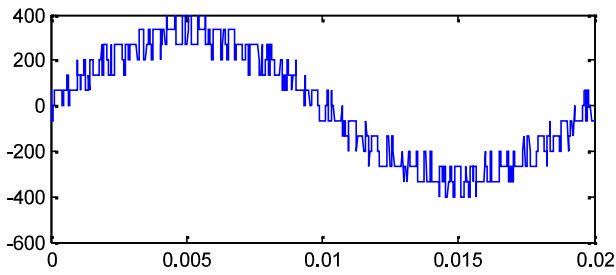


Fig. 5 Output voltage waveform (V) and its FFT for the APOD method

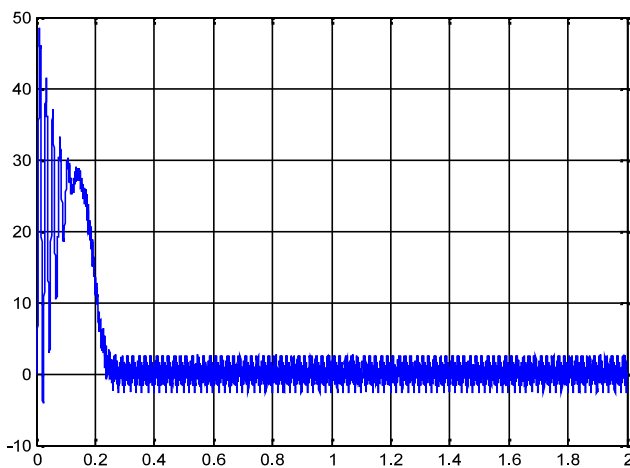


Fig. 6 Electromagnetic torque (Nm) of IM for the APOD method

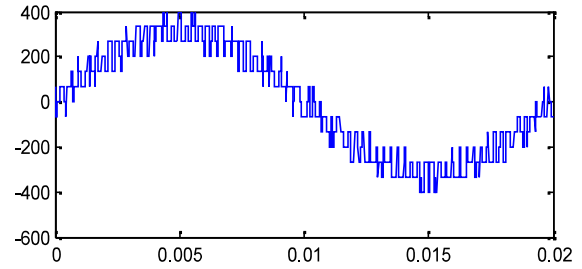


Fig. 7 Output voltage waveform (V) and its FFT for the PD method

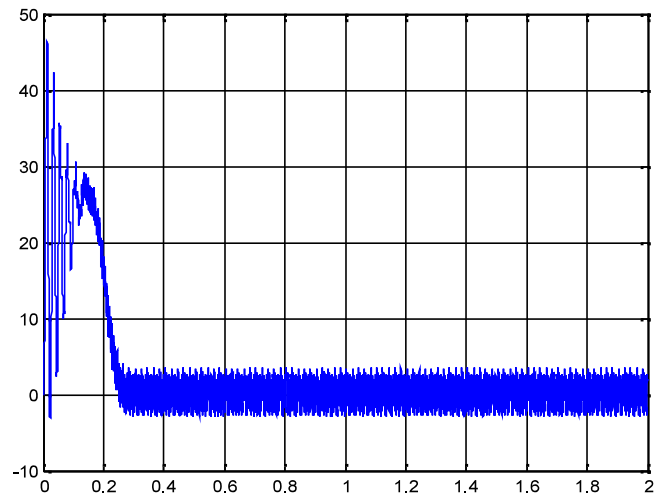


Fig. 8 Electromagnetic torque (Nm) of IM for the PD method

TABLE I
 %THD FOR DIFFERENT MODULATION INDICES

m	APOD	PD	POD
0.8	17.19	20.27	14.82
0.9	13.56	16.03	9.19
1	10.31	13.22	6.76

TABLE II
 ΔT_e (V) FOR DIFFERENT MODULATION INDICES

m	APOD	PD	POD
0.8	7.88	8.71	6.97
0.9	5.57	6.55	4.26
1	3.21	4.11	2.38

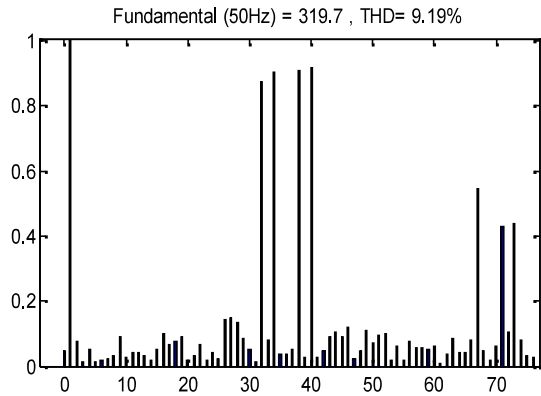
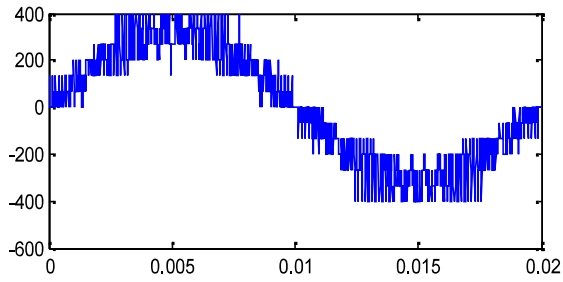


Fig. 9 Output voltage waveform (V) and its FFT for the POD method

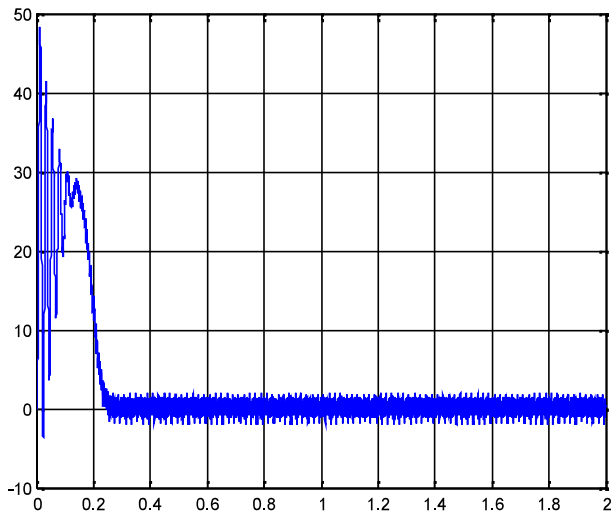


Fig. 10 Electromagnetic torque (Nm) of IM for the POD method

V. CONCLUSION

In this work the simulation results of three phase Five-Level Flying Capacitor Inverter (5LFCI) fed Induction Motor (IM) load with various modulating strategies are obtained through MATLAB-Simulink. The output quantities like phase voltage, THD spectrum for phase voltage, and torque characteristics of IM are obtained. It is observed that the PODPWM method presents better performances than the other methods (PDPWM & APODPWM).

REFERENCES

- [1] J. Rodriguez, S. Bernet, P. K. Steimer, I. E. Lizama, *A Survey on Neutral-Point-Clamped Inverters*, IEEE Transactions on Industrial Electronics, vol. 57, no. 7, pp. 2219-2230, July 2010.
- [2] J. Huang, K. A. Corzine, *Extended operation of flying capacitor multilevel inverters*, IEEE Transactions on Power Electronics, vol. 21, no. 1, pp. 140-147, January 2006.
- [3] E. Babaei, *A cascade Multilevel Converter Topology with Reduced Number of Switches*, IEEE Transactions on Power Electronics, vol. 23, no. 6, pp. 2657-2664, November 2008.
- [4] T.A. Meynard, H. Foch, *Multi-level conversion: high voltage choppers and voltage-source inverters*, 23rd Annual IEEE Power Electronics Specialists Conference (PESC'92), vol. 1, pp. 397-403, Toledo, 29 June-3 July 1992.
- [5] A.K. Sadigh, M. Abarzadeh, K.A. Corzine, V. Dargahi, *A New Breed of Optimized Symmetrical and Asymmetrical Cascaded Multilevel Power Converters*, vol. 3, no. 4, pp. 1160-1170, July 2015.
- [6] J. Rodriguez, J.S. Lai, F.Z. Peng, *Multilevel inverters: a survey of topologies, control and applications*, IEEE Transaction on Power Electronics, vol. 49, no. 3, pp. 724-738, August 2002.
- [7] L.M. Tolbert, F.Z. Peng, T.G. Habetler, *Multilevel converters for large electric drives*, IEEE Transactions on Industry Applications, vol. 35, no. 1, pp. 36-44, January-February 1999.
- [8] P. Omer, J. Kumar, B.S. Surjan, *Comparison of multicarrier PWM techniques for cascaded H-bridge inverter*, IEEE Students' Conference on Electrical, Electronics and Computer Science (SCEECS'14), pp. 1- 6, Bhopal, 1-2 March 2014.
- [9] E.T. Renani, M.F.M. Elias, N.A. Rahim, *Performance evaluation of multicarrier PWM methods for cascaded H-bridge multilevel inverter*, 3rd IET International Conference on Clean Energy and Technology (CEAT'14), pp. 1-5, Kuching, 24-26 November 2014.
- [10] A. Kumar, P. Bansal, *A novel symmetrical multilevel inverter topology with reduced switching devices using different PWM techniques*, International Conference on Electrical, Electronics, Signals, Communication and Optimization (EESCO'15), pp. 1-6, Visakhapatnam, 24-25 January 2015.