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Hybrid Pulse Width Modulation Techniques for the Reduction of Switching Losses and Voltage Harmonics in Cascaded Multilevel Inverters

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Abstract**—**These days, the industrial trend is moving away from heavy and bulky passive components to power converter systems that use more and more semiconductor elements. Also, it is difficult to connect the traditional converters to the high and medium voltage. For these reasons, a new family of multilevel inverters has appeared as a solution for working with higher voltage levels. Different modulation topologies like Sinusoidal Pulse Width Modulation (SPWM), Selective Harmonic Elimination Pulse Width Modulation (SHE-PWM) are available for multilevel inverters. In this work, different hybrid modulation techniques which are combination of fundamental frequency modulation and multilevel sinusoidal-modulation are compared. The main characteristic of these modulations are reduction of switching losses with good harmonic performance and balanced power loss dissipation among the device. The proposed hybrid modulation schemes are developed and simulated in Matlab/Simulink for cascaded H-bridge inverter. The results validate the applicability of the proposed schemes for cascaded multilevel inverter.

Keywords**—**Hybrid PWM techniques, Cascaded Multilevel Inverters, Switching loss minimization.

I. Introduction

MULTILEVEL inverters offer a number of advantages compared to the conventional two-level inverters. The stepped approximation of the sinusoidal waveform using higher levels reduces the harmonic distortion of the output waveform, and the stresses across the semiconductor devices. It also allows higher voltage/current and power ratings. The multilevel voltage source inverter is recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output [1]. The reduced switching frequency of each individual switch of the converter reduces the switching losses and improves the efficiency of the converter [1].The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages. As the number of levels reach infinity, the output THD approaches zero [2].

The Diode-clamped multilevel inverters, Flying-capacitor multilevel inverters, Cascaded-inverters with separate DC sources are the mostly used types of multilevel inverters. Among these topologies, diode clamped inverter is difficult to be expanded to multilevel because of the natural problem of DC link voltage unbalancing. Moreover, Flying-capacitor inverter is also difficult to be realized because each capacitor must be charged with different voltages as the voltage level increases. Where as in cascaded multilevel inverter, the problem of DC link voltage unbalancing doesn't occur, thus easily expanded to multilevel. This inverter can avoid extra clamping diodes or voltage balancing capacitors [4], [5]. Due to these advantages cascaded multilevel inverter has been widely applied to such applications as HVDC, SVC, stabilizer and high power motor drives [3].

A single-phase two-cell series configuration of cascaded inverter is shown in Fig. 1.

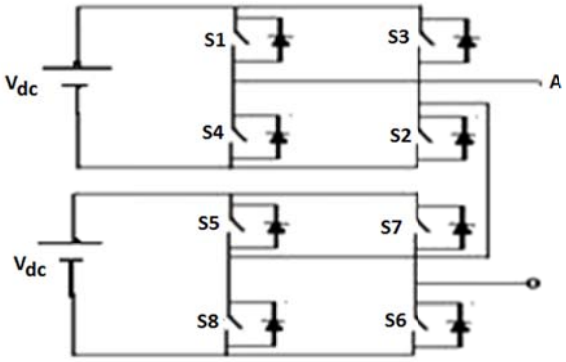

Fig. 1 Single-phase structure of a cascaded inverter

Each separate DC source is associated with a single-phase full-bridge inverter. The ac terminal voltages of different level voltages are connected in series. By different combinations of the four switches (S1-S4), each full bridge inverter can generate three voltage outputs, $-V_{dc,}$ $+V_{dc,}$ and zero. The ac output of each of the full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. Note that the number of output phase voltage levels is defined in different way from those of two previous inverters. In this topology, the number of output phase voltage levels (m) is defined by

$$m=2S+1 \quad (1)$$

where S is the number of DC sources. Table I shows the switch combination of the voltage levels and their corresponding switch states.

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TABLE I
VOLTAGE LEVELS AND SWITCHING STATES OF A TWO-CELL CASCADED INVERTER

Output V_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$V_5= 2V_{dc}$	1	1	0	0	1	1	0	0
$V_4= V_{dc}$	1	1	0	0	1	0	1	0
$V_3= 0$	0	0	0	0	0	0	0	0
$V_2= -V_{dc}$	0	0	1	1	0	1	0	1
$V_1= -2V_{dc}$	0	0	1	1	0	0	1	1

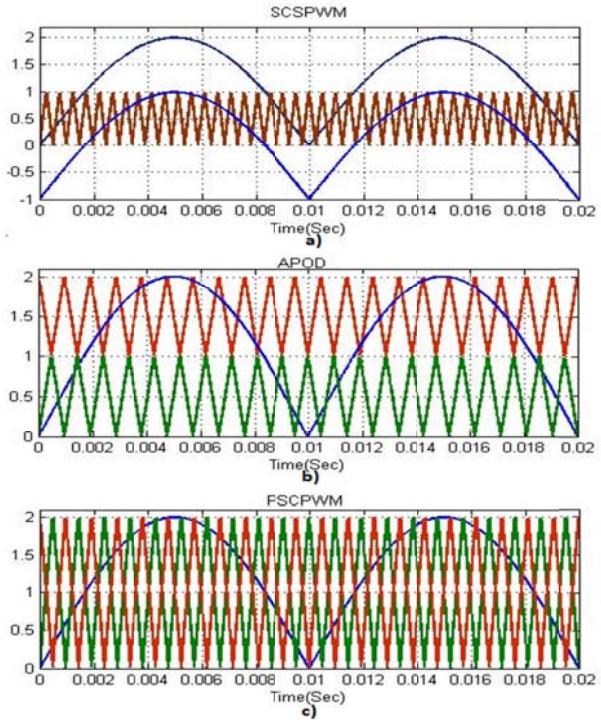

Fig. 2 Sinusoidal reference and carriers of MSPWM operation

In this paper, hybrid-modulation technique for cascaded multilevel inverter is proposed in order to reduce the switching losses with good harmonic performance, balanced power loss dissipation among the devices within a cell. Hybrid-modulation strategies are compared with three different sequential switching strategies for cascaded multilevel inverter by using MATLAB/Simulink software.

II. MULTILEVEL SINUSOIDAL PWM (MSPWM) STRATEGIES

The well-known modulation schemes for multilevel inverters are the Selective Harmonic Elimination Pulse Width Modulation (SHE-PWM) and Sinusoidal Pulse Width Modulation (SPWM). Recently, hybrid modulation technique has been developed. Selective harmonic elimination scheme requires offline calculations, making dynamic operation and closed-loop implementation not straight forward. SHE becomes unfeasible with the increase of number of levels [6]. Moreover, sinusoidal pulse width modulation methods are based on multi-carrier arrangements as alternative phase opposition disposition (APOD) PWM, phase-shifted carrier (PSC) PWM, single-carrier sinusoidal (SCS) PWM. It is the most efficient method of controlling the output voltage by incorporating the pulse width modulation control within the inverters [7]-[9]. It offers good harmonic performance. Whereas, the switching loss reduction of multilevel sinusoidal modulation schemes with low computational overhead is possible with hybrid-modulation technique.

Single-carrier sinusoidal PWM (SCS-PWM) technique is a result of two sinusoidal reference signals with a frequency of f_0 and amplitude of A_m and one carrier signal. The carrier signal is a train of triangular waveforms with a frequency of f_c and amplitude of A_c. The arrangement of carrier and two reference signals is as shown in Fig. 2 (a). Alternative phase opposition disposition (APOD) technique requires (m-1)/2 carrier signals for an m-level inverter and are to be phase disposed from each other by 180 degree alternatively as shown in Fig. 2 (b). Phase-shifted carrier pulse width modulation (PSC-PWM) is a good solution for single-phase cascaded inverters compared to alternative phase opposition disposition. The carrier waves are phase shifted by $2\pi/(N-1)$. The arrangement of reference wave and carrier wave of PSC-PWM is shown in Fig. 2 (c).

The modulation index is defined as

$$m_i = A_m/M * A_c \quad (2)$$

where M is the number of converter cells, A_c is the amplitude of carrier wave. The definition of the modulation frequency ratio m_f for converter is given as

$$m_f = \frac{f_c}{f_0} \quad (3)$$

where m_f is frequency modulation, f_c and f_0 are the frequencies of carrier and reference waves.

III. HYBRID MODULATION TECHNIQUES FOR CASCADED MULTILEVEL INVERTERS

Hybrid modulation is the combination of fundamental frequency modulation (FPWM) and MSPWM for each inverter cell operation so that the output inherits the features of switching loss reduction from FPWM and good harmonic performance from MSPWM. In this modulation technique, the four switches of each inverter cell are operated at two different frequencies; two being commutated at FPWM, while the other two switches are modulated at MSPWM, therefore the resultant switching patterns are the same as those obtained with MSPWM. A sequential switching scheme is embedded with this hybrid modulation in order to overcome unequal switching losses and therefore differential heating among the power devices. A simple base PWM circulation scheme is also introduced here to get resultant hybrid PWM circulation makes balanced power dissipation among the power modules. It consists of modulation base generator, base PWM circulation module, and hybrid modulation controller (HMC) to generate new modulation pulses.

In this modulation strategy, three base modulation pulses are needed for each cell operation in a CMLI. A sequential switching pulse (A) is a square wave signal with 50% duty ratio and half the fundamental frequency. This signal makes

every power switch operating at MSPWM and FPWM sequentially to equalize the power losses among the devices. FPWM (B) is a square wave signal synchronized with the modulation waveform; B=1 during the positive half cycle of the modulation signal, and B=0 during negative half cycle. A sequential switching pulse (SSP) and FPWM pulses are same for all inverter cells. MSPWMs (C or D) for each cell, differs depends upon the type of carrier and modulation signals used. The proposed sequential hybrid modulation block diagram representation is as shown in Fig. 3 (a).

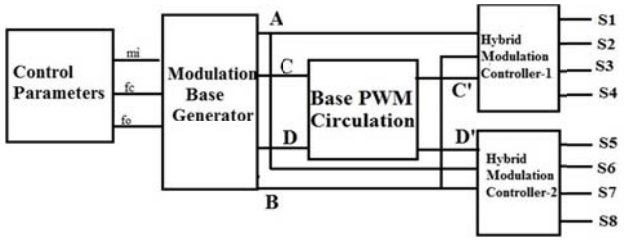

Fig. 3 (a) Proposed sequential hybrid modulation

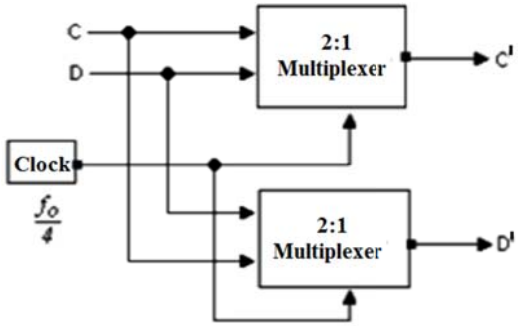

Fig. 3 (b) Base PWM circulation for five-level

For long operating-time expectancy, it is important to share the power loss among every module, and furthermore, to every power device in the cell. This is one of the key issues the modulation should cover. A simple base PWM circulation scheme is introduced here to get resultant hybrid PWM circulation among the power modules. The scheme of five-level base PWM circulation is shown in Fig. 3 (b). It consists of two 2:1 multiplexer, and selects one among the two PWMs based on the select clock signal. The clock frequency is $f_0/4$, makes the time base for PWM circulation from one module to another. After two fundamental frequency periods, the order is changed so that the first module HPWM becomes the second module; the second becomes the third and so on while the last module HPWM shifts to the first.

Hybrid Modulation Controller (HMC) combines SSP, and MSPWM, that produces SSHM pulses. It is designed by using a simple combinational logic and the functions for a five-level HPWM are expressed as

$$S_1 = ABC^I + \bar{A}B;$$
$$S_2 = A\bar{B}C^I + \bar{A}\bar{B};$$
$$S_3 = \bar{A}\bar{B}C^I + A\bar{B};$$
$$S_4 = \bar{A}BC^I + AB;$$
$$S_5 = ABD^I + \bar{A}B;$$
$$S_6 = A\bar{B}D^I + \bar{A}\bar{B};$$
$$S_7 = \bar{A}\bar{B}D^I + A\bar{B};$$
$$S_8 = \bar{A}BD^I + AB \quad (4)$$

where A is a SSP, B is a FPWM, C' is a MSPWM for cell-I and D' is MSPWM for cell-II. If SSP A=1, then S1, S2, S1' and S2' are operated with MSPWM, while S3, S4, S3' and S4' are operated at FPWM. If SSP A=0, then S1, S2, S1' and S2' are operated at FPWM, while S3, S4, S3' and S4' are operated with MSPWM. Since A is a sequential signal, the average frequency amongst the four switches is equalized. Voltage stress and current stress of power switches in each cell is inherently equalized with this modulation. After every two fundamental periods, the HPWM pattern is changed so that the first module (S1, S2, S3 and S4) becomes the second module (S1', S2', S3' and S4'), and the second shifts to the first. As a result, all inverter cells operate in a balanced condition with the same power handling capability and switching losses. It is found that the proposed modulations offer lower THD compared to the conventional one, thus the superiority. Hybrid pulse width modulation technique, in which one duty cycle includes a combination of four pulses, among them two are constant pulses and remaining two are the pulses of C' and D'. In order to avoid losses, one of the two switches to be turned on with constant pulse.

A. Hybrid Alternative Phase Opposition Disposition (HAPOD) Technique

In the HAPOD modulation strategy, three base modulation pulses are needed for each cell operation in CMLI. A sequential switching pulse (A) is a square wave signal with 50% duty ratio and half the fundamental frequency. This signal makes every power switch operating at MSPWM, and FPWM sequentially to equalize the power losses among the power modules. FPWM (B) is a square wave signal synchronized with the modulation waveform; B=1 during the positive half cycle of the modulation signal, and B=0 during the negative half cycle. APOD modulation pulse for cell-I (C) is obtained from the comparison between unipolar modulation waveform and carrier, while APOD modulation pulse for cell-II (D) is obtained from the comparison between modulation waveform and carrier with DC bias of $-V_c+2A_c$ as shown in Fig. 4:

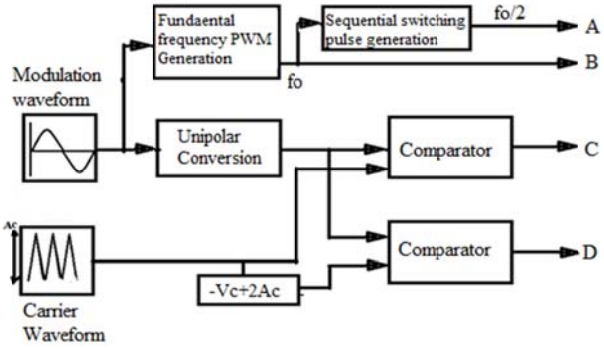

Fig. 4 Hybrid alternative phase opposition disposition (HAPOD)

B. Hybrid Single-Carrier Sinusoidal PWM (HSC-PWM) Technique

The HSC-PWM technique is described in Fig. 5. In this modulation strategy also the generation of A and B pulses are same as the HAPOD. SCS-PWM modulation pulse (C) for cell-I of CMLI is obtained from the comparison between unipolar modulation waveform and carrier waveform, while SCS-PWM pulse (D) for cell-II of CMLI is generated from the comparison between the modulation signals with bias of $-A_c$ and single carrier as shown in Fig. 5.

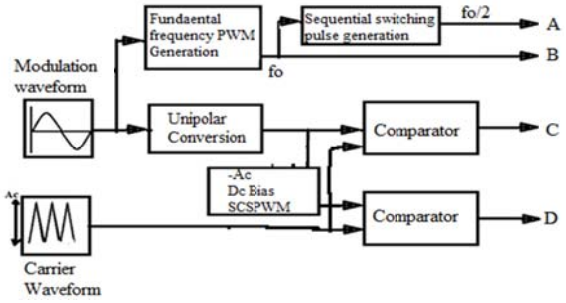

Fig. 5 Hybrid single-carrier sinusoidal PWM (HSC-PWM) technique

C. Hybrid Phase- Shifted Carrier PWM (HPSC) Technique

The block diagram of Hybrid Phase- Shifted Carrier PWM technique (HPSC) technique is shown in Fig. 6. In this modulation strategy also the generation of A and B pulses are same as the HAPOD. The PSC pulses (C and D) are based on the comparison of modulation waveform with the corresponding PSC waveform for every cell in a CMLI as shown in Fig. 6.

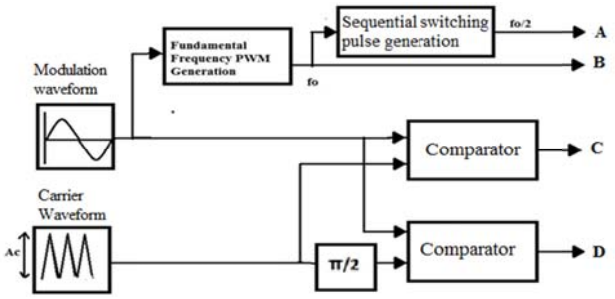

Fig. 6 Hybrid Phase-shifted carrier PWM technique (HPSC)

IV. Simulation Results

The proposed hybrid modulation techniques are developed and simulated using MATLAB/SIMULINK software for a five level CMLI with the dc-bus voltage of 50V.The frequency of modulated wave and carrier wave are 50 and 1500 Hz, respectively. First, the five-level CMLI is simulated with multi sinusoidal PWM strategies viz. SCS, APOD and PSC. Fig. 7 shows the five-level output voltage waveform and harmonic distortion using SCS PWM techniques with a modulation index of 0.7. The THD of the output voltage waveform is observes as 52.81%. Fig. 8 depicts the five-level output voltage waveform and harmonic distortion using APOD PWM techniques with a modulation index of 0.7. The THD of the output voltage waveform is observes as 22.05%. The output voltage waveform and harmonic distortion using PSC PWM techniques for the same modulation index of 0.7 is shown in Fig. 9 and the THD is observes as 22.09%.

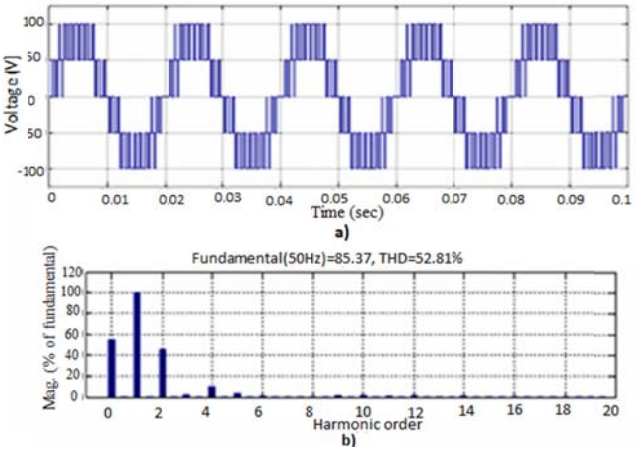

Fig. 7 (a) Output voltage waveform and (b) FFT analysis using SCS PWM

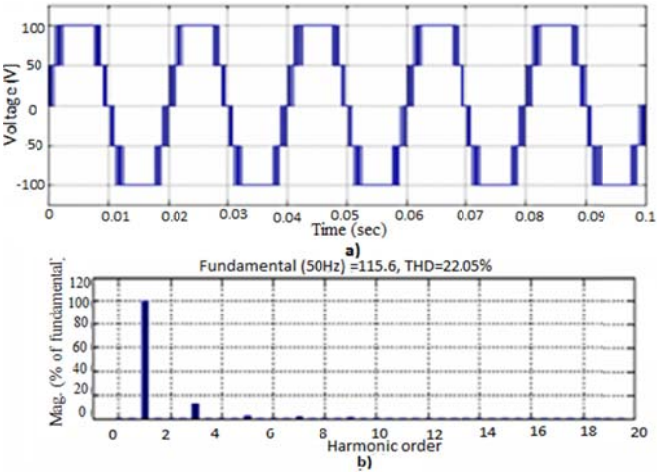

Fig. 8 (a) Output voltage waveform and (b) FFT analysis using APOD PWM

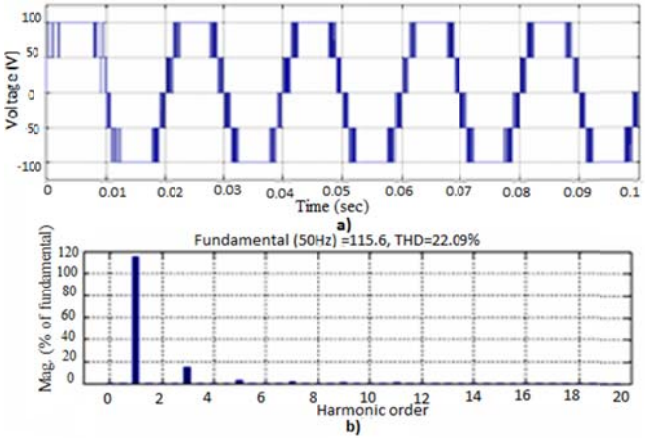

Fig. 9 (a) Output voltage waveform and (b) FFT analysis using PSC PWM

The proposed hybrid modulation techniques for five-level CMLI are simulated and output voltage and harmonic contents are compared with conventional multi-sinusoidal strategies. In the Hybrid modulation technique, it is observed that two switches of each inverter cell are operated at FPWM, while the other two switches are modulated at MSPWM. Therefore, the hybrid modulation techniques minimize the switching losses by considerable amount while achieving the same fundamental voltage output. Fig. 10 shows the five-level output voltage waveform and harmonic distortion using Hybrid SCS PWM techniques with a modulation index of 0.7. The THD of the output voltage waveform is observes as 39.46%. Fig. 11 depicts the five-level output voltage waveform and harmonic distortion using Hybrid APOD PWM techniques. The THD of the output voltage waveform is observes as 22.35%.The output voltage waveform and harmonic distortion using Hybrid PSC PWM techniques for the same modulation index of 0.7 is shown in Fig. 12. The THD of the output voltage waveform is observes as 21.50%.

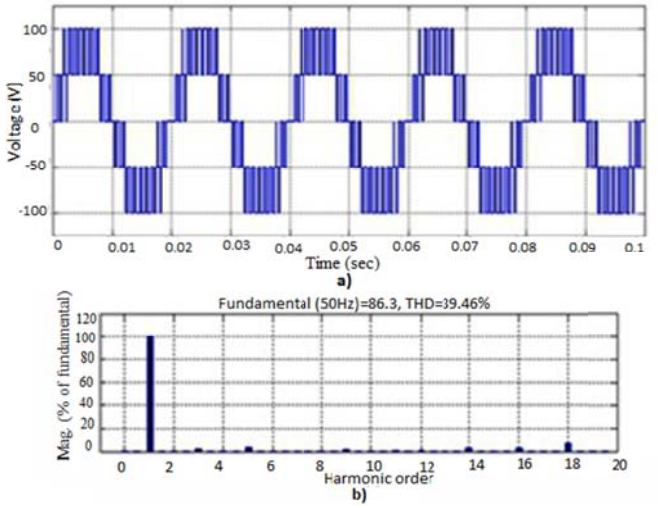

Fig. 10 (a) Output voltage waveform and (b) FFT analysis using HSC PWM

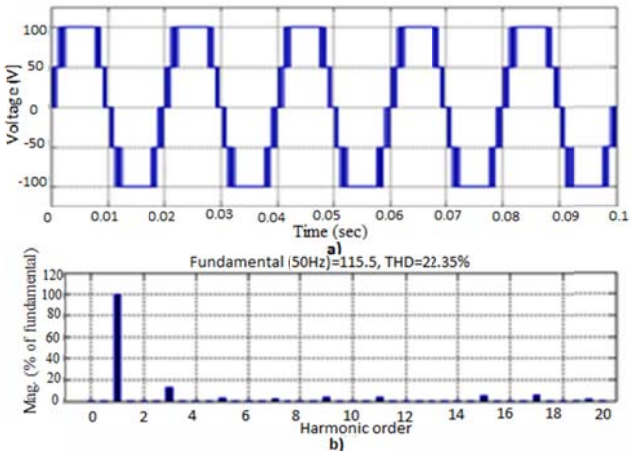

Fig. 11 (a) Output voltage waveform and (b) FFT analysis using HAPOD PWM

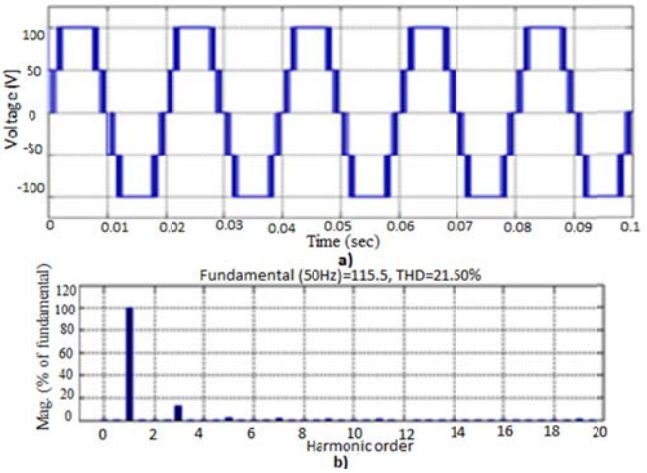

Fig. 12 (a) Output voltage waveform and (b) FFT analysis using HPSC PWM

From the results, it can be observed that the hybrid modulation techniques also reduce the harmonic content. The proposed hybrid modulation techniques are simulated with different values of modulation index. The THD with different hybrid modulation schemes at different modulation indices are described in Fig. 13. From the results, it can be observed that HPSC scheme produces less harmonic content than the other schemes at all the modulation indices.

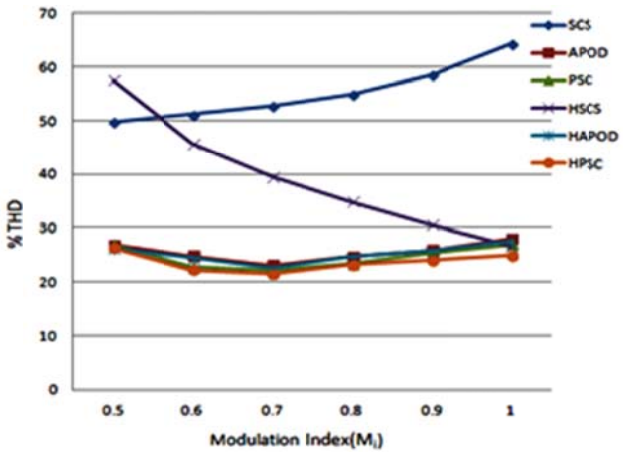

Fig. 13 Comparison of different PWM schemes

V. Conclusion

In this paper, an efficient sequential switching and PWM circulation techniques are embedded with the Hybrid modulations for balanced power dissipation among the power devices and for low switching losses. Three different hybrid modulation schemes viz. Hybrid Alternative Phase Opposition Disposition (HAPOD) scheme, Hybrid Single-Carrier Sinusoidal PWM (HSC-PWM) scheme and Hybrid Phase-Shifted Carrier PWM technique (HPSC) schemes for cascaded multilevel inverter are presented in this work. Comparison of the performance of these hybrid modulation techniques among them and also with conventional schemes is done by using MATLAB/SIMULINK software. It is noticed that, in this

proposed hybrid modulation techniques, 50% of the devices will operate only at fundamental frequency in every cycle and hence results in low switching losses. Compared to conventional MSPWM techniques, considerable switching loss reduction and voltage harmonic reduction are obtained in hybrid modulation schemes while achieving the same fundamental voltage tracking. Furthermore, it is found that phase-shifted carrier scheme generates the least harmonic distortion among these schemes.

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Dr. Reddy is a member of IEEE, ACM, the Institution of Engineers (India), Indian Society for Technical Education. He is a recipient of the Young Engineers Award in the year 2013 and Tata Rao Prize in 2012 from the Institution of Engineers (India).