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A Double PWM Source Inverter Technique with Reduced Leakage Current for Application on Standalone Systems

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***Abstract*—**The photovoltaic (PV) panel with no galvanic isolation system is well known technique in the world which is effective and delivers power with enhanced efficiency. The PV generation presented here is for stand-alone system installed in remote areas when as the resulting power gets connected to electronic load installation instead of being tied to the grid. Though very small, even then transformer-less topology is shown to be with leakage in pico-ampere range. By using PWM technique PWM, leakage current in different situations is shown. The results shown in this paper show how the pico-ampere current is reduced to femto-ampere through use of inductors and capacitors of suitable values of inductor and capacitors with the load.

***Keywords*—**Photovoltaic (PV) panel, Duty cycle, Pulse Duration Modulation (PDM), Leakage current.

I. Introduction

PHOTOVOLTAIC (PV) panels make up serious contenders to wind-energy for supplying to electric utilities through grid connectivity as renewable energy source-based distributed generating units. Even large companies, hotels, restaurants and residential developments are equipped with solar energy panels. PV panels are also used for small distributed power generation feeding the power supply blocks of installation in inaccessible locations. The use of power invertors or that of DC-DC converters is quiet common in such applications in between the PV panels and the appliances using solar energy ultimately. Increased power conversion efficiency alongside a good level of quality of the resulting AC output for grid connectivity is aim being explored in all such design pursuits. A transformer less inverter being light and less complex is a preferred choice these days when compared to its transformer based counter-parts as the later are bulky as well as hard to install in a system [1]. Rather than using transformer, transformer-less system shows better performance in the form of higher efficiency as well as less complex, lower cost and smaller volume compared to the transformer galvanic isolation feature of transformer-based [2]-[7]. The development of common-mode (CM) voltages in the case of transformer-less topologies is another concern that leads to large charge and discharge current flowing through the panel and inverter to the ground. This CM ground current causes an increase in the current harmonics, leading to higher losses, safety and EMI related concerns about human safety hazards [4]-[9]. Not only that, the CM current is the reason of distortion occurring in grid current [10]-[13]. It depends upon the topology of the proposed inverter [14] and the amplitude/voltage of fluctuated frequency content [15] when estimating total losses in the whole system. It flows through different places in a system such as the ground lines, the power lines, the output filter, and the parasitic capacitance itself [13]-[15]. To reduce the leakage current which is actually occurred the huge loses that can be done by modulation techniques especially in pulse width modulation (PWM) [6], [16]-[19]. Pulse Duration Modulation (PDM) has huge advantages in the case of getting actual signal through inverter. Uni-polar PWM is more preferable and the maximum current ripple is four times smaller than the bipolar PWM [19]. The use of embedded systems, microcontrollers, VLSI sensors and wireless communication technologies, have made it is possible to make small, cheap and efficient wireless sensor based stations either for collection of useful data reasons or monitoring purposes. Such hardware installations are deployed these days over long spans on highways or railway tracks often passing through inaccessible locations. Acquiring of solar energy for charging or of battery supplies relieve companies from extra personnel cost. This work is intended to look into elaborating the current leakage problem in inverters meant for deployment on of one such installation.

In this paper is shown how different wave shapes for various values of duty cycles have effect on the leakage current. This is shown with and without the use of inductors and capacitors with load, aimed at proposing a model that helps reduce the leakage current.

II. Some of the Important Key Parameters

Here are detailed some theoretical details and description of parameters being used in this work for obtaining results.

A. Duty Cycle (DC)

Duty cycle means the active movement of a machine or system over a period of single cycle. Hence, it's very easy to measure the ON/OFF time of the system. Moreover, below in Fig. 1 is shown a circuit 555-timer-based schematic for generating a digital output of variable duty cycle, DC.

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Different DC have different ratio of resistances where the capacitor is fixed. In below, has been shown the effect of duty cycle in a system.

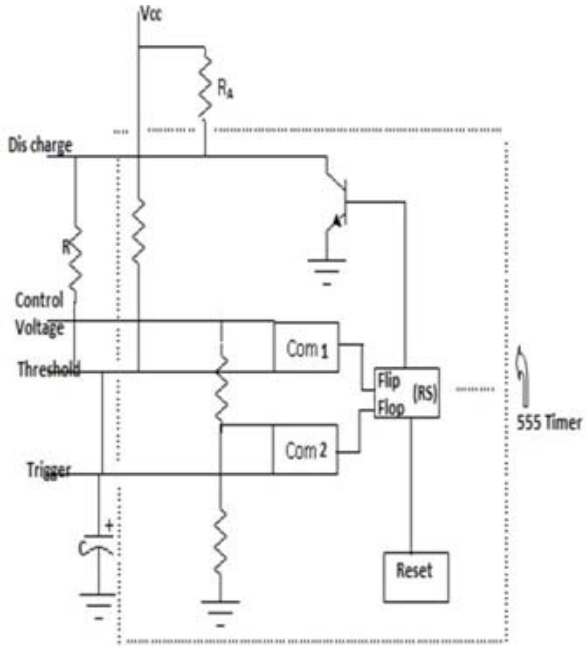

Fig. 1 555 timer for finding duty cycle

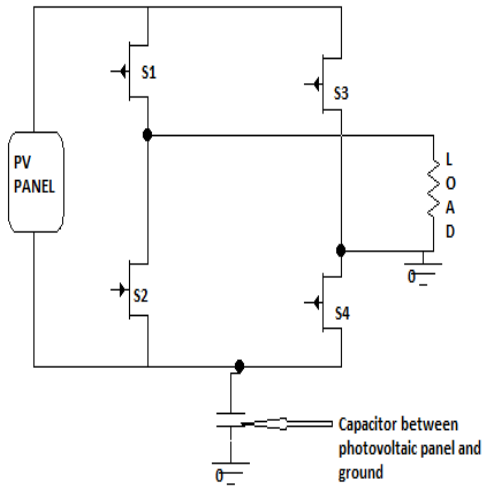

Fig. 2 Normal inverter with PV panel

$$(\frac{\text{ON TIME } (T_{ON})}{\text{ON TIME } (T_{ON})} + \text{OFF TIME } (T_{OFF} + 100\%)$$

TON = 0.69 (RA+R) C and TOFF =0.69 RC

T= TON + TOFF = 0.69 (RA+R) C + 0.69 RC = 0.69 (RA +2R) C
DC= TON/T = TON / (TON + TOFF)

20%duty cycle:
0.2=0.69(RA+R) C/0.69(RA+2R) C = (RA+R)/ (RA+2R)
RA=-0.75R

50% duty cycle:
0.5=0.69(RA+R) C/0.69(RA+2R) C = (RA+R)/ (RA+2R)
RA =0

60%duty cycle:
0.6=0.69(RA+R) C/0.69(RA+2R) C = (RA+R)/ (RA+2R)
RA=0.5R

75% duty cycle:
0.75=0.69(RA+R) C/0.69(RA+2R) C = (RA+R)/ (RA+2R)
RA=2R

B. Common-Mode Leakage Current (CMLC)

Common mode leakage current is a current which is flows between photovoltaic panel and ground. Hence, fully affect the main system which is reason to increase the system price and less power quality. It makes problem to operate the converter operating with low power efficiency. It can be said load current or residual current as well.

C. Pulse Width Modulation (PWM)

Pulse Width/duration Modulation is a modulation where we can set our pulse according to our need. Hence, we can turn on or off our switches. Uses of PWM are huge such as motors, lights, heaters and so on. It actually helps to change the whole system especially for inverter switching technique where it uses in different way for getting actual effect. Using unipolar PWM control commercially available and literature reported indicate inverters with 96-98% efficiency. A microcontroller is programmed for producing a PWM sequence in order to turn ON/OFF a net of MOSFETs and IGBTs either in Boost or Buck mode.

III. Circuit Diagrams with Wave Shapes

In Fig. 2 is shown a circuit diagram when the DC from a PV panel is converted into AC is associated with leakage current through what is called as parasitic capacitor. The same becomes the reason for the leakage current flowing from PV panel to ground. In this circuit diagram used four MOSFET switches. In positive half cycle S1 and S4 are working whereas S2 and S3 are working in negative half cycle. In contrast, using load in this circuit is used resistive load. Fig. 4 shows the pulses for switching the four switches. Here using pulses for 50% duty cycles where used 5V input supply.

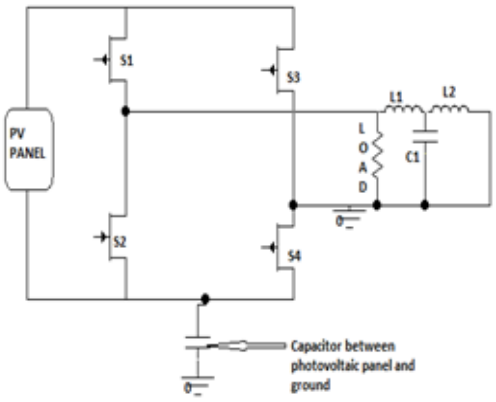

Fig. 3 Loaded inverter with inductor and capacitor

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As the using four switches are worked in alternative way, Hence S1 and S4 switches are in positive mode when S2 and S3 are in negative mode. In addition, Fig. 3 shows how an inverter with inductors and capacitor in parallel with the load is having effect on leakage current. The load current which is in the pico ampere ranges that shown in the same figure. Moreover, the switching currents and times are divided in to four sectors t1 to t4. Within that have two cycles are completed. The current of the switches are shown in both cases positive half cycle and negative half cycle. In both cases the getting current is in pico range.

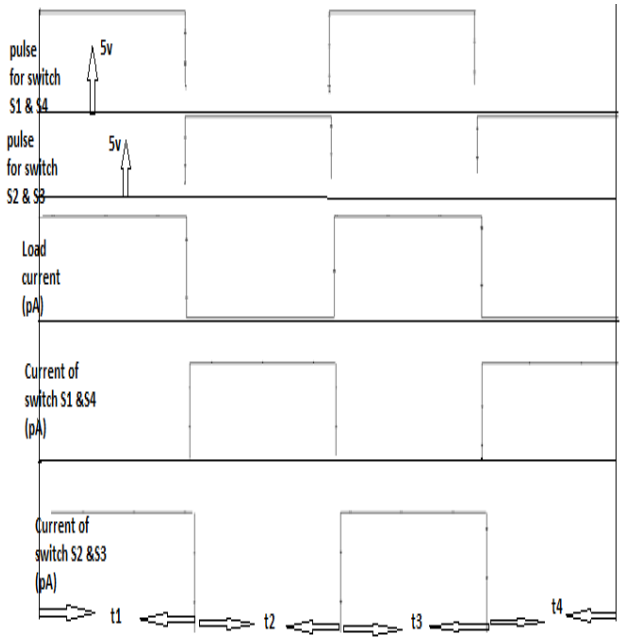

Fig. 4 Different wave shapes for 50% duty cycle

In Fig. 5 (a) is shown the leakage current for 50% duty cycle. However, when inductor and capacitor are used with load this current fluctuations are reduced in nano ampere range from pico range that has been shown in Fig. 5 (b).

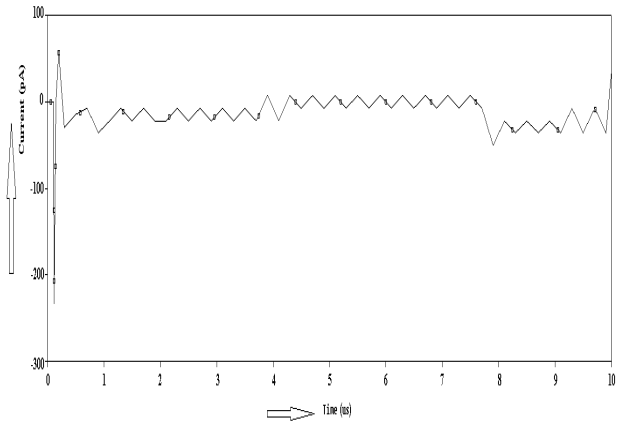

Fig. 5 (a) Leakage current for 50% duty cycle

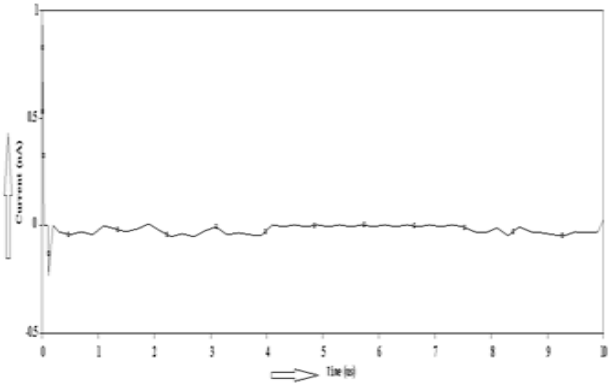

Fig. 5 (b) Leakage current for 50% duty cycle of inductor and capacitor added load

All values are dependent on the PWM. Hence are shown in Fig. 6 which is for 75% duty cycle and Fig. 8 where the duty cycles are 20% and 60%.

In Figs. 6 and 8 both cases, the using input value is 5V. Load current is shown as well as the current flow through the switches are shown in both positive and negative as well switches. To reduce the leakage current, used inductance and capacitance which is added with load. Hence the achieving leakage current is in nano range in Fig. 7 (b). In Fig. 9 (a) is shown the leakage current for 20% (S1 and S4) and 60% (S2 and S3) duty cycle whereas Fig. 9 (b) is shown the effect of adding inductance, capacitance in same configuration.

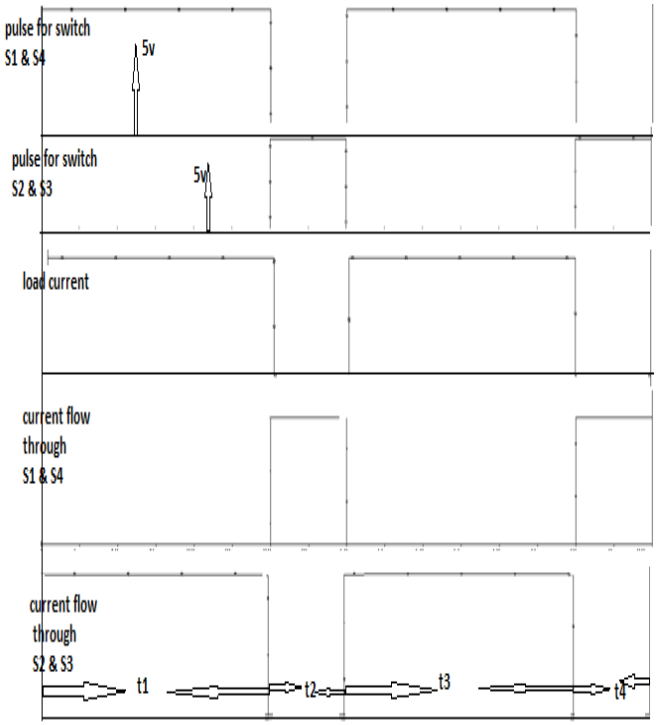

Fig. 6 Different wave shapes for 75% duty cycle

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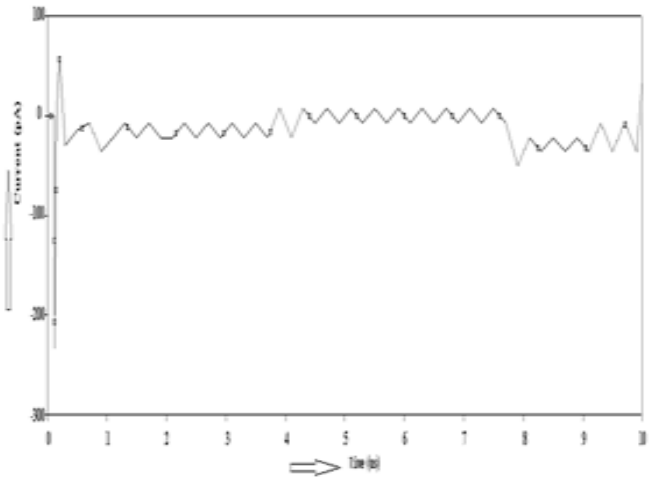

Fig. 7 (a) Leakage current for 75% duty cycle

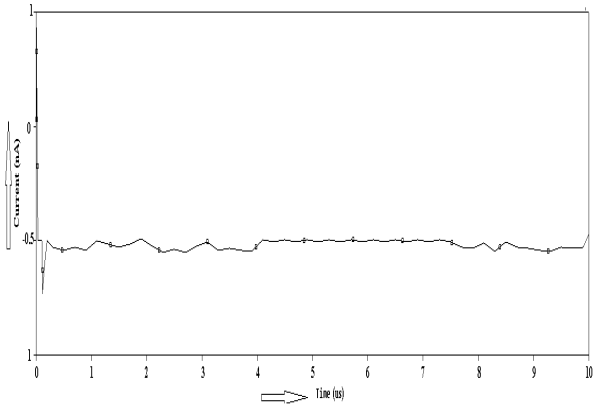

Fig. 7 (b) Leakage current for 75% duty cycle of inductor and capacitor added load

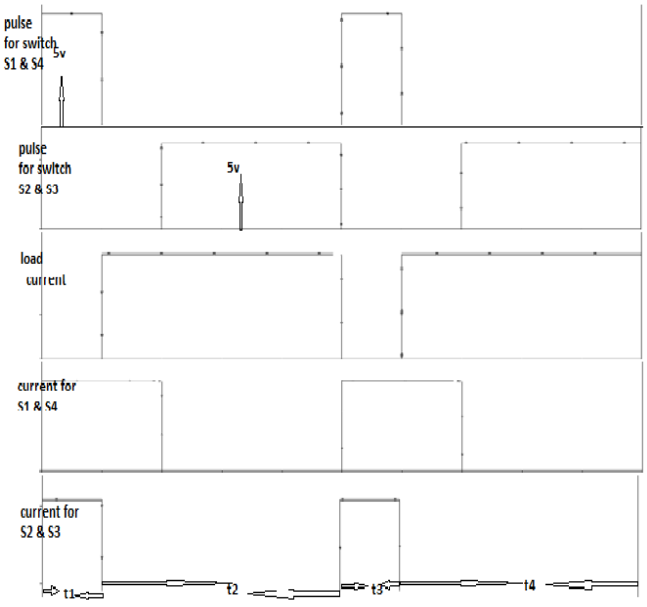

Fig. 8 Different wave shapes for 20% and 60% duty cycle for switch

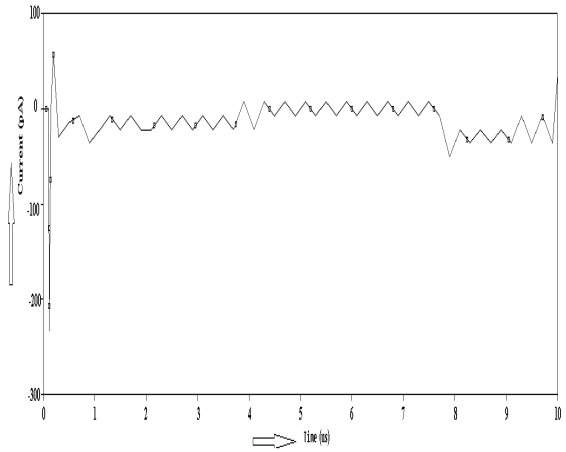

Fig. 9 (a) Leakage current for 20% (S1 and S4) and 60% (S2 and S3) duty cycle

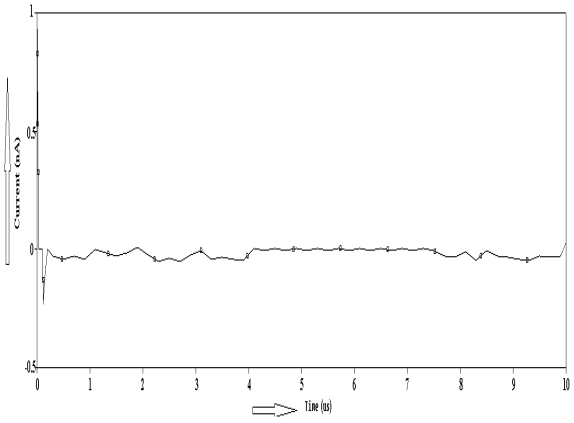

Fig. 9 (b) Leakage current for 20% (S1 and S4) and 60% (S2 and S3) duty cycle of inductor and capacitor added load

The current for 75% duty cycle is shown which is in pico range with huge fluctuation that has been shown in Fig. 7 (a).

IV. Result and Discussion

Fig. 10 shows a circuit schematic proposed that helps to reduce the leakage current from pico ampere range to femto ampere by using two extra switches with inverter. Fig. 11 shows the reduce leakage current. By using these two switches, leakage current is prevented and here on/off switching condition helps to protect or reduce to pass the leakage current that actually flow through parasitic capacitance. In positive cycle, S1 and S4 are on whereas S2 and S3 are off. On the other hand, S5 and S6 are on/off according to the Pulse, hence these two switches are works separately that actually not dependents with inverter switches and when the leakage current is occurred, these two extra using switches is helped to reduce it by their switching conditions. Pulse width/ duration modulation is shown to show how leakage current in the case of transformer-less inverter is presented here where shown the 555 timer circuit that actually used for duty cycle purposes. In a transformer-less topology

faces problem that is the leakage current through parasitic capacitance.

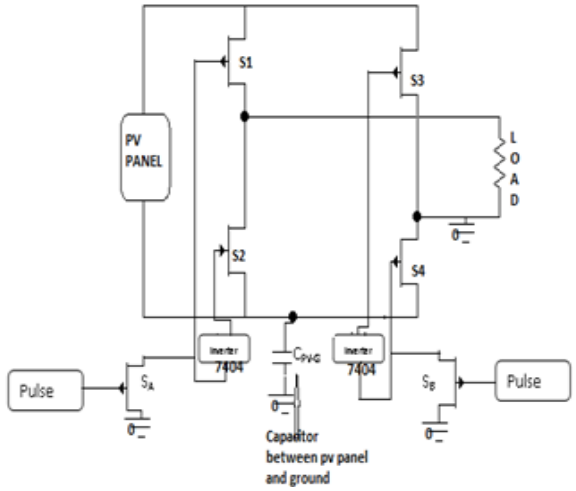

Fig. 10 Proposed loaded inverter for reducing leakage current

However, two Pulse Width Modulation (PWM0 sources are used to show the effect of leakage current in the system and how much it's possible to reduce. Here, used 50% and 75% duty cycle for making a pulse, as a result switches are on in 50% and 75%time and later we used different duty cycles in one system for operating switches (MOSFETs and IGBTs). To do so, we find out the leakage current which is actually in pico ampere range for both cases with and without using inductors and capacitor with load. After having done all of those things, here proposed an inverter system where it's clearly shown the reduction of leakage current. In addition, proposed inverter used two switches with pulse and two inverters to invert the pulse which can get from using switches. After that, it's used in for switches. Hence, the output of the leakage current shows less than previous that actually around femto range.

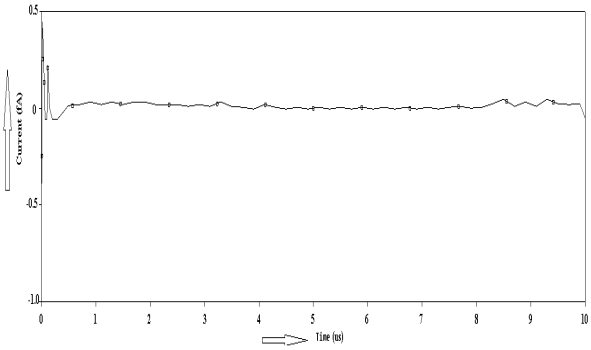

Fig. 11 Leakage current for proposed loaded inverter

V. Conclusion

PWM helps to turn on and off the switches. Hence, it's possible to get good wave form according to our need. In this paper, it's already shown that the use of PWM to find out the leakage current and variations of it. In addition, proposed a circuit diagram of an inverter that actually used to reduce the leakage current. Extensive simulation results are obtained in an attempt to produce as evidence the performance of the proposed converter topology of switches operated by given PWM reducing the effect of common mode voltage in the form of current to the ground is reduced.

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