Designing of Full Adder Using Low Power Techniques

Shashank Gautam

Abstract—This paper proposes techniques like MT CMOS, POWER GATING, DUAL STACK, GALEOR and LECTOR to reduce the leakage power. A Full Adder has been designed using these techniques and power dissipation is calculated and is compared with general CMOS logic of Full Adder.

Simulation results show the validity of the proposed techniques is effective to save power dissipation and to increase the speed of operation of the circuits to a large extent.

Keywords—Low Power, MT CMOS, Galeor, Lector, Power Gating, Dual Stack, Full Adder.

I. INTRODUCTION

IN the present era, there is a continuous development in the VLSI fabrication which has caused rapid decrease in the size and geometries of the transistors and an increase in the densities of the transistors. Due to this reason, the circuit consumes large amount of energy and many times it leads to silicon failure in the chips [1], [2].

High speed operation with low power dissipation is becoming a critical factor in the modern design of several electronic components. Different types of low power implementations are proposed in this paper. The main objective is to reduce the power losses through the methodology explained later.

II. MT CMOS

Multi-threshold CMOS (MTCMOS) is a variation of CMOS chip technology which has transistors with multiple threshold voltages (vth) in order to optimize delay or power [3]. The vth of a MOSFET is the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistor.

Low v_{th} devices switch faster, and are therefore useful on critical delay paths to minimize clock period. A common implementation of MTCMOS for reducing power makes use of sleep transistors.

Low v_{th} devices are used in the logic where fast switching speed is important. High v_{th} devices connecting the power rails and virtual power rails are turned on in active mode, off in sleep mode. High v_{th} devices are used as sleep transistors to reduce static leakage power (Fig. 1).

III. POWER GATING

Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use. In addition to reducing

Shashank Gautam is pursuing his Master of Technology degree in Electronics and Communication Engineering from Uttar Pradesh Technical University, Lucknow, India (e-mail: shashankgautam92@gmail.com).

stand-by or leakage power, power gating has the benefit of enabling Iddq testing [4].

Power gating uses low-leakage PMOS transistors as header switches to shut off power supplies to parts of a design in standby or sleep mode. NMOS footer switches can also be used as sleep transistors. Inserting the sleep transistors splits the chip's power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off. (Fig. 2)

IV. DUAL STACK

In dual stack approach two PMOS in the pull down network and two NMOS in pull up network are applied in the CMOS logic circuit. The advantage is that NMOS degrades the high logic level. Sleep transistors are sized such that any sleep transistor between vdd and a pull up network takes the size of the largest transistor in the pull up network and any sleep transistor between ground and a pull down network takes the size of the largest transistor in the pull down network [5], [6].

In other words the transistors used for dual stacking have high threshold voltages than the transistors used in the pull up and pull down network. (Fig. 3)

V. GALEOR

In this technique two gated leakage transistors are inserted between pull-up and pull-down networks of CMOS circuit. Gated leakage NMOS transistor is placed between output and pull-up circuit and a gated leakage PMOS transistor is placed between output and pull-down circuitry. The gates of these additional transistors are controlled by the drain voltages. Gated Leakage transistors cause increase in resistance of the path from Vdd to ground since one of the leakage transistors is always near its cutoff region, hence decreasing leakage current [7], [8].

This technique can also be implemented in larger circuits like memory elements by placing gated leakage transistors at the output gates. Gated leakage transistors must have threshold voltage higher than the transistors used in pull up and pull down network. (Fig. 4)

VI. LECTOR

In lector technique two "leakage control transistors" (a p-type and an n-type) are introduced within the logic gate for which the gate one of the LCTs is always "near its cutoff voltage" for any input combination. This increases the resistance of terminal of each leakage control transistor (LCT) is controlled by the source of the other (Fig. 5). In this arrangement the path from Vdd to ground leads to significant decrease in leakage currents. [9] The gate-level net list of the given circuit is first converted into a static CMOS complex

World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:9, No:4, 2015

gate implementation and then LCTs are introduced to obtain a leakage-controlled circuit.
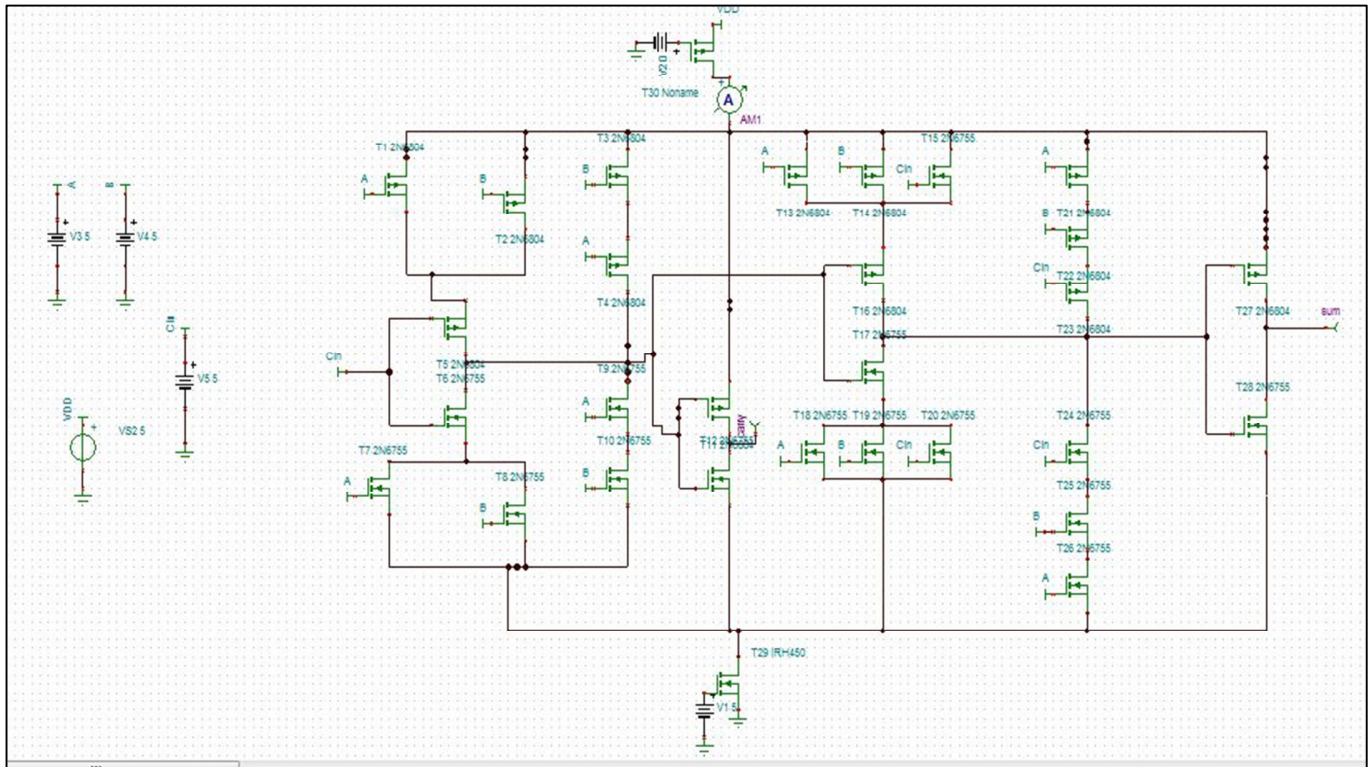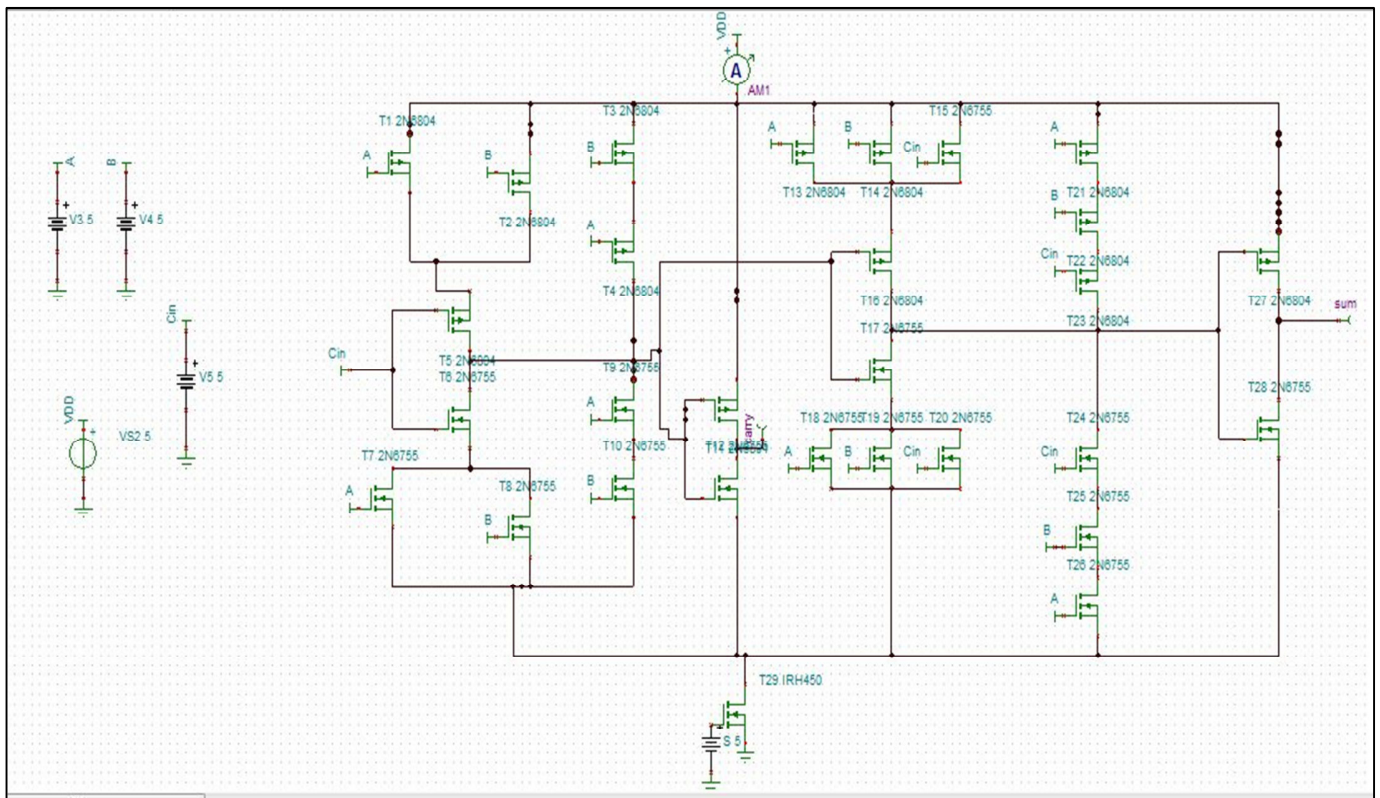

Fig. 1 Full Adder Using MT-CMOS
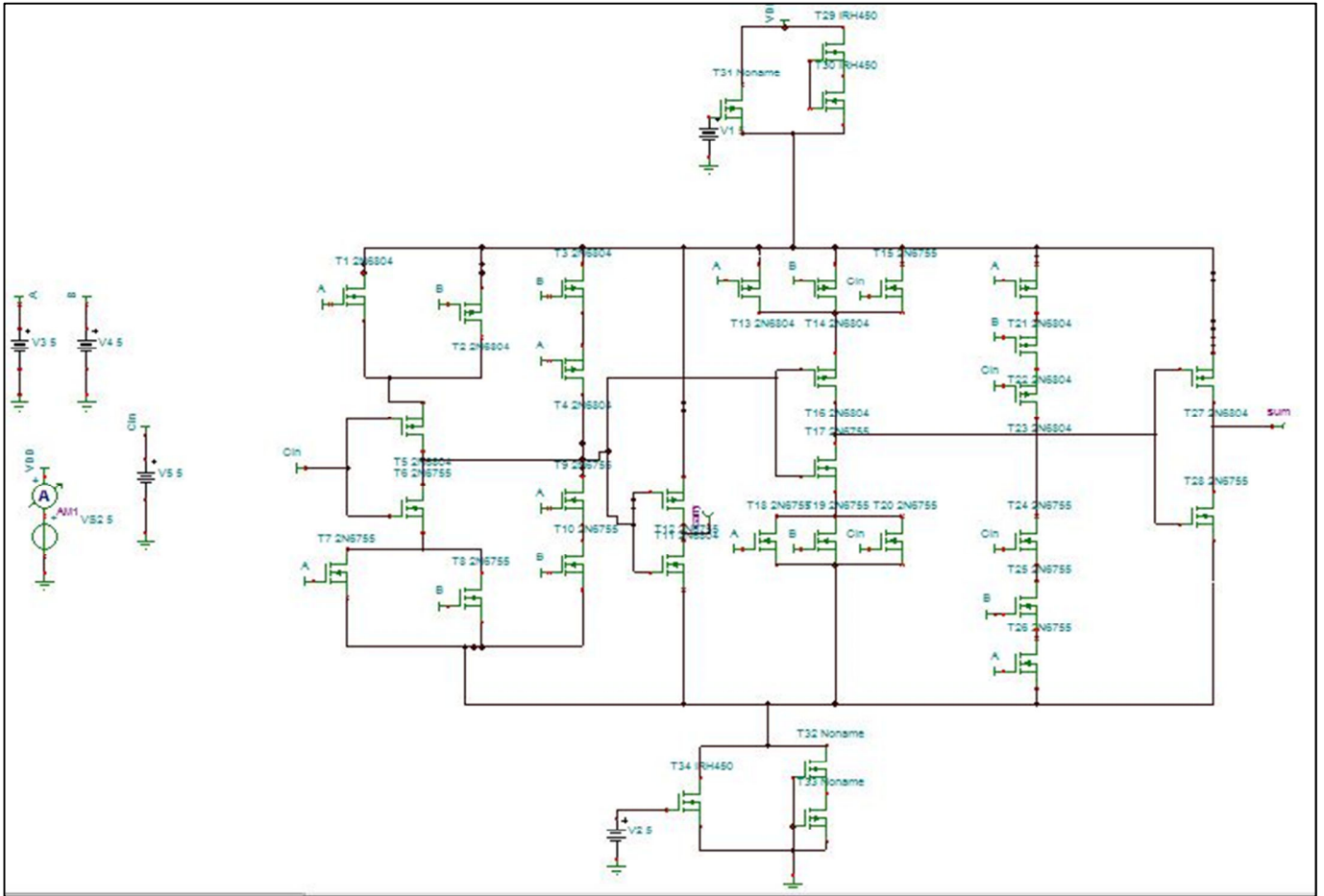

Fig. 2 Full Adder Using Power Gating

World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:9, No:4, 2015

Fig. 3 Full Adder Using Dual Stack Technique
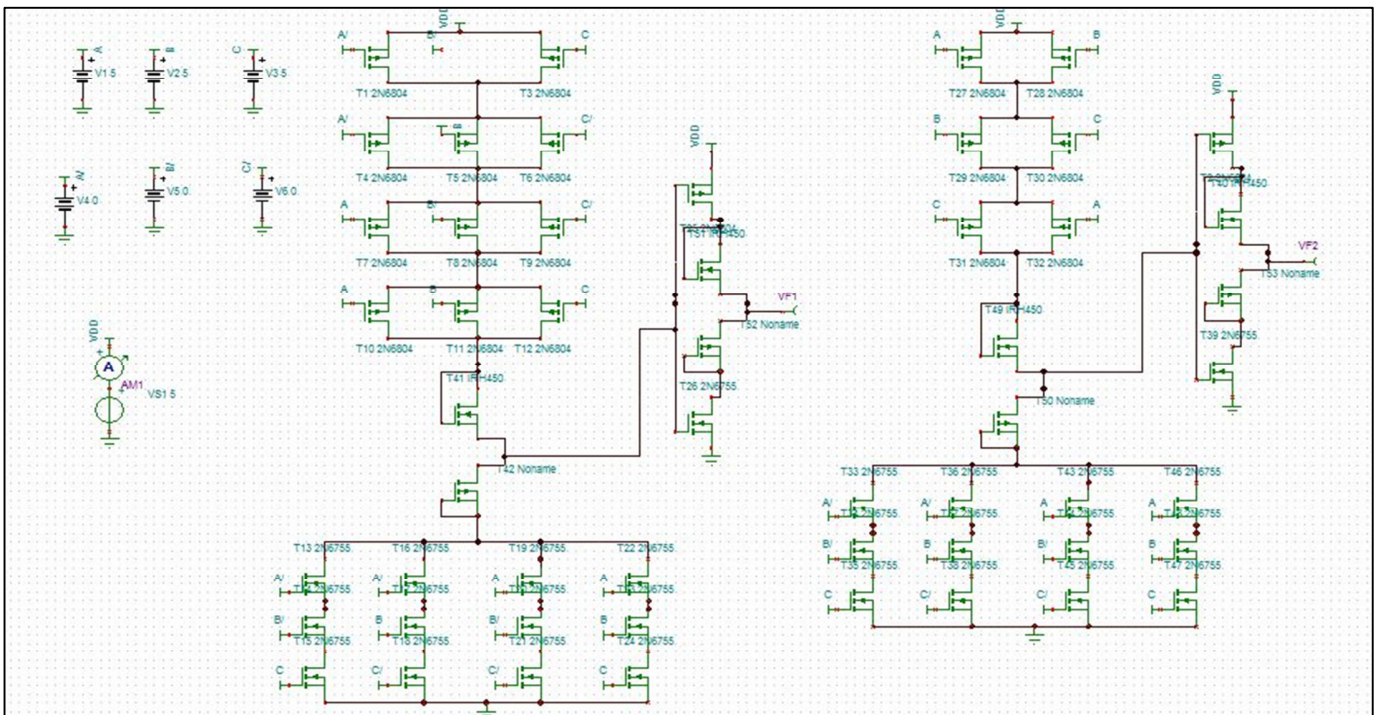
Fig. 4 Full Adder Using Galeor Technique

World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:9, No:4, 2015

The basic idea behind our approach for reduction of leakage power is the effective stacking of transistors in the path from supply voltage to ground [10], [11].

VII. SIMULATION RESULT

In this paper, several different designs are included for performance comparison analysis purpose. A new full adder implementation based on Multi Threshold CMOS, Power gating, Dual stack, Galeor and Lector techniques have been proposed in this paper, achieving high speed operation with

percentage power reduction 51.16%, 43.77%, 24.53%, 59.19%, 59.19% respectively. (Table I)

The parameter of transistor width has been fixed for all simulations of the conventional design and the proposed one as well. In each of the cases under consideration, the proposed technique has shown improvement in terms of power consumption over conventional techniques.

Simulation results show the validity of the proposed techniques is effective to save power dissipation and to increase the speed of operation of the circuits to a large extent.
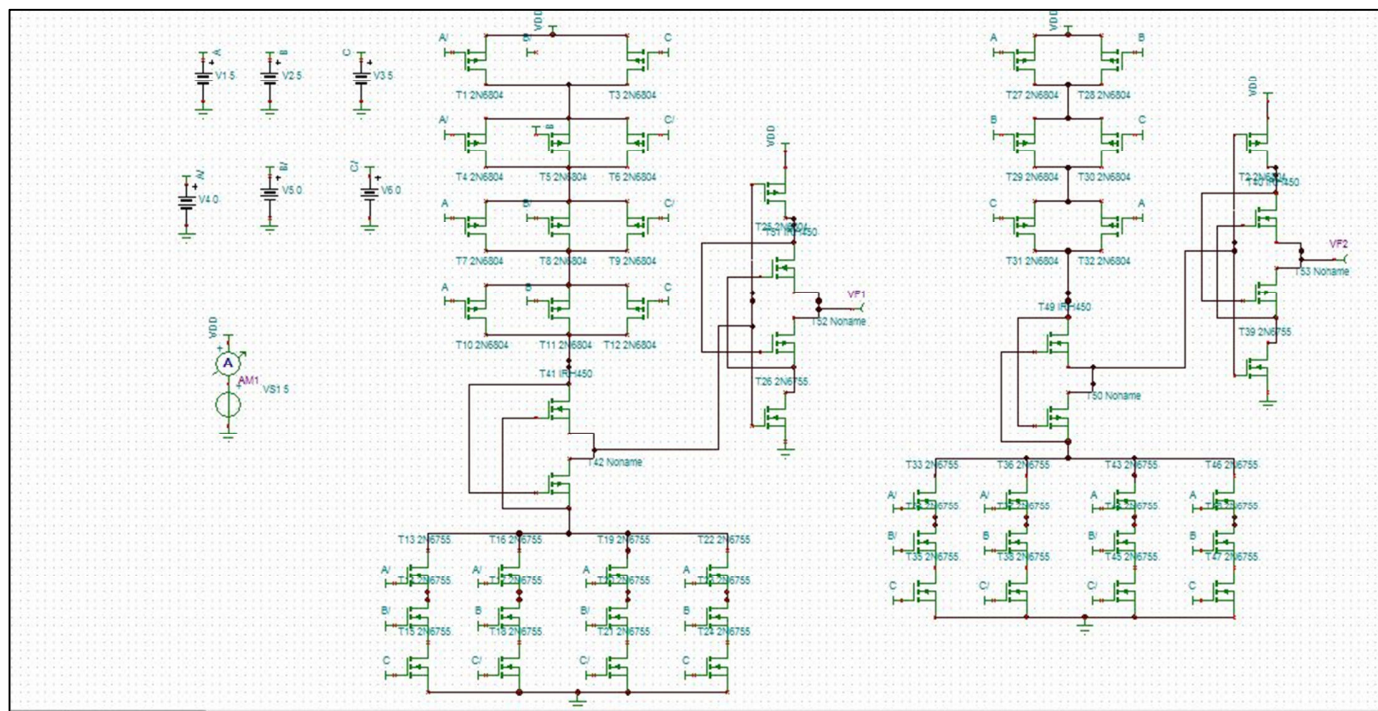

Fig. 5 Full Adder Using Lector technique

TABLE I
POWER CONSUMED AND PERCENTAGE REDUCTION

S No.	Technique used	Power consumed	Percentage Reduction
1	CMOS Circuit	94.35 uW	
2	Dual Stack	71.20 uW	24.53 %
3	Power Gating	53.05 uW	43.77 %
4	MT-CMOS	46.08 uW	51.16 %
5	Galeor	38.50 uW	59.19 %
6	Lector	38.50 uW	59.19 %

VII. CONCLUSION

In this Paper analysis of Combinational Circuit (Full Adder) is performed using five different techniques. GALEOR and LECTOR techniques are found most efficient ones among various techniques used. For Full Adder percentage power reduction comes out to be 59.19 % that is these two techniques have low power consumption than other techniques.

REFERENCES

[1] Johnson M, Somasekhar D, Chiou L-Y, et al. Leakage control with efficient use of transistor stacks in single threshold CMOS. IEEE Trans. Very Large Scale Integration. (VLSI) Syst. 1–5 Feb 2002; 10(1).
[2] Kang S. Accurate simulation of power dissipation in VLSI circuits. IEEE Journal of Solid-State Circuits. 1986; 889–91p
[3] Hyo-Sig Won, et al. An MTCMOS design methodology and its application to mobile computing. Intl. Symp. on Low Power Electronics and Design. 2003; 110–15p
[4] Saxena Chhavi, Pattanaik Manisha, Tiwari RK. Enhanced power gating schemes for low leakage low ground bounce noise in deep submicron circuits. IEEE. 2012.

[5]   Roy K, Mukhopadhyay S, Mahmoodi-Meimand H. Leakage current mechanisms and leakage reduction techniques in deep-sub-micrometer CMOS circuits. In Proc. IEEE Feb. 2003; 91: 305–27p

[6]   Park JC, Mooney III VJ, Pfeiffenberger P. Sleepy stack reduction of leakage power. Proceeding of International Workshop on Power and Timing Modeling, Optimization and Simulation. September 2004; 148–58p

[7]   Balabanian N, Carlson B. Digital Logic Design Principles. John Wily & Sons, Inc. 2001.

[8]   Zhao P, Darwish T, Bayoumi M. High-performance and low power conditional discharge flip-flop. IEEE Trans Very Large Scale Integration (VLSI) Syst. May 2004; 12(5): 477–84p.

[9]   Seta K, Hara H, Kuroda T, et al. 50% active-power saving without speed degradation using standby power reduction (SPR) circuit. In Proceedings of the IEEE International Solid State Circuits Conference. 1995

[10] Hanchate N, Ranganathan N. LECTOR: A technique for leakage reduction in CMOS circuits. IEEE Transactions on VLSI Systems Feb., 2004; 12: 196–205p.

[11] Gautam Shashank. Low Power and High Speed Techniques for Sequential Circuits. Journal of Power Electronics & Power Systems (2014) 41-45p.

Shashank Gautam received his Bachelor of Technology degree in Electronics and Communication Engineering from Uttar Pradesh Technical University, Lucknow, India in 2014. He is pursuing his Master of Technology degree in Electronics and Communication Engineering from Uttar Pradesh Technical University, Lucknow, India. He is a member of organizations like UACEE, IAENG and IACSIT etc.