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A Superior Delay Estimation Model for VLSI Interconnect in Current Mode Signaling

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Abstract**—**Today's VLSI networks demands for high speed. And in this work the compact form mathematical model for current mode signalling in VLSI interconnects is presented.RLC interconnect line is modelled using characteristic impedance of transmission line and inductive effect. The on-chip inductance effect is dominant at lower technology node is emulated into an equivalent resistance. First order transfer function is designed using finite difference equation, Laplace transform and by applying the boundary conditions at the source and load termination. It has been observed that the dominant pole determines system response and delay in the proposed model. The novel proposed current mode model shows superior performance as compared to voltage mode signalling. Analysis shows that current mode signalling in VLSI interconnects provides 2.8 times better delay performance than voltage mode. Secondly the damping factor of a lumped RLC circuit is shown to be a useful figure of merit.

Keywords**—**Current Mode, Voltage Mode, VLSI Interconnect.

I. Introduction

MODERN deep sub-micron system on chip (SoC) designs, interconnects play a dominant role in determining circuit performance and reliability. As the die size of CMOS integrated circuits continues to increase and feature sizes decrease, the performance of high speed VLSI circuits is primarily limited by the interconnect delay. Traditionally, voltage mode repeaters inserted in the long interconnects have been used to reduce the delays in signal transmission. However, there is a limit to the performance improvement that can be obtained with repeater insertion in deep submicron designs in terms of power and delay [1], [2]. Current mode signaling has been explored as an alternative for data transmission over repeater inserted interconnects [3]-[5]. In this technique, it is approximated that input resistance (R_{in}) seen by the modulated signal at the receiver end is very low (ideal value R_{in}= 0) compared to voltage mode signaling where R_{in} is very high (ideally $R_{in} = \infty$),the same concept is already used to speed up SRAM CMOS circuits [6]. In [7] Schmid, has given that researchers can explicitly apply the current mode approach. The current mode approach is mainly an alternative way of designing analog integrated circuits (ICs) and not a tool to classify circuits. Tabrizi [8] has used an efficient approach to optimize the power and delay of the global interconnects. The low swing method is optimized and used for various lengths of global interconnect. Again, [9] has proposed two accurate and efficient approaches to optimize the power and delay of global interconnects in VLSI ICs. The conventional buffer insertion and low swing methods are modified for delay and power optimizations of various length of global interconnect. Non- equidistance buffer insertion and current mode driver and receiver techniques are addressed with smart optimization procedure. Maekawa has proposed [10] solution for on-chip pulsed-current-mode transmission line interconnect (PTLI) with a stacked-switch transmitter that does not consume static power and generates return-to-zero (RZ) codes. Dave [11] has proposed that the current mode signaling is an energy efficient technique for data transmission. It is found experimentally that 6mm long link (on-chip interconnects) offers 22% improvement in delay with 81% lower energy consumption at 0.62Gbps over the voltage mode scheme. Kancharapu [12] has proposed low power low skew current mode based clock distribution network and proposed receiver consumes 35% less power than that of state of the art current mode receiver. A closed- form RC model for current mode interconnects has been derived using first order moment approximation and boundary condition matching[14], [15]. Transmission line model for delay formulation is also exploited in [16]. However, as system requirements push for the use of wider low resistance line, the inductance become increasingly dominant under fast transitions in GHz frequency range. In this case a RC delay model in [14] results in an error more than 20% compared to HSPICE simulations when operating in inductance dominated regions. But this aspect is important for current mode interconnects and therefore has been attempted in the present research work. An RLC interconnect line needs to be approximated as a RC line model using inductance-resistance equivalent model. This helps in mitigating the estimated error in [14] for GHz frequency range. Due to this the overall system performance gets improved in terms of speed.

The rest of the paper is organized as follows. In Section II inductance equivalent resistance concept is discussed. In Section III the proposed analytical model and mathematical formulation is presented for resistive load termination and damping factor is considered for accuracy. Results and their discussion are presented in Section IV. Finally conclusions are drawn in Section V.

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II. Inductance-Resistance Equivalent Model

The current mode interconnect delay expression is derived through two main steps namely, (A) absorbing the line inductance into effective resistance and (B) using transfer

function Laplace operator approach and by applying boundary conditions at source and load end of line.

The line inductance is converted into an effective resistance. In case of *RC* interconnects, the equivalent line resistance is "$R_s + R_T$". However, when inductive effect is dominant the equivalent resistance equals "$R_T + 0.65R_s + 0.36Z_0$" where the factors 0.65 and 0.36 reflect the shielding effect of inductance [13]. For delay computation the I[st] order transfer function dominant pole is evaluated, because the dominant pole decides the delay of a distributed network. Thus the equivalent resistance is given as

$$r = 0.65R_s + 0.36Z_o + R_T \quad (1)$$

where R_s is the source resistance and Z_o is the characteristic impedance ($Z_0 = \sqrt{L_T/C_T}$) and R_T, C_T and L_T represents total line resistance, capacitance and inductance discussed in Table I for any length of line.

III. Mathematical Model Formulation

A. Problem Definition

In this work a bit line delay is modeled when a read operation performed on CMOS SRAM. Current mode signaling technique is exploited for fast access/transfer of information to data line of any microprocessor/ microcontroller. For current mode signaling a system consist of a driver circuitry, interconnect line and followed by receiver circuitry having a decoding unit. The problem targeted in this work detailed in Fig. 1(a).

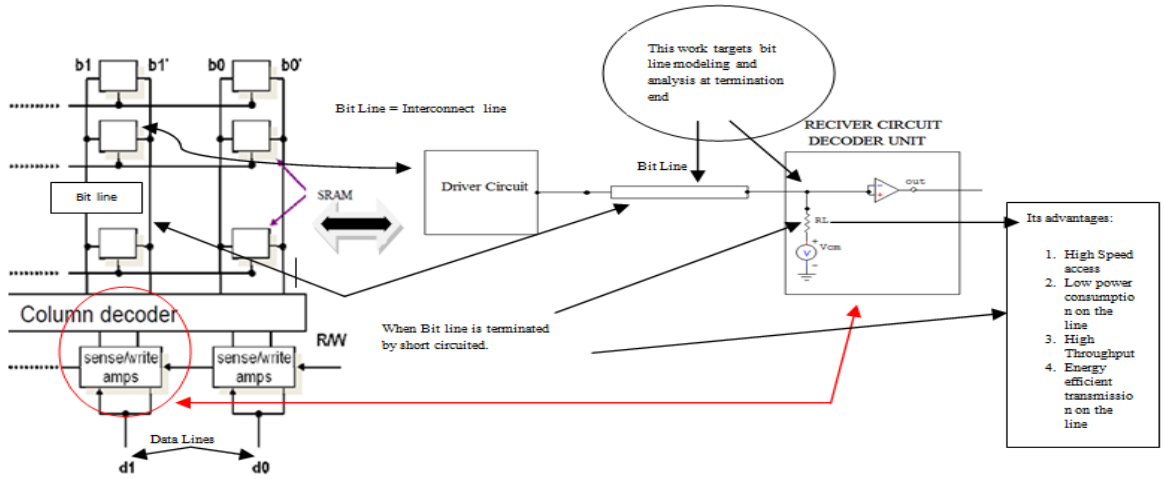

Fig. 1 (a) Analogue for the proposed problem (when SRAM transmit a signal on bit line)

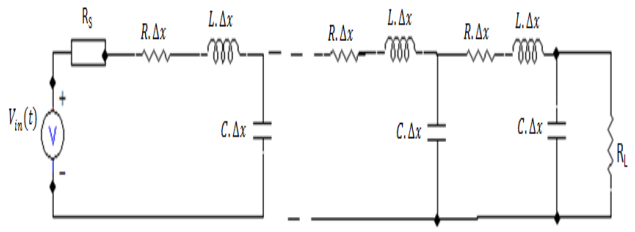

Fig. 1 (b) Current mode interconnect model

For the above analogue distributed RLC model for a current mode interconnects is shown in Fig. 1(b). Line parameters are designated *R*, *L*, and *C* as unit length resistance, inductance and capacitance respectively, $\Delta \boldsymbol{x}$ is the length of each lumped section and R_S is the source resistance. It is very much clear from literature that current mode signaling differs from voltage mode in that interconnect terminates at a finite resistance in addition to capacitive load. In this work delay model is proposed for resistive load. As shown in Fig. 1(b), the principle of current mode signaling is that by loading the line with finite impedance, the dominant pole of the system shifts, results in a smaller time constant and thus less delay. Long transmission line is modeled as a linear time invariant distributed network. Furthermore, to represent a constant current and voltage on the line the differential equations representation is used, where voltage $\boldsymbol{V(x,t)}$and $\boldsymbol{V((x+\Delta x),t)}$and current $\boldsymbol{I(x,t)}$and $\boldsymbol{I((x+\Delta x),t)}$, are represented at the source and load ends *at* $\boldsymbol{x = 0}$ and$\boldsymbol{x = d}$ (length of line) respectively. Fig. 2 shows the equivalent distributed *rc* interconnect model. Here $\boldsymbol{r}$ represent unit length equivalent resistance and $\boldsymbol{c}$ represent unit length capacitance of the interconnect.

For constant current

$$\frac{V(x,t) - V(x+\Delta x,t)}{r.\Delta x} = I(x,t)$$

For $\Delta x \to 0$

$$I(x,t) = -\frac{1}{r}\frac{\partial V(x,t)}{\partial x} \quad (2)$$

For constant voltage

$$I(x,t) - I(x+\Delta x,t) = c\Delta x \frac{\partial V(x,t)}{\partial t}$$

For $\Delta x \to 0$

$$\frac{\partial I(x,t)}{\partial x} = -c\frac{\partial V(x,t)}{\partial t} \quad (3)$$

Substituting (2) into (3), reduces to

$$\frac{\partial^2 V(x,t)}{\partial x^2} = rc\frac{\partial V(x,t)}{\partial t}$$

Thus

$$\frac{\partial^2 V(x,t)}{\partial x^2} - rc\frac{\partial V(x,t)}{\partial t} = 0 \quad (4)$$

s-domain representation of(4) is

$$\frac{\partial^2 V(x,s)}{\partial x^2} - rcsV(x,s) = 0 \quad (5)$$

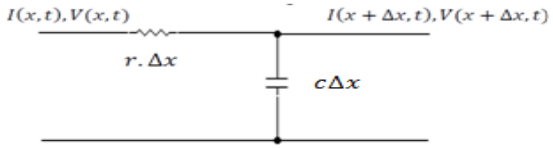

Fig. 2 Equivalent *rc* interconnect line model

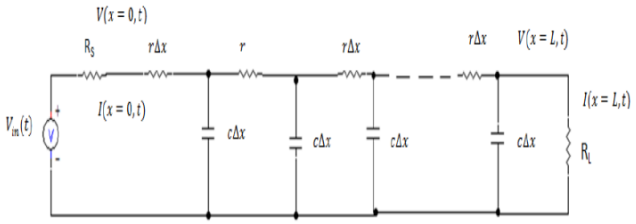

Fig. 3 Interconnect line model as a distributed line

Fig. 3 gives the *rc* distributed model of an interconnect line. $V_{in}(t)$ is the time varying input signal, and R_S is a source resistance with R_L resistive load.$r.\Delta x$ and $c.\Delta x$ represent small increments in the value of unit length resistance and capacitance down the interconnect line.The solution of partial differential equation (5) in terms of voltage and current on the line is given by

$$V(x,s) = A_{11}sinh(\sqrt{scr}x) + B_{11}cosh\,(\sqrt{scr}x) \quad (6)$$

$$I(x,s) = -\sqrt{\frac{sc}{r}}\,[A_{11}cosh\,(\sqrt{scr}x) + B_{11}sinh(\sqrt{scr}x)] \quad (7)$$

Applying the boundary conditions on (6) and (7),A_{11}, B_{11} with R_L as resistive load termination are obtained. And the boundary conditions are:

$$V_{in}(s) = V(x=0,s) + I(x=0,s)R_S$$
$$V(x=d,s) = I(x=d,s)R_L$$

$$A_{11} = -\frac{V_{in}(s)[cosh(\sqrt{scr}d) + \sqrt{\frac{sc}{r}}R_L sinh(\sqrt{scr}d)]}{\left(\frac{scR_LR_S}{r}+1\right)sinh(\sqrt{scr}d) + \sqrt{\frac{sc}{r}}(R_L+R_S)cosh(\sqrt{scr}d)}$$

$$B_{11} = \frac{V_{in}(s)[sinh(\sqrt{scr}d) + \sqrt{\frac{sc}{r}}R_L cosh(\sqrt{scr}d)]}{\left(\frac{scR_LR_S}{r}+1\right)sinh(\sqrt{scr}d) + \sqrt{\frac{sc}{r}}(R_L+R_S)cosh(\sqrt{scr}d)}$$

On calculation (6) and (7) can be reproduced as (8):

$$\frac{V(x=d,s)}{V_{in}(s)} = \frac{\sqrt{\frac{sc}{r}}R_L}{\left(\frac{scR_LR_S}{r}+1\right)sinh(\sqrt{scr}d)+\sqrt{\frac{sc}{r}}(R_L+R_S)cosh(\sqrt{scr}d)} \quad (8)$$

Let $\sqrt{scr}d = u$

This leads to

$$\frac{V(x=d,s)}{V_{in}(s)} = \frac{\frac{u}{dr}R_L}{\left(1+\frac{u^2}{r^2d^2}R_LR_S\right)sinh(u) + \frac{u}{dr}(R_L+R_S)cosh(u)}$$

$$\frac{V(x=d,s)}{V_{in}(s)} = \frac{1}{\left(\frac{rd}{uR_L}+\frac{u}{rd}R_S\right)\left(\frac{e^u-e^{-u}}{2}\right)+\left(1+\frac{R_S}{R_L}\right)\left(\frac{e^u+e^{-u}}{2}\right)} \quad (9)$$

Rewriting (8) as:

$$f(u) = \left(\frac{a}{u}+bu\right)\left(\frac{e^u-e^{-u}}{2}\right) + c\left(\frac{e^u+e^{-u}}{2}\right) \quad (10)$$

where,

$$a = \frac{rd}{R_L} = \frac{R_1}{R_L},\quad b = \frac{R_S}{rd} = \frac{R_S}{R_1},\quad c = (1+\frac{R_S}{R_L})$$

On simplifying (10), it gives:

$$f(u) = 1/2[e^u\left(\frac{a}{u}+bu+c\right) + (c-bu-\frac{a}{u})e^{-u} \quad (11)$$

By solving (11), $f(u)$ finally reduces to

$$f(u) = (a+c) + \left(b+\frac{c}{2!}+\frac{a}{3!}\right)u^2 + \left(\frac{b}{3!}+\frac{c}{4!}+\frac{a}{5!}\right)u^4 + \left(\frac{b}{5!}+\frac{c}{6!}+\frac{a}{7!}\right)u^6 + \cdots\ldots\ldots\ldots \quad (12)$$

Substituting the value of $u = \sqrt{scr}d$; $cd = C_1$, Total capacitance of interconnect line of length'd'.$rd = R_1$, Total effective resistance of interconnect line of length'd', and (12) becomes:

$$f(u) = (a+c) + \left(b+\frac{c}{2!}+\frac{a}{3!}\right)C_1R_1s + \left(\frac{b}{3!}+\frac{c}{4!}+\frac{a}{5!}\right)(C_1R_1)^2s^2 + \left(\frac{b}{5!}+\frac{c}{6!}+\frac{a}{7!}\right)(C_1R_1)^3s^3 + \cdots\ldots\ldots\ldots \quad (13)$$

Thereby the distributed network is further approximated to a first order transfer function as shown below where a_1 is the dominat pole that determines the delay of the line.

$$\frac{V(x=d,s)}{V_{in}(s)} = \frac{1}{(a+c)+\left(b+\frac{c}{2!}+\frac{a}{3!}\right)C_1R_1s} \quad (14)$$

First order transfer function is equivalent to

$$\frac{V(x=d,s)}{V_{in}(s)} = \frac{K_1}{s+a_1} = \frac{V_{dd}}{s}\left(\frac{K_1}{s+a_1}\right) \quad (15)$$

Finally, system response is converted into time domain and gives:

$$V(x=d,t)=\frac{V_{dd}}{a+c}[1-e^{-a_1 t}]u(t) \quad (16)$$

Hence the delay time is computed as:

$$\tau_d=\frac{1}{a_1}=\frac{\left(b+\frac{c}{2!}+\frac{a}{3!}\right)}{a+c}C_1R_1 \quad (17)$$

Substituting the values of value of *a, b,* and *c*, (17) reduces to:

$$\tau_d=\frac{[\frac{R_S}{R_1}+\frac{1}{2}\left(1+\frac{R_S}{R_L}\right)+\frac{1R_1}{6R_L}]C_1R_1}{[\frac{R_1}{R_L}+\left(1+\frac{R_S}{R_L}\right)]} \quad (18)$$

B. Damping Factor

For current mode signalling, a lumped system model can be used for the approximate evaluation of the line inductance effect .This analysis of an *RLC* transmission line is compared to the analysis of a lumped *RLC* circuit [21].

The interconnect is modelled as a lumped RLC circuit with R_T= *R*.d, L_T= *L*.d, C_T= *C*.d as shown in Fig. 4.

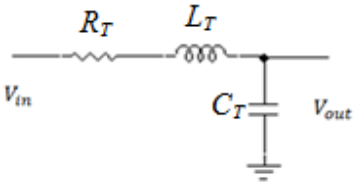

Fig. 4 Lumped *RLC* circuit model of an Interconnect line

The poles of the circuit are

$$P_{1,2}=\omega_0[-\xi\pm\sqrt{(\xi^2-1)}] \quad (19)$$

and the damping factor ξ is

$$\xi=\frac{R.d}{2}\sqrt{\frac{C}{L}} \quad (20)$$

As (19) implies, if ξ is greater than one, the poles are real and the effect of the inductance on the circuit is small. The greater the value of ξ, the more accurate the*rc* model become.

On the other hand, as ξ become less than one, the poles become complex and oscillation occur. In that case, the inductance cannot be neglected. This relationship is physically intuitive, since ξ represents the degree of attenuation the wave suffers as it propagates a distance equal to the length of the line. As this attenuation increase, the effect of the reflections decrease and the *rc*model becomes more accurate. Therefore ξ is useful figure of merit that anticipates the importance of considering in a particular interconnect line.

IV. Results and Discussion

The various results obtained are presented in this section. Their implications are also given. In order to verify the analytical results, simulations of the *RLC* line modeled in Fig. 3 i.e. *rc* line are performed. Using PTM parameters for interconnects in 180nm technology node, the results are evaluated for 2mm to 10mm length of global interconnect [15]. For proposed model validation the parameters used are detailed in Tables I and II. Table II gives the computation of inductance effect into equivalent resistance and the change in unit length resistance is also detailed. R_S = 2.5k is used in the analysis. Different results are computed from the analytical model by using MATLAB (7.80) [18]. Furthermore the results are verified by SPICE simulations [20]. Analyses show that the proposed delay model is in close agreement to the simulation results. The various case studies which validate the proposed model are presented in this section.

TABLE I
The Values of Interconnect Line Parameters Using PTM [19]

(d) (mm)	$R_T(\Omega)$	C_T (F)	L_T (H)	$r'(\Omega/m)$	$c(F/m)$	$l(H/m)$
2	44	0.487p	3.23n	22k	243p	1615n
4	88	0.975p	7.015n	22k	243.75p	1753.75n
6	132	1.462p	11.00n	22 k	243.67p	1833.33n
8	176	1.950p	15.14n	22 k	243.75p	1892.5n
10	220	2.437p	19.37n	22k	243.7p	1937n

TABLE II
Inductance Conversion into Equivalent Resistance

$Z_o=\sqrt{L_T/C_T}$	$X_{Leff}=0.36Z_o/L$ (Ω/m)	r= r'+ X_{Leff}	$0.65R_S$ (Inductance effect included)
81.440	14.65k	36.65k	1.625k
84.823	7.634k	29.63k	1.625k
86.741	5.204k	27.20k	1.625k
88.114	3.965k	25.96k	1.625k
89.1532	3.21k	25.21k	1.625k

Case 1: In Fig. 5 the delay variation with interconnect length for current mode signaling with (R_L=0) i.e. ideally load resistance must be zero is shown. This result is computed by proposed analytically model (18) for current mode interconnect. The results of the proposed model are compared with existing current model in literature [15]. It is concluded that the proposed model shows speed improvement when compared to that in [15]. With variation in the length of interconnect the detailed results are shown in Table III. This improvement in delay factor is because moment approximation method is used in [15] while the proposed model overcomes the approximation.

Case 2: For voltage mode ideally load is terminated by infinite resistance (R_L = infinite) which is practically not possible. The value of R_L has been approximated in range 1kΩ to 5KΩ for voltage mode signaling. Delay value for voltage mode signaling is detailed in Table IV. Delay variation with interconnect length for R_L = 200 to 5kΩ is shown in Fig. 6 and6 respectively. From these figures it is inferred that for larger values of load resistance, the system response goes sluggish. Therefore, system demands for smaller values of load impedance for quicker response.

Case 3: In Fig. 7 the delays obtained by voltage and current mode system are compared. It is found that current mode signaling is far better than voltage mode signaling for data

transmission over longer interconnects is detailed in Table V. It is completely high speed data transmission system. Longer interconnect lengths for instance 10 mm current mode (CM) system gives 14.68 times lesser delay than voltage mode at R_L= 5kΩ.

Case 4: For $R_L = R_T = R_I$, total line resistance. The delay is almost three time the current mode value (R_L=0). It is still less than voltage mode signaling. This is according to results shown in Fig. 8. At 10mm interconnect length it is found that at $R_L = R_I$, the delay is 0.8012ns, which is 2.77 times the proposed current mode system at R_L = 0 where delay is 0.288ns.

Case 5: Fig. 9 shows the variation of delay with load resistance as a variable. It is found that increase in the value of load, makes the system slower. It means that only for smaller value of impedance the system will respond faster. A comparative analysis of the proposed mathematical model and SPICE simulation results is carried for *RLC* interconnects and shown in Fig. 10. The value of N for distributed network is taken 1001 [17]. The simulation results deviate from the proposed model by 0.01%, 3.57%, 4.38%, 5.61% and 6.44% for 2mm, 4mm, 6mm, 8mm, and 10mm lengths of interconnect line respectively. The average error is 3.96% between the proposed model and the SPICE simulations. This shows fairly good agreement between the two.

V. Conclusion

In this paper a novel analytical delay model for current mode signaling is developed and presented. By using this proposed model dominant pole is computed from the first order system function. It is analyzed for different current mode circuit parameters to determine the nature of current mode circuits. It is also observed that with the increase in the length of interconnect the simulation results deviate from the proposed model by 3.96%. For load resistance equal to total equivalent resistance of RLC lines the system delay is still smaller than voltage mode signalling. The delay at R_L=0 is 2.8 times lesser than the current mode delay at $R_L = R_T$. Finally, it is concluded that the use of current mode techniques can lead to significant speed enhancement in long VLSI interconnects. This proposed current mode technique can significantly impact chip access times and architecture trade-offs for future fast CMOS SRAM design. Current mode signal receivers can be used to significantly reduce the line delays in CMOS VLSI chips. Secondly, figure of merit have been developed that determine the relative accuracy of a $R_{Teff}C_T$ model of on-chip interconnects. The derived expression along with accuracy analysis can serve as a convenient tool for delay estimation with minimal computation during design.

TABLE III
Delay Obtained Using the Proposed Analytical versus Existing Model

Length (mm)	Delay (ns)[15] (R_L=0 Ω)	Analytical Delay (ns) (R_L=0 Ω)	Simulation delay (ns)	% Decrease in delay value of Col. 3 compared to Col. 2. (ns)	% of Relative error Analytical v/s Simulation	Delay (ns) at $R_L=R_I$
2	0.021	0.017	0.017	19.04	0.01	0.1262
4	0.062	0.056	0.058	9.677	3.57	0.2653
6	0.123	0.114	0.119	7.31	4.38	0.4309
8	0.201	0.192	0.203	4.47	5.61	0.6083
10	0.297	0.288	0.307	3.03	6.44	0.8012

TABLE IV
Delay for Different Length of Interconnect for Voltage Mode Signaling

Length (mm)	Delay				
	R_L=1kΩ	R_L =2kΩ	R_L =3kΩ	R_L =4kΩ	R_L =5kΩ
2	0.358ns	0.550ns	0.673ns	0.759ns	0.822ns
4	0.717ns	1.092ns	1.333ns	1.502ns	1.626ns
6	1.114ns	1.684ns	2.053ns	2.311ns	2.502ns
8	1.510ns	2.268ns	2.760ns	3.105ns	3.361ns
10	1.917ns	2.860ns	3.476ns	3.909ns	4.230ns

TABLEV
Comparison between Voltage and Current Mode Interconnect Delay for (R_L= 1KΩ)

Line Length (mm)	CM delay (ns)	VM delay (ns)
2	0.017	0.358
4	0.056	0.717
6	0.114	1.114
8	0.192	1.510
10	0.288	1.917

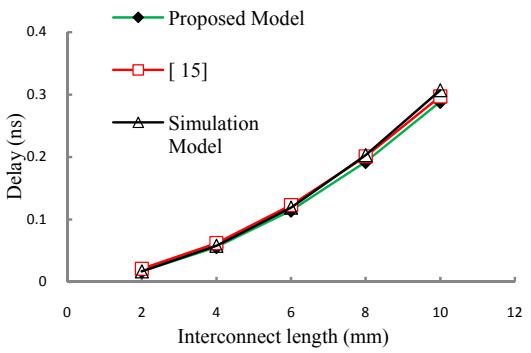

Fig. 5 Delay comparison between proposed and existing model

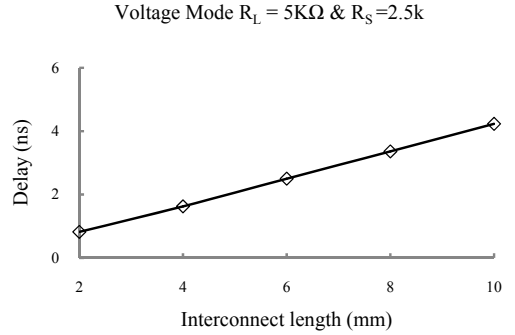

Fig. 6 Delay variations for Voltage mode with interconnect length

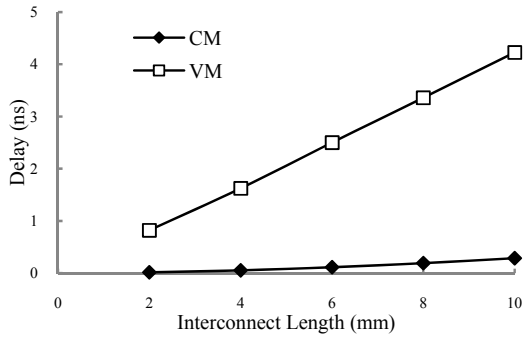

Fig. 7 Delay variation with interconnect length for current and voltage mode signaling

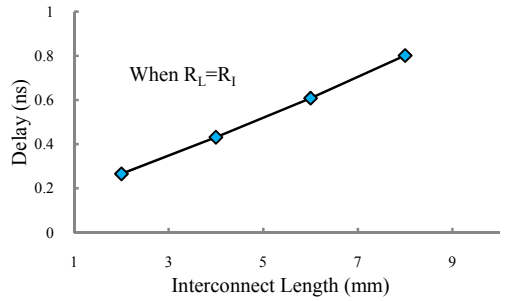

Fig. 8 Delay versus interconnect length when load impedance equal to line impedance

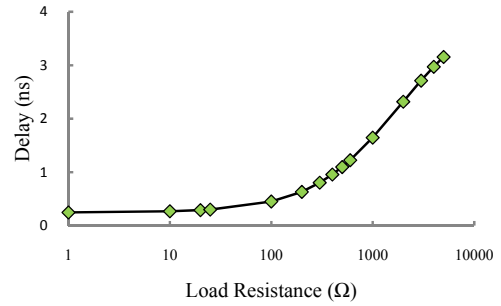

Fig. 9 Delay variation with load resistance for CM signalling

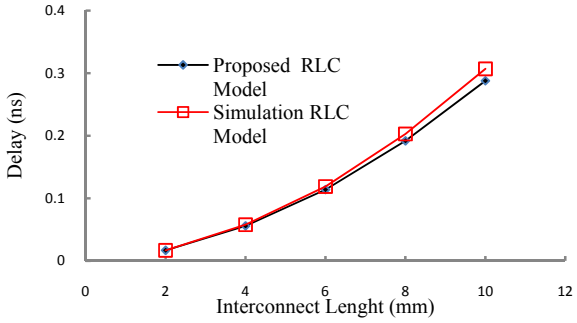

Fig. 10 Analytical versus simulation results for delay variation with interconnect length

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REFERENCES

[1] D.Liu and C. Svensson Power Consumption Estimation in CMOS VLSI Chips. IEEE Journal of Solid State Circuits1994,29(6),pp. 663–670.
[2] D. Sylvester and K. Kuetzer "Getting to the Bottom of Deep Submicron II: The Global Wiring Paradigm". *in Proc. International Symposium on Physical Design*, April 1999, pp. 193–200.
[3] R. Bashirullah, W. Liu, and R. K. Cavin Current Mode Signaling in Deep Submicrometer Global Interconnects. IEEE Transactions on VLSI Systems,2003, 11(3) pp. 406–417.
[4] I. Dhaou, M. Ismail, and H. Tenhunen. Current Mode, Low Power, On-Chip Signaling in Deep Sub-micron CMOS Technology. IEEE Transactions on Circuits and Systems, 2001, 50(3) pp. 397–406.
[5] V. Venkatraman and W. Burleson, Robust Multi-Level Current-Mode On-Chip Interconnect Signaling in the Presence of Process Variations, *inProc. of Sixth International Symposium on Quality Electronic Design*, March 2005, pp. 522–527.
[6] E. Seevinck, P. van Beers, and H. Ontrop. Current Mode Techniques for High Speed VLSI Circuits with Application to Current Sense Amplifier for CMOS SRAMs. in IEEE Journal Of Solid State Circuits, 1991, 26(4)pp. 525–536.
[7] H.Schmid, Why the terms 'Current mode' and 'voltage Mode' Neither Divide nor qualify circuits, *in Proc. of IEEE*, 2002, pp. 29-32.
[8] M.M Tabrizi, N. Masoumi, M. Deilami, High Speed Current Mode Signalling for Interconnects Considering transmission line and Crosstalk effects, in *Proc. of IEEE* 2007, pp. 17-20.
[9] M.M Tabrizi, N. Masoumi, Low-power and high-performance techniques in global interconnect signalling in Microelectronics Journal, (2009) pp.1-9.
[10] Tomoaki Maekawa et al., Highly Energy-Efficient On-Chip Pulsed-Current-Mode Transmission Line Interconnect, solid state circuit technologies (book), pp 263-280, January 2010.
[11] Marshnil Dave et al., Energy efficient current mode signaling scheme, IEEE Asian Solid State circuit conference, November 8-10, 2010.
[12] Naveen K.Kancharapu et.al, A Low-Power Low Skew Current-Mode Clock Distribution Network in 90nm CMOS Technology, in *IEEE Proc*. ISVLSI 2011, pp 132-137.
[13] R.Venkatesan, J. Davis, and J.Mendil, Compact distributed RLC interconnect models part IV: unified models for time delay, crosstalk, and repeater insertion, IEEE Trans. Electron Devices, 50 (2003) pp. 1094-1102.
[14] R. Bashirullah, W. Liu, and R. K., Delay and power model for current mode signaling in deep submicron global interconnects, Proceedings of IEEE Custom Integrated Circuits Conference, May 2002, pp. 513-516.
[15] M.Zhou,W.Liu and M.Sivaprakasam,A Closed-form Delay Formula for On-Chip RLC Interconnectsin Current-Mode Signaling in *IEEE Proc. 2005,* pp 1082-1085.
[16] S.Jadav,M.Vashishth, Rajeevan Chandel, Close form delay model for on chip signalling with resistive load termination using: Current mode technique" in *IEEE Proc.* of ICIIS 2014, pp-1-6.
[17] M. Ismail, N. Tan, Modeling Techniques for energy efficient system-on-a- chip signaling, *IEEE Circuits and Device Magazine*, 19 (2003) pp. 8-17.
[18] MATLAB version R2009a Online, http://mathwork.com, 2013.
[19] PTM models online: http://www.berkely edu.com, 2013.
[20] Tanner EDA tools online: http:// tannereda.com, 2013.
[21] Y. Ismail, E. Friedman, and J. Neves, "Figures of Merit to Characterize the Importanceof On-Chip Inductance," IEEE Trans. On VLSI system, vol. 7(4), 1999, pp. 442-449.