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Stabilization Technique for Multi-Inputs Voltage Sense Amplifiers in Node Sharing Converters

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***Abstract*—**This paper discusses the undesirable charge transfer through the parasitic capacitances of the input transistors in a multi-inputs voltage sense amplifier. Its intrinsic rail-to-rail voltage transitions at the output nodes inevitably disturb the input sides through the capacitive coupling between the outputs and inputs. Then, it can possible degrade the stabilities of the reference voltage levels. Moreover, it becomes more serious in multi-channel systems by altering them for other channels, and so degrades the linearity of the overall systems. In order to alleviate the internal node voltage transition, the internal node stabilization techniques are proposed. It achieves 45% and 40% improvements for node stabilization and input referred disturbance, respectively.

***Keywords*—**Voltage sense amplifier, multi-inputs, voltage transition, node stabilization, and biasing circuits.

I. Introduction

VOLTAGE sense amplifiers are widely used circuit blocks to generate firm decisions from a meaningful input analog signals. There are lots of different types of voltage sense amplifiers, and they are widely used in various fields such as memories, display driver, data converters, communication transceivers, and so on [1]-[4].

Each structure has its own advantages and disadvantages. Depending on the existence of static currents, voltage sense amplifiers can commonly be divided into two categories. First, the static voltage sense amplifiers use the static biasing current, and so its power consumption is high and probably not tolerable in nowadays mobile environment. On the other hand, the dynamic latch-type voltage sense amplifier can save its power consumption because it breaks the continuous current path. Due to its high power efficiency and rail-to-rail output swing, the dynamic latch-type voltage sense amplifier gains more popularity nowadays. However, its full-scale output swing can possible create unacceptable input-referred disturbance through the coupling capacitances. This phenomenon can be more serious when a voltage sense amplifier has multi-input terminals, which is useful to reduce the switching sequences and increase the decision speed. The node stabilization techniques for a multi-input voltage sense amplifier are proposed in the paper to reduce the input referred disturbance.

This paper is organized as follows: Section II shows a popular dynamic latch-type voltage sense amplifier to explain the sources of node disturbance, and present a multi-inputs voltage sense amplifier. The node stabilization technique and design procedures are presented in Section III. The conclusions are shown in Section IV.

II. Consideration of Node Disturbance

A. Dynamic Latch-Type Voltage Sense Amplifier

A dynamic latch-type voltage sense amplifier consists of pre-amplifier and dynamic latch stages in the top [5], [6]. Its operation is solely controlled by the CLK signal, and exhibits two distinguished reset and decision phases. Despite of numerous advantages of the dynamic latch-type voltage sense amplifier, the direct coupling between the pre-amplifier and latch stages can possibly create a serious input referred disturbance or noise. This input disturbance becomes more critical in multi-channel system because it manipulates the reference voltage levels that can possible result in a wrong decision in neighboring channels.

The input referred disturbance due to full scale output transitions can be mitigated by separating the structure. A double-tail voltage sense amplifier shows the lower input referred disturbance by separating the pre-amplifier stage and dynamic latch stages in Fig. 1 [7]. Moreover, its separating structure seems more applicable to low voltage deep sub-micron CMOS technologies. The intermediate transistors M_6 and M_7 are inserted to transfer the signals from the pre-amplifier to the dynamic latch stages, and also mitigate the abrupt disturbance from the dynamic latch-type stage to the pre-amplifier stage. However, the input referred disturbance may be insufficiently suppressed even in the double-tail dynamic latch-type voltage sense amplifier in Fig. 1 for the multi-channel systems which share the reference nodes for each sub-channel.

There are two main sources that transfer the internal voltage fluctuations into the input sides, resulting in inevitable input disturbance. First, the gate-drain parasitic capacitances C_{gd2} and C_{gd3} of the input differential pair in Fig. 1 create the input referred noise. The charge transfer through the C_{gd2} and C_{gd3} mainly results from the dynamic latch operation. The rapid voltage divergence at the output nodes can affects the input nodes. Especially when the positive feedback in the dynamic latch is not sufficiently strong, the unbalanced voltage fluctuation is leaked to the input sides through the C_{gd2} and C_{gd3}, so that it may have a chance to invert the final decisions,

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degrading the overall system performance. The other sources of the input referred noise are the parasitic gate-source capacitances C_{gs2} and C_{gs3} of the differential pair in the pre-amplifier stage. As mentioned earlier, the common source node of the differential pair is floating during the reset phase. When the CLK goes high, M_1 should reconstruct the current path and the common source node of the differential pair should drop to ground immediately. Then, a large amount of charge is interacted with the input nodes through C_{gs2} and C_{gs3}, and then the input referred disturbance generates. Moreover, the input differential pair transistors M_2 and M_3 have different capacitance sizes of C_{gs2} and C_{gs3} because the differential voltage levels are applied to the differential input nodes. Thus, different amounts of the input referred disturbance can possible worsen the conversion linearity.

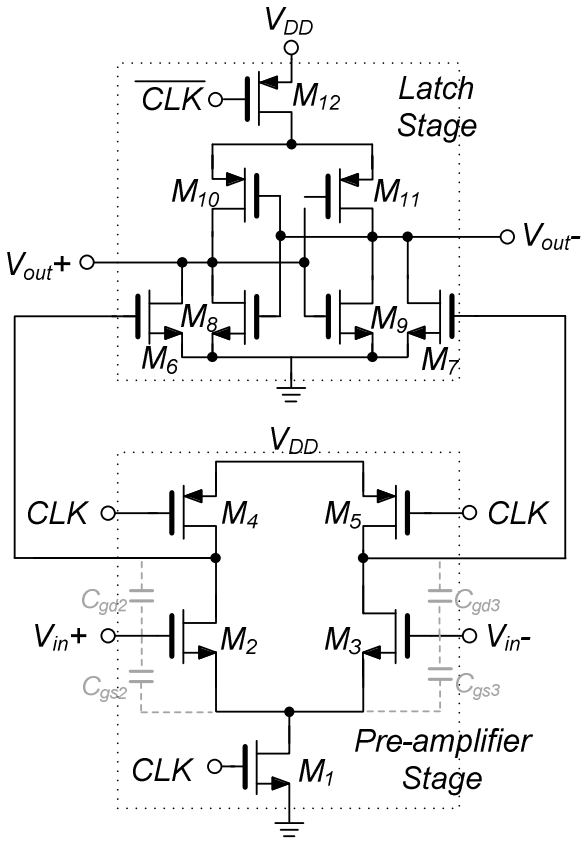

Fig. 1 A double-tail voltage sense amplifier

B. Multi-Inputs Voltage Sense Amplifier

A double-tail dynamic latch-type voltage sense amplifier can be expanded, and sense and compare multi-input voltage levels. The double-tail dynamic latch-type voltage sense amplifier with dual differential inputs is especially useful when the differential input pair should be compared with the differential reference levels without excess switching steps to fit in a typical single differential pair input [8], [9]. Fig. 2 shows the multi-inputs double-tail dynamic latch-type voltage sense amplifier by expanding the input side with dual differential pairs. Since it can directly compare the multi-input signals, the comparison time can be minimized. It can be important feature for the systems which operate in successive comparisons.

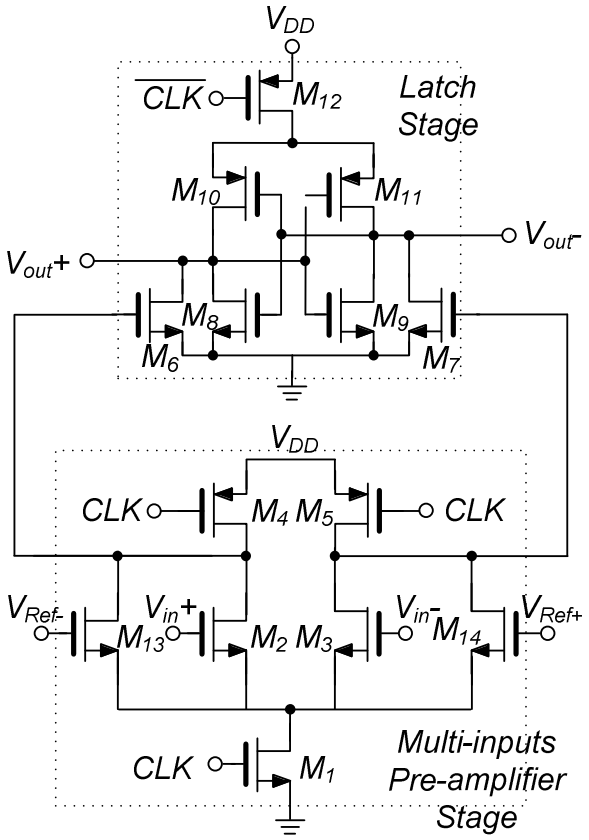

Fig. 2 Multi-inputs double-tail dynamic latch-type voltage sense amplifier

The multi-inputs double-tail dynamic latch-type voltage sense amplifier can be more vulnerable to the node disturbance at the source and drain nodes of the differential pairs due to doubled input transistors, although it is more convenient and faster due to efficient switching steps. Therefore, the node stabilization techniques should be carefully considered. Fortunately, the node disturbance phenomena are quite similar with those in the double-tail dynamic latch-type voltage sense amplifier.

III. Node Stabilization Techniques

A. Latch Disturbance Suppression Technique

The main sources for the input-referred disturbances are the node voltage fluctuation at drain and source sides of the input differential pair, as explained earlier. The drain side fluctuation is mainly due to the gate-drain parasitic capacitances of the input differential pairs, which are given by

$$Cgd,i = \frac{1}{2} C_{OX} WiLi, \quad (1)$$

where W, L, and C_{OX} denote width, length, and the oxide capacitance, respectively. The subscript, i, denotes the number of transistors in the input differential pairs. Since the output nodes of the pre-amplifier stage are clamped to VDD during the

reset phase and diverge to the supply levels during the decision phase, its abrupt large voltage transition is coupled to the input sides through gate-drain parasitic capacitances of the input differential pairs and results in the input referred disturbance. It may have a chance to invert the final decisions, degrading the overall system performance.

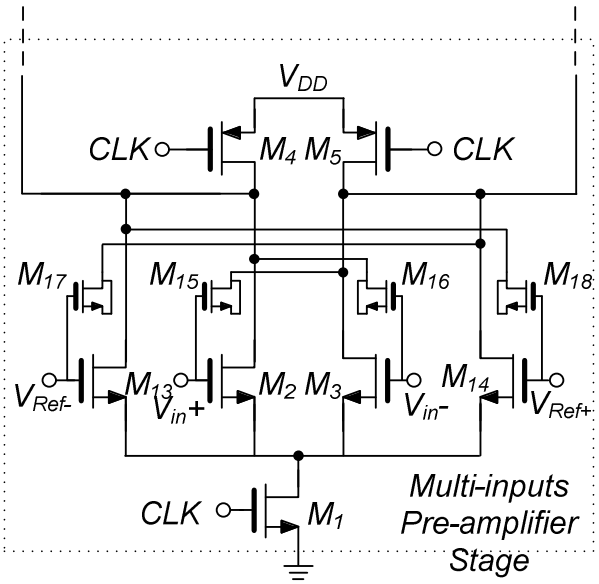

Fig. 3 Drain node stabilization technique using neutralization techniques for dual differential pairs input

The drain side fluctuation due to the gate-drain parasitic capacitances of the input differential pairs, *Cgd,i*, can be effectively suppressed by the isolation between the latch and preamplifier stages, cascode structure, and neutralization technique. In the double-tail voltage sense amplifier structure, the intermediate transistors M_6 and M_7 play an important role by isolating the pre-amplifier stage from the dynamic latch-type stage. Moreover, the neutralization technique is applied to further suppress the node voltage fluctuation in each drain sides of the input differential pairs, as shown in Fig. 3. The capacitors are formed by the source-drain tied MOS transistors, $M_{15\text{-}18}$. When they are operated in the strong inversion mode, its equivalent capacitance can be given by

$$C_{MOS},i = C_{OX}WiLi, \quad (2)$$

where C_{MOS} denotes the equivalent capacitance. When the drain side node voltage of the input transistor changes; the preceding stage should provide necessary charge through the gate-drain capacitance. With the help of the cross-coupled MOS capacitors in Fig. 3, the charge transfer from the preceding stage is suppressed [10], [11]. It is noted that the cascode devices are not applied in Fig. 3 because it is not suitable for the low power supply applications.

B. Common Source Node Stabilization Technique

The input referred disturbance at the input nodes is alleviated by suppressing the voltage fluctuation at the common source node of the input differential pair. One remedy is to place an external capacitor C_{ex} to the ground, as shown in Fig. 4. This method is very simple. However, it can seriously slow down the decision speed. The proposed method is to intentionally control the voltage level at the common source node so that the voltage fluctuation is suppressed. In order to do that, an added biasing circuit is inserted, as shown in Fig. 4. The added biasing circuit prevents the common source node of the differential pair from dropping to the ground even when the CLK goes high. Therefore, the voltage fluctuation is suppressed and the amount of input referred disturbance is reduced.

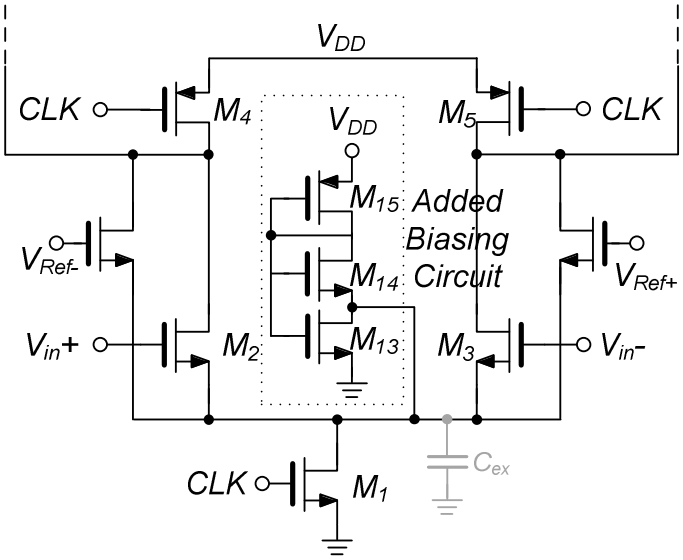

Fig. 4 Common source node stabilization technique using an added biasing circuit in the pre-amplifier stage

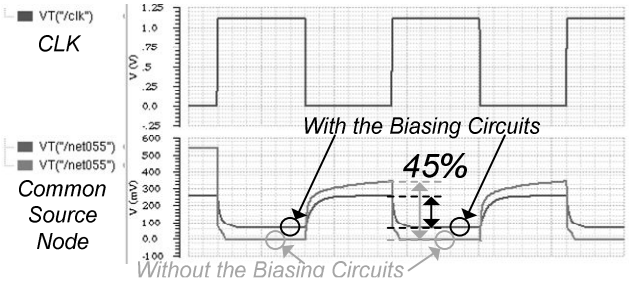

Fig. 5 The effect of the proposed added biasing circuits on suppressing the voltage fluctuation in the common source node of the pre-amplifier stage

The effects of the proposed added biasing circuit on suppressing the voltage fluctuation in the common source node of the pre-amplifier stage is simulated and shown in Fig. 5. The voltage fluctuation with the added biasing circuit decreases by 45%, compared to the voltage fluctuation without the biasing circuit.

The effects of the proposed added biasing circuit on suppressing the input referred disturbance is simulated and shown in Fig. 6. The voltage fluctuation at the input nodes with the added biasing circuit decreases by 40%, compared to the voltage fluctuation without the biasing circuit. Note that the

resistance and capacitance at the input sides are modified to exaggerate the input referred disturbance in the simulations. Due to the added biasing circuit, the voltage level of the common source node at the pre-amplifier stage does not perfectly drop to ground during the decision phase. Nevertheless, the static current path still does not exist in Fig. 6 during the decision phase because the current source transistor M_1 stay in the deep sub-threshold operation.

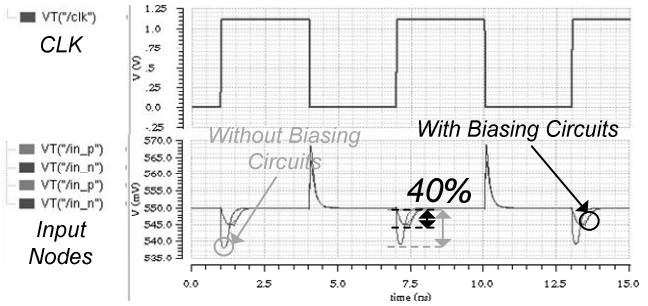

Fig. 6 The effect of the proposed added biasing circuits on suppressing the input referred disturbance in the pre-amplifier stage

TABLE I
RELATIONSHIP BETWEEN VOLTAGE RATIO AND SIZE RATIO

Voltage Ratio, $\left(\frac{V_{OV}}{V_{Target}}\right)$	Size Ratio, $\frac{(W/L)_{13}}{(W/L)_{14}}$
1/2	1/8
1	1/3
2	4/5
4	16/9

C. Design of the Biasing Circuits

An added biasing circuit in Fig. 4 can basically be an arbitrary circuit that can generate the certain voltage level. A current mirror structure is very simple to satisfy the design goal. However, it is very difficult to get the precise controllability as well as an arbitrary voltage level without additional branch which adds more power consumption. The *sooch* cascode current mirror is adopted in Fig. 4 [12], [13]. In this structure, the voltage level can be easily controlled by the transistor size ratio between M_{13} and M_{14}. Since M_{14} always makes M_{13} operate in the triode region, their size ratio m is defined by

$$m = \frac{\left(\frac{W}{L}\right)_{13}}{\left(\frac{W}{L}\right)_{14}} = \frac{\left(\frac{V_{OV}}{V_{Taget}}\right)^2}{2\left(\frac{V_{OV}}{V_{Taget}}\right)+1}, \quad (3)$$

where W, L, and V_{OV} denote the width, length and overdrive voltage of a given transistor. The desired voltage level is denoted by V_{Target} in (1). The relationship between m and the voltage ratio V_{OV}/V_{Target} is illustrated in Table I.

IV. CONCLUSIONS

The input referred disturbance problems of the multi-inputs voltage sense amplifiers are discussed. Due to the parasitic coupling capacitances between the preamplifier and latch stages, the voltage fluctuation of the internal nodes generates abrupt charge transfer to the input sides and result in the form of unwanted disturbance. The presented isolation between input and output nodes, cross-coupled capacitors at the input differential pairs, and added biasing circuits are effective to stabilize the internal node to suppress the voltage fluctuation. The 45% and 40% of improvements for the voltage stabilization at the common source node and the input referred disturbance are verified in simulations.

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