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Design and Implementation of a 10-bit SAR ADC with A Programmable Reference

Hasmayadi Abdul Majid, Yuzman Yusoff, Noor Shelida Salleh

***Abstract*—**This paper presents the development of a single-ended 38.5 kS/s 10-bit programmable reference SAR ADC which is realized in MIMOS's 0.35 µm CMOS process. The design uses a resistive DAC, a dynamic comparator with pre-amplifier and a SAR digital logic to create 10 effective bits ADC. A programmable reference circuitry allows the ADC to operate with different input range from 0.6 V to 2.1 V. The ADC consumed less than 7.5 mW power with a 3 V supply.

***Keywords*—**Successive Approximation Register Analog-to-Digital Converter, SAR ADC, Resistive DAC, Programmable Reference.

I. Introduction

ARCHITETURE sophistication of System-on-Chip (SOC) leads to an increasing need for low power analog-to-digital converter (ADC). Successive Approximation Register (SAR) ADCs are preferable than pipelined and sub-range ADCs due to low power consumption, high resolution, high accuracy and smaller die area [1]-[7]. Because of these benefits and a good tradeoff between resolution and speed, SAR ADCs are often be integrated with other functional blocks.

In a system where different types of sensors are integrated, converting analog signals to digital signals is a big challenge. This is due to difference sensors have different input range and resolution. The ADC used in the system must be able to cover all sensors input range.

In this paper, a single-ended 10-bit SAR ADC with programmable reference voltage is proposed and implemented using MIMOS' 0.35 µm CMOS process. Result shows that this proposed ADC could cover the wide input range while maintaining its performance.

II. Design of the SAR ADC

A. Architecture

The 10-bit SAR ADC consists of a programmable reference circuitry, a comparator, a digital-to-analog converter (DAC) and a SAR logic module as shown in Fig. 1. The design focuses on meeting the requirement of 10 bit accuracy for a reference voltage span of 0.5 V, 1 V, 1.5 V and 2 V.

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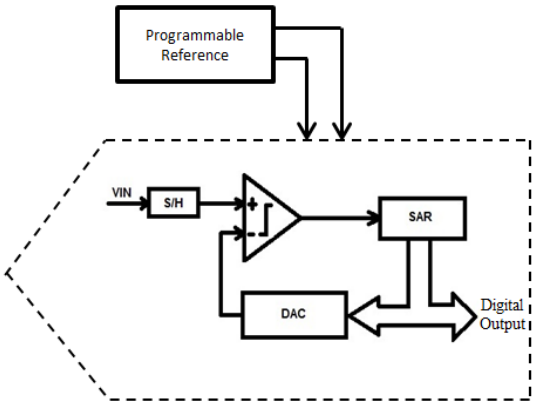

Fig. 1 SAR ADC architecture

B. Programmable Reference Generator

The programmable reference generator circuitry receives signal from bandgap circuitry and generates several desired reference voltages. The block diagram for designed reference generator is shown in Fig. 2. It receives input signal from either internal or external bandgap. The generated output voltage from bandgap is around 1.24V. The reference generator circuit has two input port; EXT_VBG and INT_VBG. Port EXT_VBG is the input from external reference while port INT_VBG is the input from internal designed bandgap. Port VREF_SEL is to select internal or external to be used.

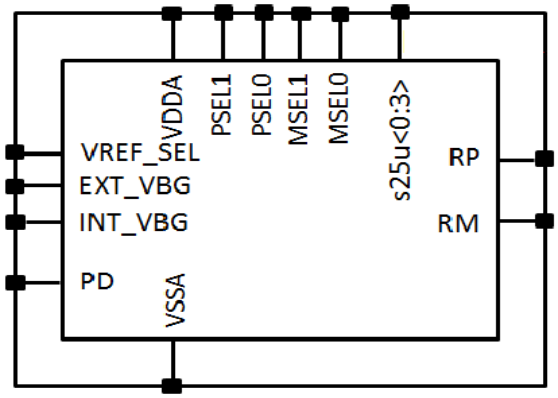

Fig. 2 Reference Generator

This block generates output voltage of 2.1V, 1.6V, 1.1V, 0.6V and 0.1V. It has two output port; RP and RM. RP voltage of 2.1V, 1.6V, 1.1V and 0.6V is selectable through PSEL0 & PSEL1 ports. On the other hand, the RM voltage of 1.6V, 1.1V, 0.6V and 0.1V is selectable through MSEL0 and MSEL1 ports. This block has Power Down (PD) option which

is used to power-off the circuitry when it is needed.

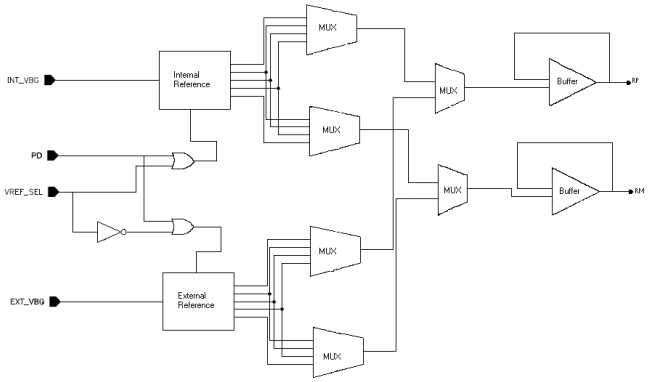

Fig. 3 Reference Generator Schematic

Fig. 3 shows that the circuitry has two sets of voltage reference generator. One of them is to generate reference voltage from internal (on the chip) bandgap voltage and the other is to generate reference voltage from the external (off the chip) bandgap voltage. Two voltage generator circuits are used due to different bandgap voltage produced by the internal bandgap and external bandgap. Output voltages from the generator go into analog mux. The analog mux select reference voltage based on the chosen selector switches (PSEL0, PSEL1, MSEL0 and MSEL1). The selector table is shown in Tables I and II. In order to minimize power consumption, only one voltage generator circuit is active at a time. If internal voltage reference is selected, the external voltage generator circuit is shut down and vice versa.

TABLE I
RP SELECTION TABLE

PSEL0	PSEL1	RP
0	0	0.6 V
0	1	1.1 V
1	0	1.6 V
1	1	2.1 V (default)

TABLE II
RM SELECTION TABLE

MSEL0	PSEL1	RM
0	0	0.1 V (default)
0	1	0.6 V
1	0	1.1 V
1	1	1.6 V (default)

Voltage generator circuitry is shown in Fig. 4. Input voltage comes from the internal/external bandgap and the voltage is amplified to 2.1 V, and divided into 1.6 V, 1.1 V, 0.6 V and 0.1 V. Proper values for resistors were chosen so that minimum amount of current is used.

Opamps used in this design are rail-to-rail folded cascade gain stage with class AB output stage. Each opamp has differential input ports and a single output port. Fig. 5 shows the circuit schematic of the opamp.

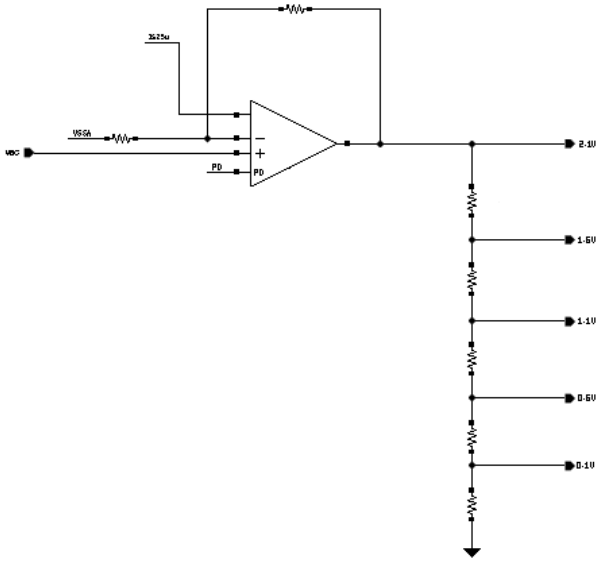

Fig. 4 Voltage Generator Circuitry

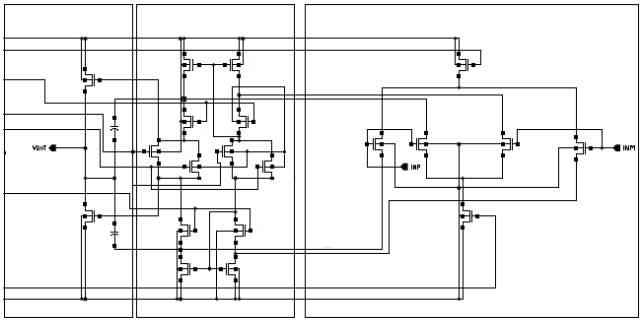

Fig. 5 Opamp Schematic

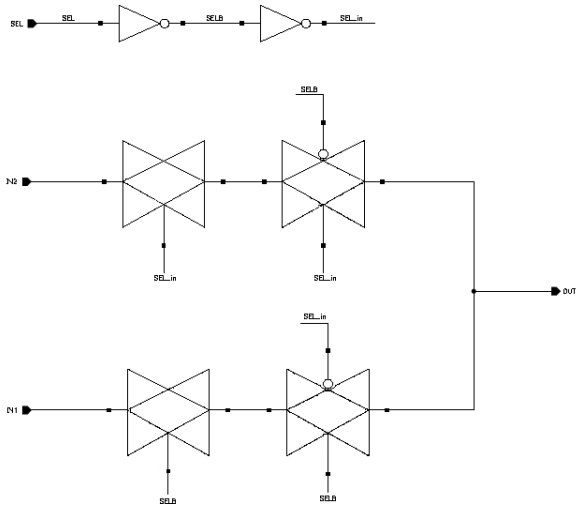

Fig. 6 2-to-1 Analog mux

Analog mux consists of a set of switches that select which input to be used. Combinations of selected pins determine which input to be relayed to the output port. Fig. 6 shows the circuit schematic of 2-to-1 analog mux. Each input line has a pair of switches. The first switch consists of a transmission gate with its output shorted to ground when the switch is off.

The second switch is a normal transmission gate where the ON and OFF are controlled by the selector pin. The same connection was implemented to the other analog mux.

C. Comparator

Comparator used in a SAR ADC must be accurate to half of the Least Significant Bit (LSB) value. For this 10-bit ADC with a minimum reference voltage of 0.5V, the LSB value is about 488 μV. Therefore, the comparator must be able to sense 244 μV differential input voltages. The comparator should produce output logic HIGH when differential input voltage equals or greater than 244 μV and output logic LOW when it is less than 244 μV.

The designed comparator comprises of a pre-amplifier and a latch. Since the latch could only sense input difference of few hundred millivolts, an amplifier is needed. A set of set of pre-amplifier is used to amplify the input signal from hundreds of microvolts to hundreds of millivolts. A comparator consists of a sample and hold (S/H) circuit, a comparator and a latch as shown in Fig. 7.

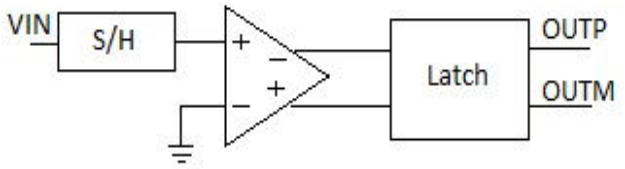

Fig. 7 Sample and Hold, pre-amplifier and latch

In this design, three single stage pre-amplifiers were used to boost the input voltage. This method relaxes the performance required by the latch. Hence, a latch design with minimum-sized devices could be used.

The pre-amplifier circuit implements a single stage fully differential architecture with a common mode feedback as shown in Figs. 8 and 9.

The LSB input voltage is very low and could be affected by the pre amplifier input and output noise. A noise cancelation technique known as "auto-zero" is used for the pre amplifiers. Fig. 10 shows the arrangement of these pre-amplifiers.

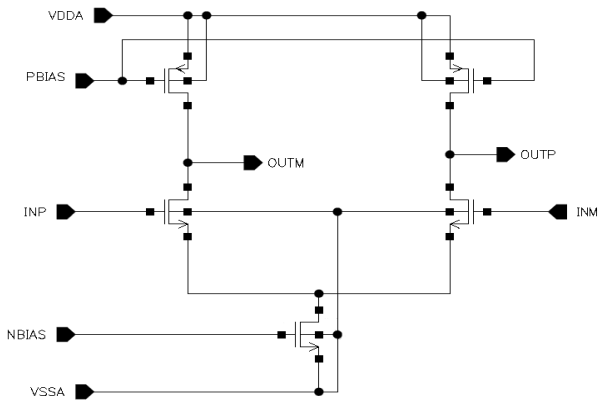

Fig. 8 Single-stage fully differential amplifier

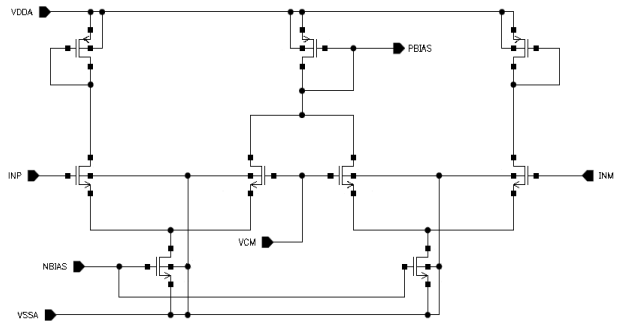

Fig. 9 Common mode feedback circuit

During sampling period, all switches are closed and all input and output ports will have same potential, hence removing the input and output offset voltage. For this design, during "auto-zero" all pre-amplifier port are set to a common mode voltage which is half of power supply.

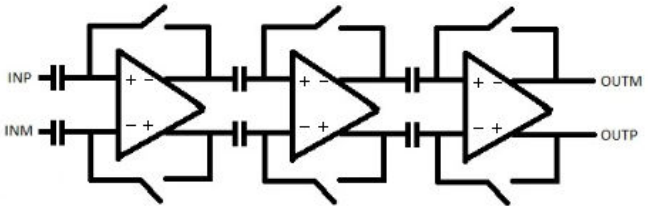

Fig. 10 Pre-amplifiers with a noise cancelation circuit

A dynamic latch with a reset was used. Input voltages for the two input terminals are reset to supply voltage when the clock is logic LOW. The advantage of using this circuitry compared to the regenerative dynamic latch is there is no extra clock state needed. This circuitry used the same clock signal as the SAR logic. Fig. 11 shows the circuit schematic of the latch.

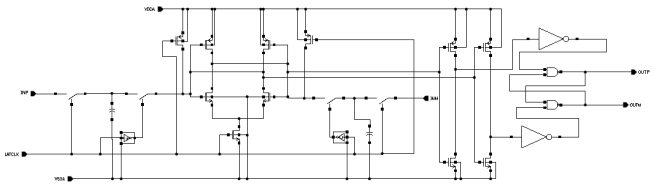

Fig. 11 Dynamic latch

D.DAC

A resistor ladder architecture; one of resistive DAC architecture available was selected. Fig. 12 shows the DAC circuit implemented in this work. This architecture is preferred due to its good linearity compared to capacitive DAC architecture.

E. SAR LOGIC

The SAR logic provides digital codes to the DAC based on the comparator output. It was designed to perform a binary search algorithm and produce ADC digital output at the end of the operation. It also produces the End of Conversion (EOC) signal when the conversion is completed and the digital outputs are valid.

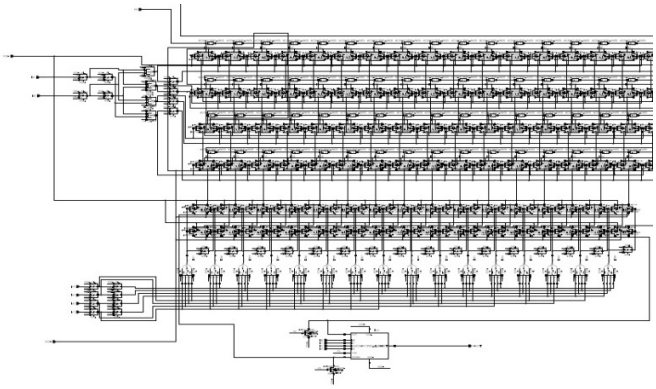

Fig. 12 DAC schematic

The SAR logic applied 13 clock cycles for conversion as shown in Fig. 13. The first 2 clock cycles are used for offset cancelation and S/H while another 10 clock cycles were used for conversion. The 13th clock cycle was used to generate the EOC signal and output parallel digital data.

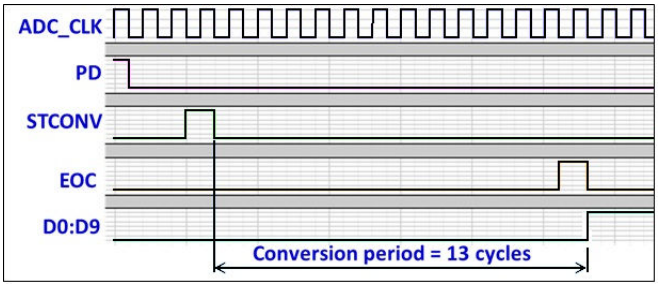

Fig. 13 SAR logic timing diagram for one conversion cycle

III. Result

A 10-bit SAR ADC was designed and simulated using MIMOS' 0.35µm technology. Fig. 14 shows the layout implementation of this ADC. At the top design is the ADC while at the bottom is the programmable reference generator and bandgap circuitry.

Table III summarizes the simulation result for the programmable voltage reference generator. It shows that there are discrepancies between the expected and simulated result. Simulated result shows generated voltages are higher than the expected output voltage by 5 mV to 8 mV. This introduces a dc offset for the DAC as well as the designed ADC. However, the DNL characteristic is not affected since the discrepancies are very small. This small dc offset is coming from the applied opamp.

TABLE III
Summary for Voltage Reference Generator

	2.1 V	1.6 V	1.1 V	0.6 V	0.1 V
Minimum	2.107 V	1.606 V	1.106 V	0.605 V	0.105 V
Average	2.108 V	1.607 V	1.106 V	0.606 V	0.105 V
Maximum	2.108 V	1.608 V	1.107 V	0.607 V	0.106 V

A simulation result for comparator is shown in Fig. 15. It is able to detect a very big positive, small negative, big negative and small positive voltage differences across all conditions (process, voltage, temperature).

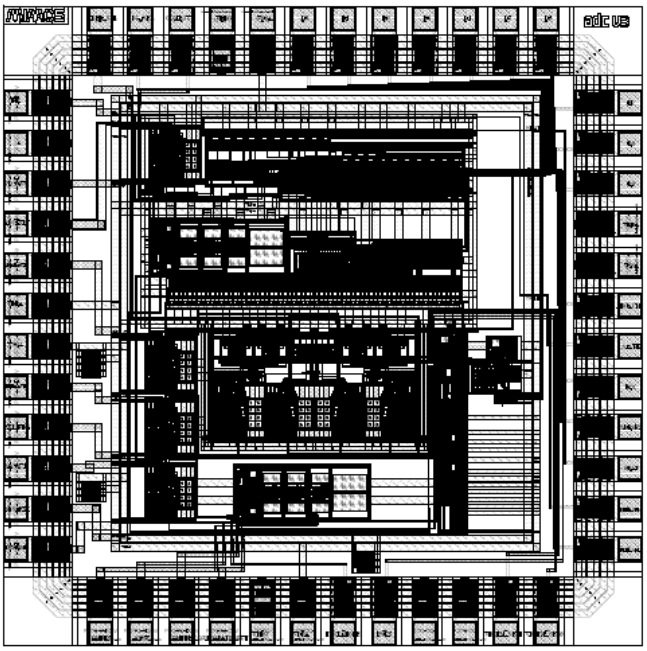

Fig. 14 ADC layout implementation

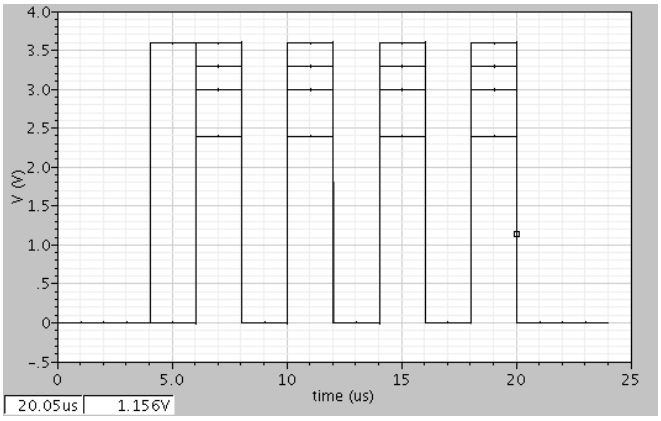

Fig. 15 Comparator result

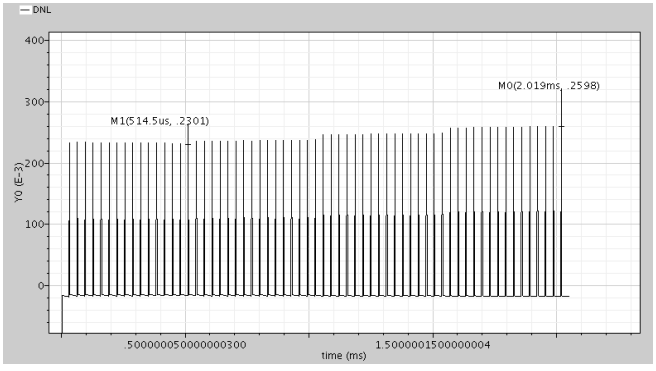

Fig. 16 Simulated DNL

The simulated DNL for the DAC is shown in Fig. 16. It has

good linearity with maximum DNL of 0.2598 LSB, which is within ± 0.5 LSB specification.

Top level simulation shows that SAR ADC is able to convert analog signal with minimum 488 µV voltage difference. Fig. 17 shows that the DAC value converged to the input value. The DAC value also shows that the SAR logic is correctly implementing binary search algorithm. Simulation by increasing the input voltage 1 LSB every conversion cycles also shows that the ADC is able to do the conversion without having a missing code. A part of this simulation is recorded and shown in Fig. 18.

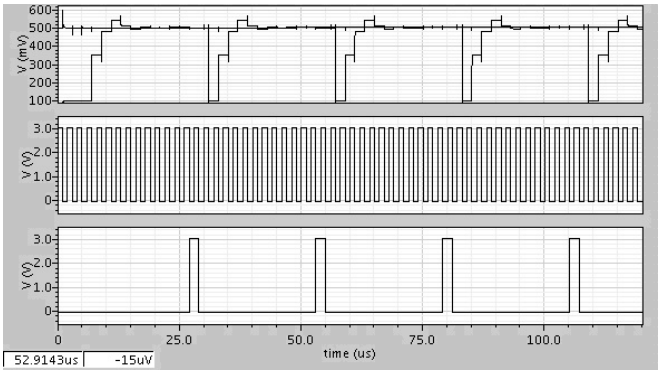

Fig. 17 DAC simulation

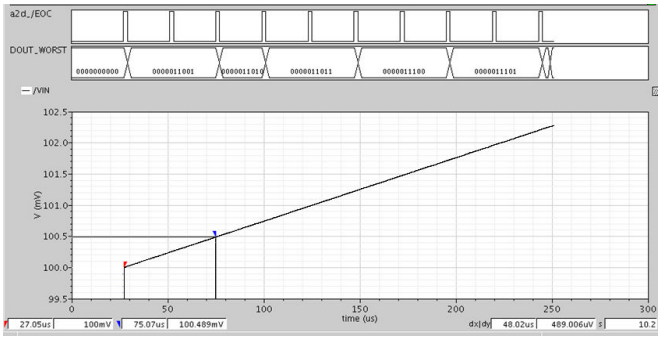

Fig. 18 Top level simulation

IV. Conclusion

A single ended 38.5 kS/s 10-bit programmable reference SAR ADC was proposed and implemented using ~~a~~ 0.35 µm CMOS technology. The designed ADC consumes of 2.5mm x 2.5mm chip size area. The total power dissipation is 7.2 mW with 3 V supply operation. The ADC produces 10-bit performance for reference of 2 V, 1.5 V, 1 V and 0.5 V. The ADC has option to become idle when it is not needed. In future, the comparator should be improved to achieve lower power consumption.

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