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Transient Analysis & Performance Estimation of Gate Inside Junctionless Transistor (GI-JLT)

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Abstract—In this paper, the transient device performance analysis of n-type Gate Inside JunctionLess Transistor (GI-JLT) has been evaluated. 3-D Bohm Quantum Potential (BQP) transport device simulation has been used to evaluate the delay and power dissipation performance. GI-JLT has a number of desirable device parameters such as reduced propagation delay, dynamic power dissipation, power and delay product, intrinsic gate delay and energy delay product as compared to Gate-all-around transistors GAA-JLT. In addition to this, various other device performance parameters namely, on/off current ratio, short channel effects (SCE), transconductance Generation Factor (TGF) and unity gain cut-off frequency (f_T) and subthreshold slope (SS) of the GI-JLT and GAA-JLT have been analyzed and compared. GI-JLT shows better device performance characteristics than GAA-JLT for low power and high frequency applications, because of its larger gate electrostatic control on the device operation.

Keywords—Gate-inside junctionless transistor GI-JLT, Gate-all-around junctionless transistor GAA-JLT, propagation delay, power delay product.

I. Introduction

METAL-oxide-semiconductor field-effect transistors (MOSFETs) are shrinking rapidly, as per the international technology roadmap of semiconductors (ITRS) and will reach to sub-10 nm regime in the few years. As a result of this scaling down, short-channel MOSFETs of below 22 nm are having various serious challenges such as higher leakage currents and short-channel effects (SCEs) due to the decreasing gate controllability over the channel. Since the device dimensions are scaled to the nanometer scale range, the influence of SCE on device performance characteristics for conventional MOSFETs are very pronounced. So, in order to overcome these issues new class of field effects devices are sorely needed. Hence, JunctionLess field-effect transistors (JL-FET) represent a new class of field effects devices having no abrupt doping junctions are coined based on Lilienfeld's innovation [1]. It has been recently revisited by J. P. Colinge and coworkers [2], [3] for its properties and design guidelines related issues [4]. The basic structure of a JL-FET consists of a uniformly highly doped silicon channel controlled by gate electrode. Unlike conventional MOSFETs, in these devices, both the source and the drain have the same type of doping as the channel, i.e., there is no pn junction. These devices are potential candidate for next generation high speed and low power integrated circuits because of its excellent short channel effect (SCE), near ideal subthreshold swing (SS), low leakage current and good carrier transport efficiency. The device structure based advantages of JL devices are simple structure with no ultrashallow p-n junction at interface of channel and source/drain region which greatly simplifies the process flow and reduce cost of device fabrication. In JLT current transport is in the bulk of the semiconductor, which reduces the impact of imperfect semiconductor/insulator interfaces. In literature various device structural variants of JLT have been reported such as Junctionless multiple-gate transistors [5] and [6], low sub-threshold swing multigate JLT [7], and the bulk planar junctionless transistor (BP-JLT) [8]. In recent research gate-all-around (GAA) architecture [9] is reported for fabricating JL devices as the gate creates a depletion region at all sides of the device to turn off the device. These structural variants of the JLT are designed to enhance the gate electrostatic control over the channel region. Hence, to enhance the gate controllability further, Gate Inside Junctionless Transistor (GIJLT) [10] and [11] has been reported as a novel device structure for use in high speed and low power electronic devices owing to their excellent short channel effect, ideal subthreshold swing, excellent gate controllability, low leakage current and good carrier transport efficiency. GI-JLT is gated resistor with no p-n junction between source/drain and channel, also it has no overlap/underlap issue between source/drain and gate. It is is volume depleted by gate to turn off the device for zero gate bias due to the effective work function difference between semiconductor and gate electrode. To achieve the 'ON' state a gate voltage is applied that brings device in flat band region. This paper, present the evaluation of the transient performance of n-type GI-JLT using ac analysis along with 3-D Bohm Quantum Potential (BQP) transport device simulation to evaluate its delay and power dissipation performance. In order to estimate the transient performance, analysis of various transient characteristics such as propagation delay, dynamic power loss, power and delay product, intrinsic gate delay and energy delay product of the GI-JLT and GAA-JLT. This paper is structured as follows. In Section II, the simulation method and the setting of the parameters for studying the device characteristics and circuits level behavior are introduced, Section III the circuit performance of GI-JLT and GAA-JLT are compared. Finally, Section IV concludes the transient analysis.

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II. Device Structure and Simulation

Fig. 1 shows device structure for n-channel GIJLT. Cross section area of gate electrode (p^+ poly-silicon) is 7 nm $\times$ 7 nm and is surrounded by the gate dielectric (AlN) of

thickness 1 nm. Silicon layer of 2nm is surrounded over gate dielectric. Device layer Doping N_d is of uniform profile having the value $3.5 \times 10^{19} cm^{-3}$ and the work-function of gate is 5.1 eV. Aluminum electrodes are used as source/drain contact on top of silicon layer. Fig. 2 shows the device structure for the n-channel GAA-JLT of channel length of 20 nm, which is simulated for transient performance comparison with identical doping profile, cross section of silicon layer is 7 nm×7 nm and gate workfunction of 4.9 eV. Transient characteristics are investigated using mixed mode TCAD simulator 3-D ATLAS version 2.10.18.R. To obtain accurate numerical results for a nanometer-scale device, the device is simulated by solving 3-D BQP transport model [12], [13] and [14]. Bandgap narrowing model (BGN), the band-to-band tunneling model, and Auger and Shockley-Read-Hall both recombination models are used to account for the leakage current. In addition to this, the doping-dependent model are also considered. The direct tunneling model is not utilized because high-k /metal-gate technology is used. For a fair comparison, threshold voltages (V_{th}) are adjusted to about 0.33V by tuning the gate work-function by doping p^+ polysilicon.

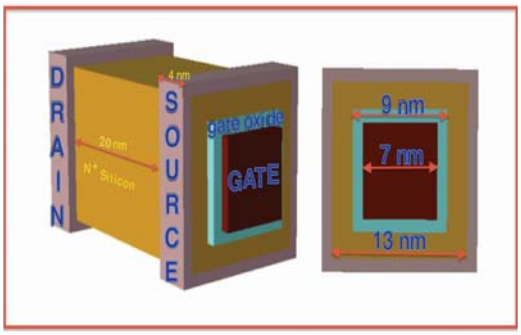

Fig. 1. Proposed n-type GI-JLT

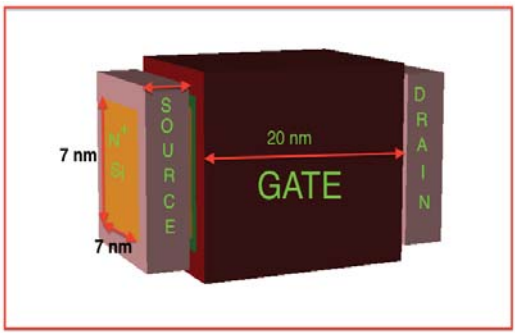

Fig. 2. Device structure of n-type GAA-JLT

III. SIMULATION RESULTS AND DISCUSSION

For better comparision the transient performance parameters of both GI-JLT and GAA-JLT are evaluated and compared in depth in this section.Even though conventional MOSFET parameters and its physics based understanding is not one to one correlated with the device parameters of JLT but its

TABLE I
PARAMETERS USED DURING THE N-TYPE DEVICE SIMULATIONS

Parameters	GI-JLT	GAA-JLT
Channel length (L_g)	$20nm$	$20nm$
Device layer Doping N_d	$3.5 \times 10^{19} cm^{-3}$	$3.5 \times 10^{19} cm^{-3}$
Gate Workfunction	$5.1eV$	$4.9eV$
Gate bias	$0.0V$ to $0.9V$	$0.0V$ to $0.9V$
Drain bias	$0.04V$ & $0.9V$	$0.04V$& $0.9V$

definition and graphical extraction are similar. These extracted parameters are the indicative of the potentials of these devices. Fig. 3,4 shows the plot of Drain Current for n-channel GI-JLT and GAA-JLT as a function of the drain-to-source voltage and gate-to-source voltage for drain voltage of V_{ds} = $0.9V$ and V_{ds} = $0.04V$.

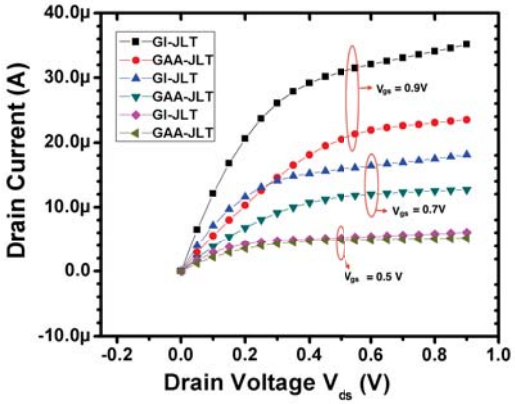

Fig. 3. Drain Current for n-channel GI-JLT and GAA-JLT as a function of the drain-to-source voltage.

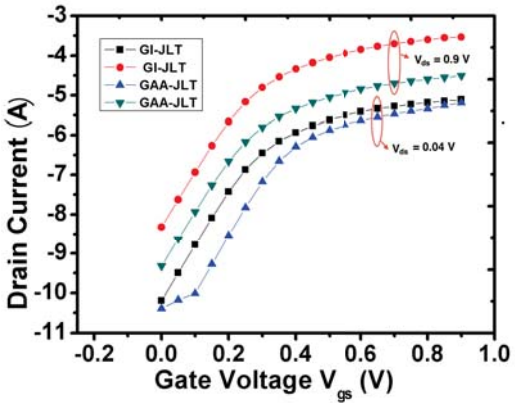

Fig. 4. Drain Current for n-channel GI-JLT and GAA-JLT as a function of the gate-to-source voltage for drain voltage of V_{ds} = $0.9V$ and V_{ds} = $0.04V$

As the transient behavior of the device is because of the various parasitic capacitances involved in the device structure. Hence, to evaluate the the transient behavior study of the parasitic capacitances in the device is sorely required. Fig. 5 explores the plot for gate-to-source capacitance C_{gs}

and gate-to-drain capacitance C_{gd} for n-channel GI-JLT and GAA-JLT as a function of the gate-to-source voltage for drain voltage of V_{ds} = $0.9V$. It shows value of gate-to-source capacitance C_{gs} as 13.9 aF for GI-JLT and 12.0 aF for GAA-JLT and gate-to-drain capacitance C_{gd} as 7.2aF for GI-JLT and 2.5 aF for GAA-JLT. As, the specific gate capacitance should be as large as possible in order to obtain a very strong electrostatic field-effect modulation for I_d. The parasitic gate capacitance C_{gg} for JLT is a vital parameter as it effects the delay significantly [15]. The parasitic gate capacitance C_{gg} in a JLT is also derived in a similar manner as in the conventional inversion mode device, i.e, oxide capacitance in series with the silicon capacitance (C_{Si}). Hence, minimum gate capacitance $C_{gg,min}$ is defined as

$$C_{gg,min} = \frac{C_{ox} \times C_{Si,min}}{C_{ox} + C_{Si,min}} \tag{1}$$

where, $C_{Si,min}$ is given by the relation

$$C_{Si,min} = \frac{\epsilon_{Si}}{d_{max}} \tag{2}$$

where, d_{max} is the maximum depletion region depth. As when JLT is turned of it goes into fully depleted state, and device dimensions remains constant for a device, hence, the minimum gate capacitance is a constant for a device with given dimensions. Various parasitic gate capacitances are tabulated in Table II.

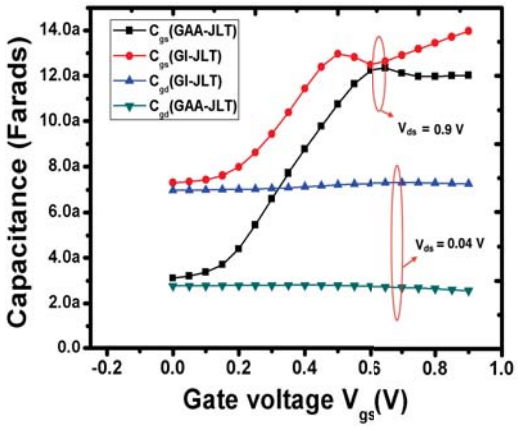

Fig. 5. Gate-to-source and gate-to-drain capacitance for n-channel GI-JLT and GAA-JLT as a function of the gate-to-source voltage for drain voltage of V_{ds} = $0.9V$.

TABLE II
PARASITIC CAPACITANCES OF N-TYPE GIJLT AND GAA-JLT AT V_{gs}=V_{ds}=0.9 V.

Parameters	GI-JLT	GAA-JLT
C_{gs} in (aF)	13.9	12.0
C_{gd} in (aF)	7.2	2.5
C_{gg} in (aF)	21.2	15.1

Intrinsic gate delay [16] is important as it represents the frequency limit of the transistor operation. The intrinsic gate delay in JLTs are because of its parasitic gate capacitance C_{gg}, it is defined as

$$\tau_{int} = \frac{C_{gg} \times V_{dd}}{I_d} \tag{3}$$

where, τ_{int} is the intrinsic gate delay. Fig. 6 shows the plot for the intrinsic gate delay as a function of drain-to-source voltage V_{ds} for GI-JLT and GAA-JLT, it shows that delay for GI-JLT is less than GAA-JLT for lower V_{ds} values as the on-current is higher for this drain-to-source voltage range. But as V_{ds} keeps on increasing on current get saturated and C_{gg} also acquires its maximum value of accumulation mode at flat band voltage V_{FB}, hence the intrinsic delay increases a bit. Hence, GI-JLT is showing better intrinsic delay performance for low power applications. In addition to this, dynamic power dissipation is also an important parameter for transient analysis of the device. Dynamic power dissipation defined as

$$P_{dyn} = \frac{C_{gg} \times V_{dd}^2}{f} \tag{4}$$

where, f is the operating frequency and P_{dyn} is dynamic power dissipation, it is plotted as a function of drain-to-source voltage for GI-JLT and GAA-JLT in Fig. 7. It is comparable for GI-JLT at lower V_{ds} values. Another important parameter for transient analysis is power delay product, it has been plotted as a function of drain-to-source voltage for GI-JLT and GAA-JLT in Fig. 8, it enhances significantly for GI-JLT as compared with GAA-JLT. Similarly, energy delay product $(C_{gg} \times V_{dd}^2)$ for both GL-Jlt and GI-JLT are plotted as a function of drain-to-source voltage in Fig. 9. It is to be noted that the unit of power is $Watt$ in place of $Watt/\mu m$ as the current I_d is in A not in $A/\mu m$ because **3-D** structure is used for simulation. As a result of this, unit of energy is taken as J-sec. Apart from this, output resistance R_o for both transistors as a function of V_{gs} has been plotted in Fig.10, it is comparable for both GI-JLT and GAA-JLT.

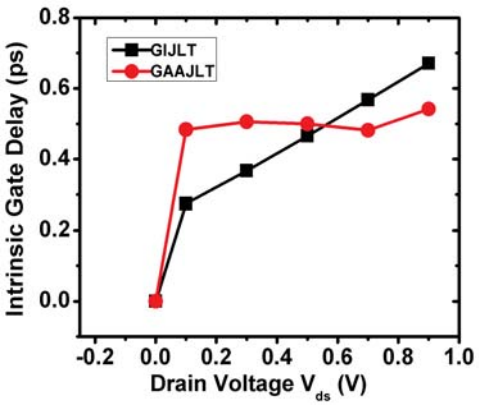

Fig. 6. Intrinsic gate delay as a function of drain-to-source voltage for both GI-JLT and GAA-JLT

For transient analysis unity gain cut-off frequency f_T is also an essential parameter to study and it is given by equation

$$f_T = \frac{g_m}{2\pi(C_{gg})} \tag{5}$$

Fig. 11 represents unity gain cut-off-frequency f_T for n-channel GI-JLT and GAA-JLT as a function of the

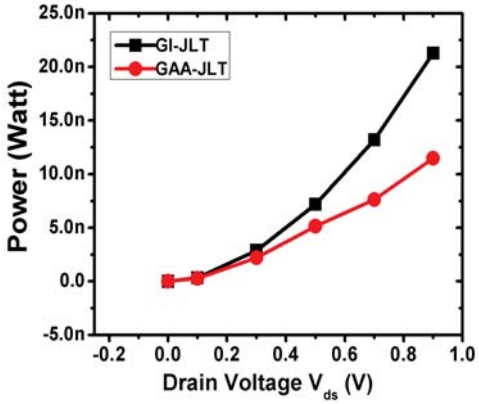

Fig. 7. Dynamic power dissipation as a function of drain-to-source voltage for GI-JLT and GAA-JLT

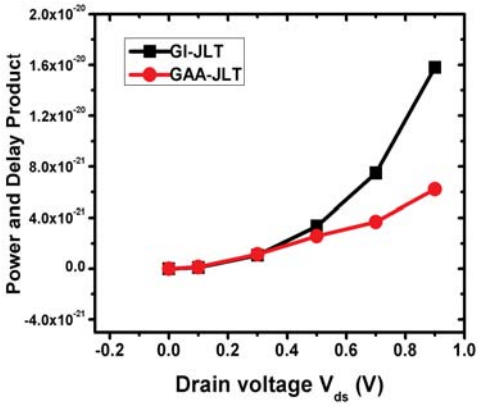

Fig. 8. Power delay product as a function of drain-to-source voltage for GI-JLT and GAA-JLT

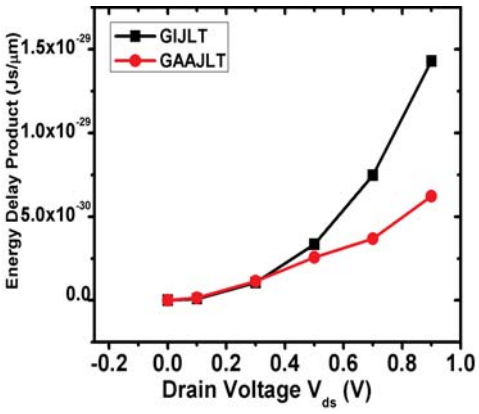

Fig. 9. Energy delay product as a function of drain-to-source voltage for GI-JLT and GAA-JLT

gate-to-source voltage for drain voltage of V_{ds} = 0.9V. GI-JLT has f_T as 380 GHz and GAA-JLT has f_T as 245 GHz. It improves by 35% for GI-JLT in comparision to GAA-JLT. As GI-JLT presents higher unity gain cut-off frequency that makes it suitable even for the high speed applications as compared to a GAA-JLT transistor. Fig. 12 shows the gain band-width product for n-channel GI-JLT and GAA-JLT as a function of the gate-to-source voltage for drain voltage

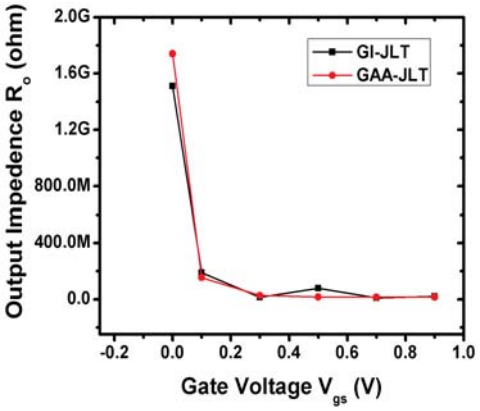

Fig. 10. Output resistance R_o for GI-JLT and GAA-JLT as a function of V_{gs}

of V_{ds} = 0.9V. As for high frequency transient analysis gain-band-width product (GBW) is one of the most defining device performance parameter, which is computed by the following approximate equation

$$GBW = \frac{g_m}{(2 * \pi * C_{gd})} \tag{6}$$

It is slightly lower for the GAA-JLT as compared with the GI-JLT. Hence, GI-JLT is better than GAA-JLT even for high frequency applications as well. Fig. 13 presents the transconductance (g_m) for n-channel GI-JLT and GAA-JLT as a function of the gate-to-source voltage for drain voltage of V_{ds} = 0.9V and V_{ds} = 0.04V. In addition to this, transconductance generation factor (TGF) defined as the ratio between transconductance and drain-to-source current is shown in Fig. 14 for n-channel GI-JLT and GAA-JLT as a function of the gate-to-source voltage for drain voltage of $V_{ds} = 0.9V$.

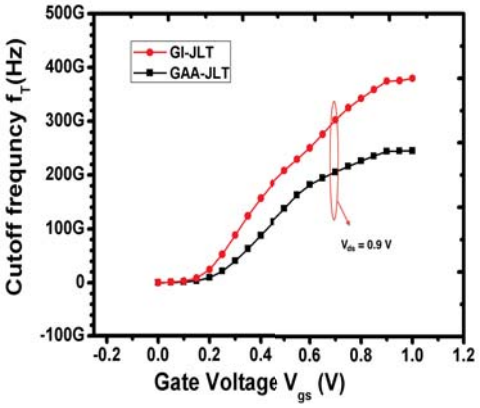

Fig. 11. Unity gain cut-off-frequency (f_T) for n-channel GI-JLT and GAA-JLT as a function of the gate-to-source voltage for drain voltage of V_{ds} = 0.9V.

IV. Conclusion

In this paper, the transient device performance analysis of n-type Gate Inside JunctionLess Transistor (GI-JLT) has been evaluated. 3-D Bohm Quantum Potential (BQP)

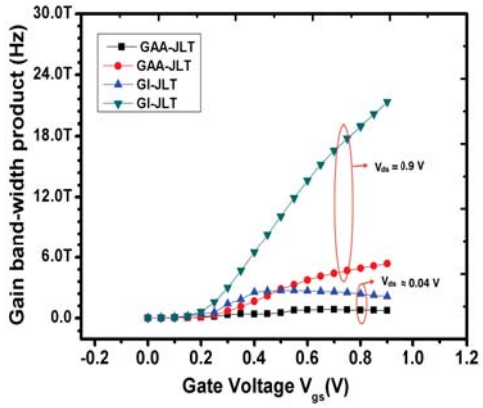

Fig. 12. Gain band-width product for n-channel GI-JLT and GAA-JLT as a function of the gate-to-source voltage for drain voltage of $V_{ds} = 0.9V$ and $V_{ds} = 40mV$.

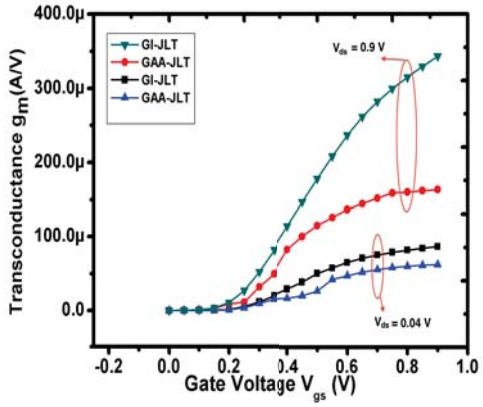

Fig. 13. Transconductance (g_m) for n-channel GI-JLT and GAA-JLT as a function of the gate-to-source voltage for drain voltage of $V_{ds} = 0.9V$ and V_{ds} = $0.04V$

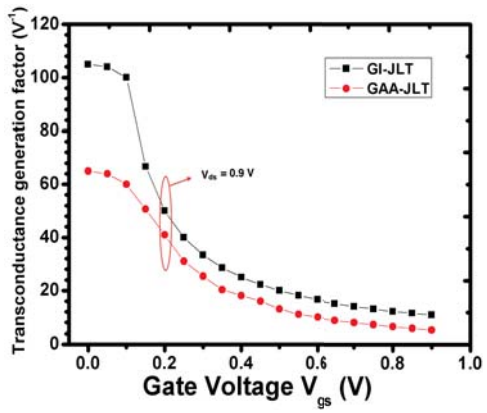

Fig. 14. TGF for n-channel GI-JLT and GAA-JLT as a function of the gate-to-source voltage for drain voltage of $V_{ds} = 0.9V$.

transport device simulation has been used to evaluate the delay and power dissipation performance. GI-JLT has a number of desirable device parameters such as reduced propagation delay, dynamic power dissipation, power and delay product, intrinsic gate delay and energy delay product over Gate-all-around transistors GAA-JLT. In addition to this, various other device performance parameters namely, on/off current ratio, short channel effects (SCE), transconductance Generation Factor (TGF) and unity gain cut-off frequency (f_T) and subthreshold slope (SS) are improved for G-JLT over GAA-JLT. GI-JLT shows better device performance characteristics than GAA-JLT for low power and high frequency applications, because of its larger gate electrostatic control on the device operation. Hence, GI-JLT is the potential candidate for future low power and high frequency applications.

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