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Design and Testing of Nanotechnology Based Sequential Circuits Using MX-CQCA Logic in VHDL

K. Maria Agnes, J. Joshua Bapu

***Abstract*—**This paper impart the design and testing of Nanotechnology based sequential circuits using multiplexer conservative QCA (MX-CQCA) logic gates, which is easily testable using only two vectors. This method has great prospective in the design of sequential circuits based on reversible conservative logic gates and also smashes the sequential circuits implemented in traditional gates in terms of testability. Reversible circuits are similar to usual logic circuits except that they are built from reversible gates. Designs of multiplexer conservative QCA logic based two vectors testable double edge triggered (DET) sequential circuits in VHDL language are also accessible here; it will also diminish intricacy in testing side. Also other types of sequential circuits such as D, SR, JK latches are designed using this MX-CQCA logic gate. The objective behind the proposed design methodologies is to amalgamate arithmetic and logic functional units optimizing key metrics such as garbage outputs, delay, area and power. The projected MX-CQCA gate outshines other reversible gates in terms of the intricacy, delay.

***Keywords*—**Conservative logic, Double edge triggered (DET) flip flop, majority voters, MX-CQCA gate, reversible logic, Quantum dot Cellular automata.

I. Introduction

THE current irreversible technologies will squander a lot of heat and will trim down the life of the circuit. To overcome this problem, the new reversible conservative logic was introduced in VLSI design. These reversible circuits are of high attention in low power CMOS design, Quantum logics. Quantum-dot Cellular Automata (QCA) is one of the narrative nanotechnologies that are being considered as a possible replacement for CMOS technology. QCA has been introduced to triumph over the limitation of CMOS technology.

In QCA, computing logic states of logic '1' and logic '0' are represented by the position of the electrons inside the QCA cell layout not by a voltage level as in the usual logic gate as illustrated in Fig. 1. Thus, when the bit is turn over from logic '1' to logic '0' there is no actual discharging of the capacitor as in unadventurous CMOS. Hence, QCA does not have to squander all its signal energy during conversion [1], [2]. For that reason, QCA has been freshly recognized as one of the most emerging technology with lot of potential application in future [3]-[9].

Further, proliferation of the polarization from one cell to neighboring cell is because of make contact with the electrons in neighboring QCA cells. As there is no progress of electrons from one QCA cell to the supplementary cell, there is no current surge. Thus, QCA has no dissipation in signal proliferation. Therefore, QCA has significant advantage compared to CMOS technology in terms of power dissipation.

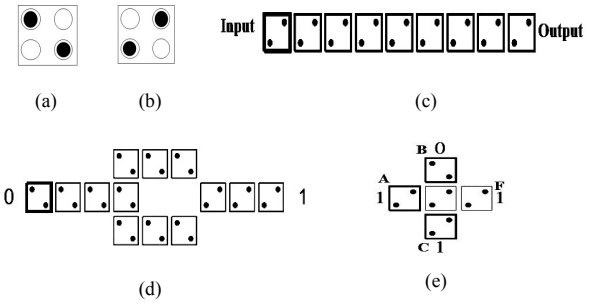


Fig. 1 QCA cell and basic QCA devices (a) QCA cell as logic '0' , (b) QCA cell as logic '1', (c) Binary, (d) wire inverter, (e) Majority Voter

In digital logic most of the functions are implemented using SOP, POS form. But in QCA logic these functions are simply implemented using majority gates [10] also in high speed pipelined architecture QCA computations are gladly well-matched. Partially reversible pipelined architecture is the amalgamations of region with Bennett clocking and memory storage come mutually for low power advantage of reversible computing and also provides high throughput. In this proposed expertise, computation phases are clocked by Bennett clocking and do not scatter power [11]. The concurrently testable reversible logic based sequential design is precise type of reversible circuits, which is based on parity preserving assets. Mostly used conservative reversible logic gate is fredkin gate [12]. This parity preserving property is useful for both eternal and ephemeral faults detection that results from the parity inequality between inputs and outputs [13]. For the purpose of testing, standard design must be rehabilitated into some other form. So that the reversible logic gates are rehabilitated into online testable form, but has some complicated steps. In this conversion procedure every reversible's gate G of the design is rehabilitated into deduced reversible gates DRG (G) without modifying its unique functionality. This conversion method needs not to be tainted for the purpose of adding testability feature to it. But area gets increased in this methodology [14].

Conservative logic is a logic family that exhibits the property that there are an equal number of 1s in the outputs as there are in the inputs. Conservative logic may be reversible in nature or may not be reversible in nature. Reversibility is the

K.Maria Agnes is with Electronics and Communication Department, Dr.Sivanthi Aditanar College of Engineering, Tiruchendur, India (e-mail: kennedyagnes.k@gmail.com).

J.Joshua Babu is a Distinguished Assistant Professor of Electronics and Communication engineering in Dr.Sivanthi Aditanar College of Engineering, Tiruchendur, India (e-mail: joshuababu@gmail.com).

belongings of circuits in which the gate/circuit that does not loose information. Conservative logic is called reversible conservative logic when there is a one-to-one mapping among the inputs and the outputs vectors together with the conservative property. Conservative logic circuits are not reversible, if one-to-one mapping between the inputs and the outputs vectors are not potted. This reversible conservative logic gate affords less power dissipation than conventional logic gates i.e. the power dissipation is less than ln2 KT [15].

The testing of the sequential circuits is even worse. The output of a sequential circuit depends, not only on the contemporary inputs, but also on the interior state of all the memory elements. Suppose we have 'm' interior memory elements; then we can have 2^m different interior states. To comprehensively test the circuit, we must afford each input to each one of the internal states for a total of 2^{n+m} different test vectors. For large circuits, we must take advantage of circuit structure to diminish the complicatedness of testing. With advert of VLSI technology, circuits are more prone to transient fault that can occur during its operation. In traditional method such as triple-modular redundancy (TMR), transient faults in the circuits are detected, but they consume large area and power. To overcome this negative aspect, reversible gates are used for the design. This reversible with conservative logic gate reduces the test vectors needed for testing and also trim down the area, delay.

II. Proposed Work

The MX-CQCA gate shown in Fig. 2 (a) can be described as a mapping (A, B, C) to [P = AB, Q = (A (~B) + BC), R=B+C] where A, B, C are the primary inputs of the MX-CQCA gate and P, Q, R are the primary outputs MX-CQCA gate, respectively. The MX-CQCA gate is conservative in nature, that is has the equivalent number of 1s in the outputs as in the inputs.

A. Design of Testable Reversible MX-CQCA Based Latches

The characteristic equation of the D latch can be written as $Q^+ = [D.E+ (\sim E).Q]$. Here the enable signal (E) pertains to the clock and is used interchangeably in place of clock. When the enable signal is 1, the value of the input D is reproduced at the output that is $Q^+ = D$. While, when E = 0 the latch maintains its previous state, that is $Q^+ = Q$. The MX-CQCA gate has one of its outputs working as 2:1 MUX, thus the characteristic equation of the D latch can be mapped to the MX-CQCA gate. Fig. 2 (b) shows the realization of the reversible D latch using the MX-CQCA gate. Moreover, the proposed work cannot be tested by two input vectors all 0s and all 1s because of feedback signal, as the output Q would latch 1 when the inputs are toggled from all 1s to all 0s and could be misapprehended as stuck-at-1 fault. In usual D-latch design cannot be used in testing side because fault detection is not possible in normal node. For this reason we propose another design that will cascade another two MX-CQCA gates to output Q shown in Fig. 3 (a).

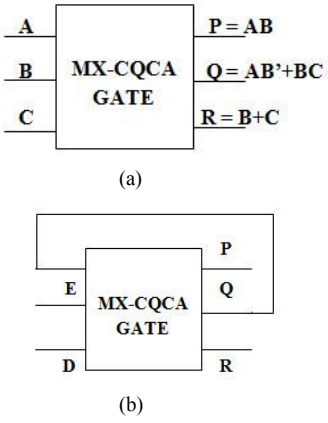


Fig. 2 (a) Block diagram of MX-CQCA gate, (b) Block diagram of MX-CQCA based D-Latch

The design has two control signals, C1 and C2. The proposed design can make for two modes: 1) Normal mode and 2) test mode.

1) Normal Mode: The normal mode is shown in Fig. 3 (b) which will have C1C2 = 01 and will have the design working as a D latch.
2) Test Mode (Disrupt the Feedback): In test mode, when C1C2 = 00 as shown in Fig. 3 (d) it will make the proposed work testable with all 0s input vectors as output T1 will be converted into 0 resulting in making it testable with all 0s input vectors. Thus, any stuck-at-1 fault can be discovered. When C1C2 = 11 as shown in Fig. 3 (c), the output T1 will be converted into 1 and the proposed design will be transformed into testable with all 1s input vectors for any stuck-at-0 fault. It can be come out from above that C1 and C2 will dislocate the feedback in test mode. Thus, our projected design works as a reversible D latch and the propose can be checked with only two test vectors, all 0s and all 1s, for any stuck-at fault by utilizing the inborn possessions of conservative reversible logic.

B. Design of Testable Master-Slave Flip-Flops Using MX-CQCA Logic

In the existing method, the master-slave move toward of using one latch as a master and the other latch as a slave is used to design the reversible flip-flop. In this projected work, we have purported the design of testable flip-flops using the master-slave strategy that can be tried out for any stuck-at faults using only two test vectors, all 0's and all 1's. Fig. 4 (a) shows the design of the master-slave D flip-flop in which we have used positive enable MX-CQCA gate-based testable D latch. This MX-CQCA gate based testable reversible D flip flops has four control signals mC1, mC2, sC1, and sC2. The signals mC1 and mC2 have power over the modes for the master latch, while sC1 and sC2 have power over the modes for the slave latch.

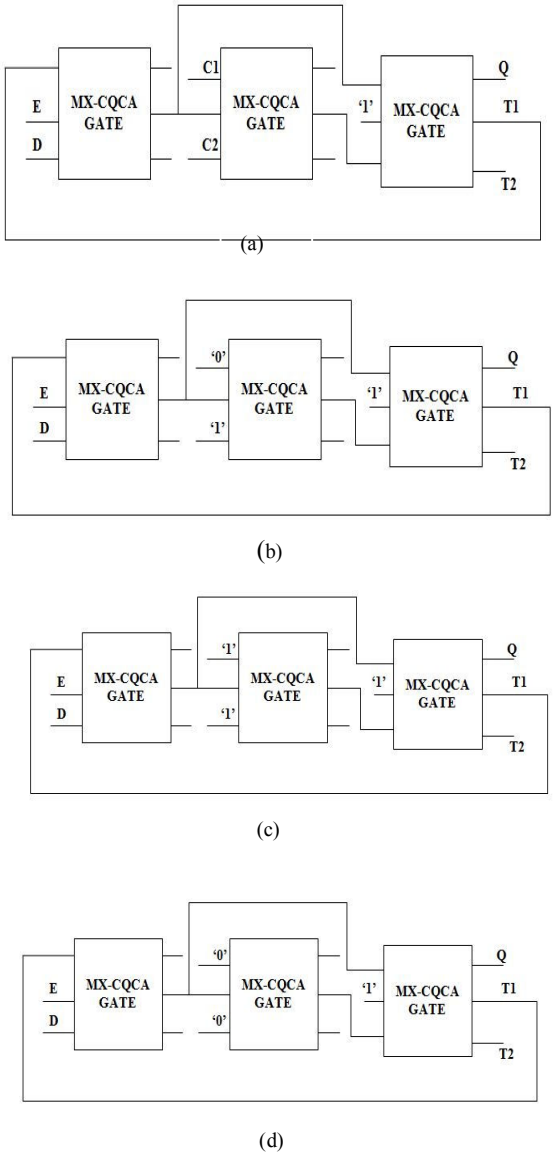
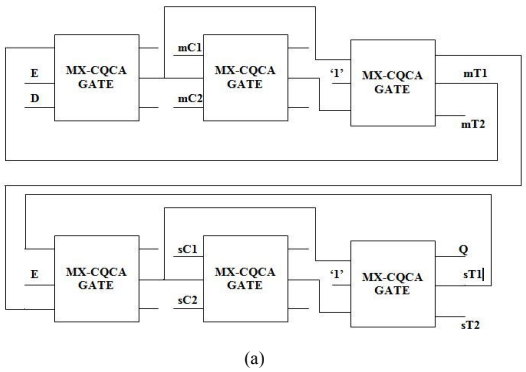


Fig. 3 Design of testable D latch using conservative MX-CQCA GATE (a) MX-CQCA based D-latch with control signal C1, C2, (b) MX-CQCA based D-latch in normal mode, (c) MX-CQCA based D-latch in test mode for stuck-at-0 fault,(d) MX-CQCA based D-latch in test mode for stuck-at- fault



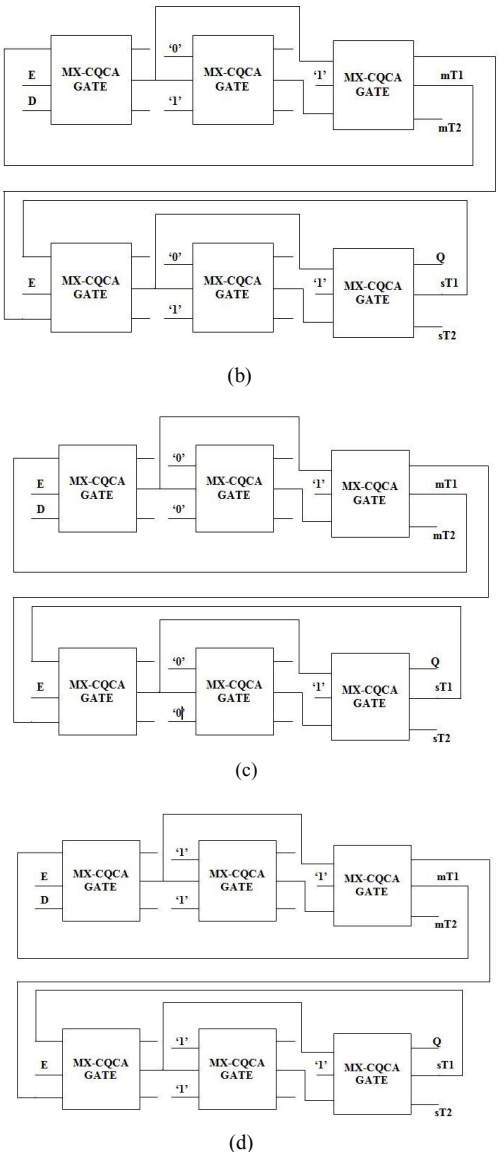


Fig. 4 Design of MX-CQCA gate based master-slave D flip-flop (a) master slave flip flop with control signal, (b) master-slave D flip-flop in normal mode, (c) master-slave D flip-flop in test mode for stuck-at-1 fault, (d) master-slave D flip-flop in test mode for stuck-at-0 fault

In the normal mode, when the design is functioning as a master-slave flip-flop the values of the controls signals will be mC1 = 0 and mC2 = 1, sC1 = 0 and sC2 = 1 (as similar to values of the control signals C1 and C2 earlier described for the testable MX-CQCA based D latch thus keep away from the FO) this will help in copying the output of the negative, positive enable D latch that will be shown in Fig. 4 (b).

In the test mode,

1) To build the design testable with all 0s input vectors for any stuck-at-1 fault is shown in Fig. 4 (c), the values of the control signals will be mC1 = 0 and mC2 = 0, sC1 = 0 and sC2 = 0. This will create the outputs mT1, sT1equal to '0', which results in flouting the feedback and the

design becomes testable with all 0s input vectors for any stuck-at-1 fault.

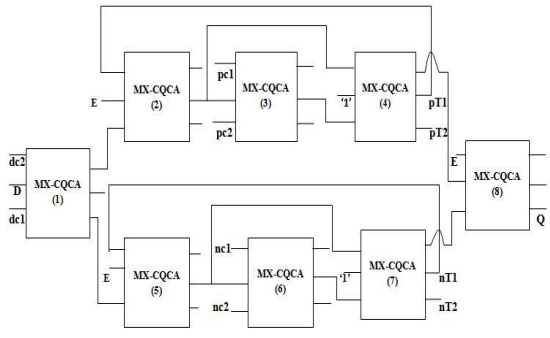
2) To build the design testable with all 1s input vectors for any stuck-at-0 fault is shown in Fig. 4 (d), the values of the control signals will be mC1 = 1 and mC2 = 1, sC1=1, and sC2 = 1. This will c outputs create mT1 and sT1 having a value of 1, flouting the feedback and resulting in the design testable with all 1s input vectors for any stuck-at-0 fault.

Using this methodology we can also create other type of master-slave flip-flops, such as the testable master-slave T flip-flop, testable master-slave JK flip-flop, and testable master-slave SR flip-flop, in which master is designed using the positive enable subsequent latch, while the slave is designed using the negative enable MX-CQCA gate-based latch.

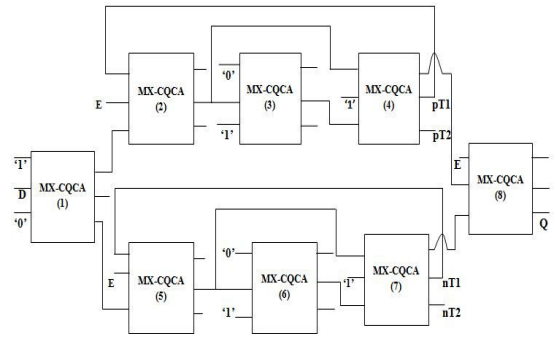
C. Design of MX-CQCA Logic Based Testable DET Flip-Flops

The DET flip-flop is a computing circuit that samples and stores the input data at both the edges that is at both the rising and the falling edge of the clock. In this proposed design of testable reversible DET flip-flop shown in Fig. 5 (a) the positive enable testable reversible D latch and the negative enable testable reversible D latch are combined in parallel manner. The MX-CQCA gates labeled as 2, 3 and 4 forms the positive enable testable D latch, while the MX-CQCA gates labeled as 5, 6 and 7 forms the negative enable testable D latch. In reversible logic fan-out is not allowed so the MX-CQCA gate labeled as 1 is used to copy the input signal D. The MX-CQCA gate labeled as 8 works as the 2:1 MUX and move the output from one of these testable latches (negative enable D latch or the positive enable D latch) that is in the storage state to the output Q.

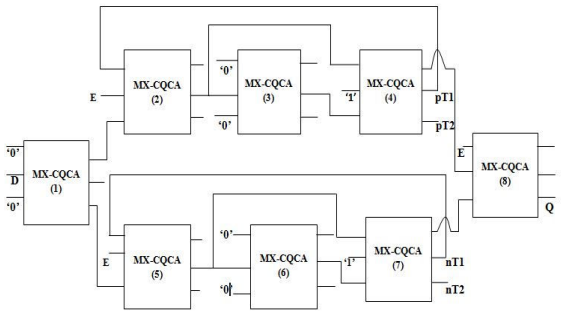
In the projected design, pC1 and pC2 are the control signals, which controls the testable positive enable D latch, while nC1 and nC2 are the control signals, which controls the testable negative enable D latch. Based on the values of the pC1, pC2, nC1, and nC2, the testable DET flip-flops bring either in normal mode or in the testing mode.



(a)



(b)



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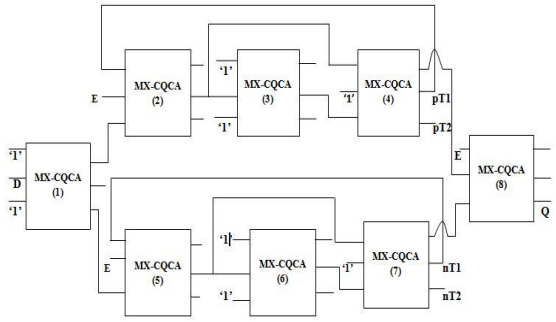


(d)

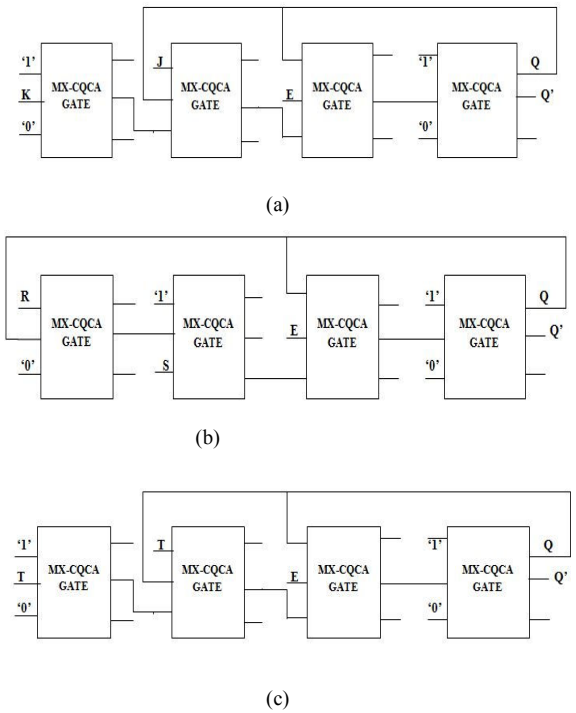
Fig. 5 Design of MX-CQCA gate based DET D-flip flop (a) DET D flip flop with control signal (b) MX-CQCA gate based DET D-flip flop in normal mode, (c) MX-CQCA gate based DET D-flip flop in test mode for stuck-at-1 fault, (d) MX-CQCA gate based DET D-flip flop in test mode for stuck-at-0 fault

1) Normal Mode: The normal mode of the DET flip flop is illustrated in Fig. 5 (b) in which the pC1 = 0, pC2 = 1, nC1 = 0, and nC2 = 1. The pC1 = 0, pC2= 1 help in copying the output of the positive enable D latch this will helping in copying the output of the positive enable D latch while then nC1=0 and nC2=1help in copying the output of the negative enable D latch.
2) Test Mode: This mode has two test modes.

a) All 1s Test Vectors: This mode is illustrated in Fig. 5 (c), in which control signals will have value as pC1 = 1, pC2 = 1, nC1 = 1, and nC2 = 1. The pC1= 1 and pC2=1 help in flouting the feedback of the positive enable D latch, while the nC1 = 1 and nC2 = 1 help in flouting the feedback of the negative enable D latch. This creates the

proposed work testable by all 1s test vector for any stuck-at-0 fault

b) All 0s Test Vectors: This mode is illustrated in Fig. 5(d), in which the control signals will have value as pC1 = 0, pC2 = 0, nC1 = 0, and nC2 = 0. The pC1 = 0 and pC2 = 0 help in breaking the feedback of the positive enable D latch, while the nC1= 0 and nC2 = 0 help in breaking the feedback of the negative enable D latch. This creates the proposed work testable by all 0s test vector for any stuck-at-1 fault



(a)

(b)

(c)

Fig. 6 Design of MX-CQCA logic based latches (a) JK latch, (b) SR latch, (c) T latch

III. Result Observation

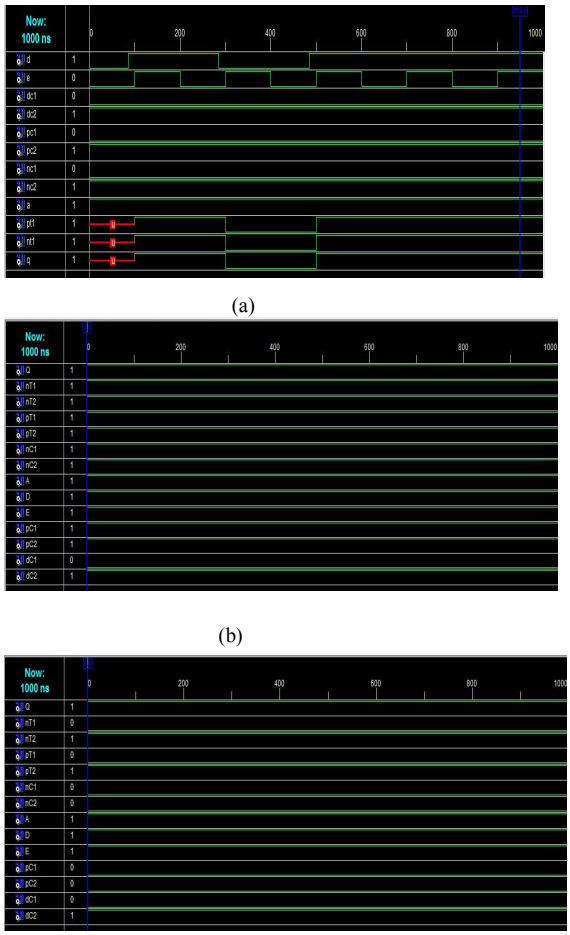
Our proposed work was implemented using Xilinx ISE simulator tool and their delay results are compared with the results obtained from the previous (Fredkin gate) design [13]. From this result comparison shown in Tables I and II, our proposed work is better than previous design [13].

TABLE I
RESEARCH OBSERVATION ON DELAY

Research Observation	Delay (ns)				
	Gate Delay	Normal D Latch design	D Latch with control signal	Master slave D flip flop	DET D flip flop
Fredkin Gate	6.32	6.437	7.646	10.313	9.458
Proposed Method (MX-CQCA Gate)	6.32	6.263	7.562	7.724	7.673

TABLE II
RESEARCH OBSERVATION ON POWER (MW)

Parameter / Design	Power (mW)		
	Fredkin Gate	Proposed Method (MX-CQCA Gate)	Power Reduction (%)
D-Latch with control signal	239.20	229.11	4.6 %
Master slave D flip flop	307.80	292.33	5.025 %
DET D flip flop	385.53	362.23	6.043 %



(a)

(b)

(c)

Fig. 7 Simulation result of MX-CQCA gate based DET D-flip flop at (a) normal mode, (b) test mode for stuck-at-1 fault, (c) test mode for stuck-at-1 fault

IV. Conclusion

This proposed design of new sequential circuits based on multiplexer conservative QCA logic gate is testable for any unidirectional stuck-at faults using only two test vectors, all 0s and all 1s. This design based on conservative logic gates progress the testability of a sequential circuit than the traditional gate and also reduces 20% delay that is classical gate produces *7.646ns* delay for normal D-latch design but this multiplexer conventional QCA logic gate has a delay of *6.347ns.* Similarly we had achieved 25.1% delay reduction for simple master-slave D-flip flop design when compare to previous method (fredkin gate). Power also comparatively

reduced using this MX-CQCA logic. This logic also reduces the area and power needed for the circuits, because nearly 1903 QCA cells are placed in 5.5μm^2 area. If the circuits is more complex, normal sequential circuits design thousands of test patterns to test all struck-at-faults, while if the same circuits is designed using the proposed work it can be tested by only using two test vector, all 0's and all 1's. The reduction in number of test vectors make light of the overhead of test time for a reversible sequential circuit. This QCA with reversible logic will become a more convenient ways to make a faster and denser circuit than the conventional CMOS logic.

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Maria Agnes.K received B.E degree in electronics and communication engineering from Dr.Sivanthi Aditanar College of Engineering, Tiruchendur, Tamilnadu, India in 2012 and pursed masters degree program in VLSI Design from Dr.Sivanthi Aditanar College of Engineering, Tiruchendur, Tamilnadu, India.E-mail: kennedyagnes.k@gmail.com

Joshua Bapu.J received B.E degree in electronics and communication engineering from Dr.Sivanthi Aditanar College of Engineering, Tiruchendur, Tamilnadu, India in 2006 and masters degree program in Applied Electronics from PSN College of Engineering, Tirunelveli,Tamilnadu, India in 2009.E-mail: joshuababu@gmail.com