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Simulation Based VLSI Implementation of Fast Efficient Lossless Image Compression System Using Adjusted Binary Code & Golumb Rice Code

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***Abstract*—**The Simulation based VLSI Implementation of FELICS (Fast Efficient Lossless Image Compression System) Algorithm is proposed to provide the lossless image compression and is implemented in simulation oriented VLSI (Very Large Scale Integrated). To analysis the performance of Lossless image compression and to reduce the image without losing image quality and then implemented in VLSI based FELICS algorithm. In FELICS algorithm, which consists of simplified adjusted binary code for Image compression and these compression image is converted in pixel and then implemented in VLSI domain. This parameter is used to achieve high processing speed and minimize the area and power. The simplified adjusted binary code reduces the number of arithmetic operation and achieved high processing speed. The color difference preprocessing is also proposed to improve coding efficiency with simple arithmetic operation. Although VLSI based FELICS Algorithm provides effective solution for hardware architecture design for regular pipelining data flow parallelism with four stages. With two level parallelisms, consecutive pixels can be classified into even and odd samples and the individual hardware engine is dedicated for each one. This method can be further enhanced by multilevel parallelisms.

***Keywords*—**Image compression, Pixel, Compression Ratio, Adjusted Binary code, Golumb Rice code, High Definition display, VLSI Implementation.

I. Introduction

THIS compression document is useful because it reduce the consumption of expensive resources, such as hard disk space or transmission bandwidth [1]. On the downside, compressed data must be decompressed to be used, and this extra processing may be unfavorable to some applications. For instance, a compression scheme for video may require expensive hardware for the video to be decompressed fast enough to be viewed as its being decompressed [5], [8]. Most lossless compression programs do two things in sequence: the first step generates a statistical model for the input data and the second step uses this model to map input data to bit sequences in such a way that "probable" (e.g. frequently encountered) data will produce shorter output than "improbable" data [2].

In Lossy compression technique, many sophisticated standards have been intensively developed such as JPEG and JPEG 2000 for still image and H.264 for multimedia communications and high-end video applications, respectively [5], [8]. Therefore the both algorithm and hardware implementation have attracted massive research effort for the evolution of lossy compression technique. Lossless compression can remove redundant information and the reconstructed procedure is as same as original information. The decoded information is exactly identical to original information [9].

FELICS algorithm can provide more efficient coding principle without data dependency, and maintain competitive coding efficiency [6]. Two main techniques, including simplified adjusted binary code and Golomb–Rice code with storage-less k parameter selection, are incorporated. The proposed color difference preprocessing (CDP) can efficiently improve the coding efficiency with simple arithmetic operation [4].

The rest of this paper is organized as follows. In Section II, the Description of the Methods is introduced. Section III presents Detailed Description of VLSI-oriented FELICS algorithm and the proposed hardware architecture of VLSI-oriented FELICS algorithm. Experiment results and discussions are described in Section IV. Finally, the conclusions and further enhanced are given in Section V.

II. Description of the Methods

The intensity distribution model is exploited to predict the correlation between current pixel and reference pixels. In this model, the intensity that occurs between L and H is with almost uniform distribution and regarded as in range.

A. Adjusted Binary Code

The adjusted binary code takes the sample of P-L to be encoded, and range indicates that the number of possible samples should be encoded for a given delta. The upper bound and lower bound denote the maximum and minimum number of bit to represent the codeword for each sample, respectively [10]. Particularly, the lower bound is identical to upper bound, while the range is exactly equal to the power of two. The threshold and shift number are utilized to determine which sample should be encoded with upper bound bit or lower bound bit. If delta = 4, the range is equal to (0, 4). The

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required number of bit is 2 for lower bound and 3 for upper bound. With the intensity distribution in range, 2 bits are allocated for the middle section, including sample of (1, 2, 3), and 3 bits for side section, including sample of (0, 4).

To describe the coding flow of adjusted binary code, the coding parameters should be first declared as follows:

delta=H-L

range=delta+1

upper_bound=[$\log_2$(range)]

lower_bound=[$\log_2$(range)]

threshold=$2^{upper\_bound} - range$

TABLE I
CODEWORD OF ADJUSTED BINARY CODE

Sample of P-L	0	1	2	3	4
Codeword	111	00	01	10	110

B. Coding Flow

First two pixels at first row are directly packed into bit stream without any encoding procedure. Find the corresponding two reference pixels N1 and N2.

Assign L=min(N1,N2),

H=max(N1,N2).

III. VLSI BASED MODIFIED FELICS ALGORITHM

A. Simplified Adjusted Binary Code

To make a simplified adjusted binary code, a compact probability distribution model, SSGM, is adopted to reduce the arithmetic operation in adjusted binary code [7]. With SSGM, the smaller residual less than threshold is allocated with shorter codeword, and the longer codeword is assigned to the residual greater than or equal to threshold.

The parameter computation generates the coding parameters; the circular rotation shifts the sample less than threshold to middle section and the others to both side sections. After circular rotation, the codeword generation adds threshold to the sample, which is greater than or equal to threshold, in side section and encodes it with upper bound bit. The lower bound bit is assigned to the other samples in middle section. As a result, the codeword length of each sample is consistent with the probability distribution of in range. The processing speed could be seriously limited.

B. VLSI Oriented Complex Coding Flow in Adjusted Binary Code

The adjusted binary code is partitioned into three coding procedures:

- Parameter Computation
- Circular Rotation
- Codeword Generation

The parameter computation generates the coding parameters; the circular rotation shifts the sample less than threshold to middle section and the others to both side sections. After circular rotation, the codeword generation adds threshold to the sample, which is greater than or equal to threshold, in side section and encodes it with upper bound bit [3]. The lower bound bit is assigned to the other samples in middle section. As a result, the codeword length of each sample is consistent with the probability distribution of in range.

IV. RESULTS AND DISCUSSION

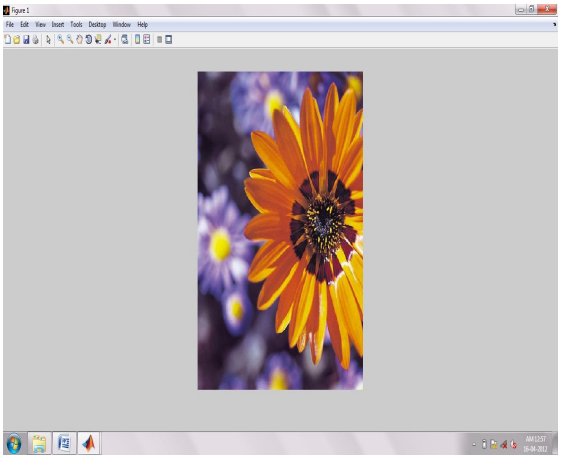

Fig. 1 Input Image

Fig. 1 represents as input color image. These input figure is the RGB based Color image. The size of the input image is 640*480. The input image is given for compression.

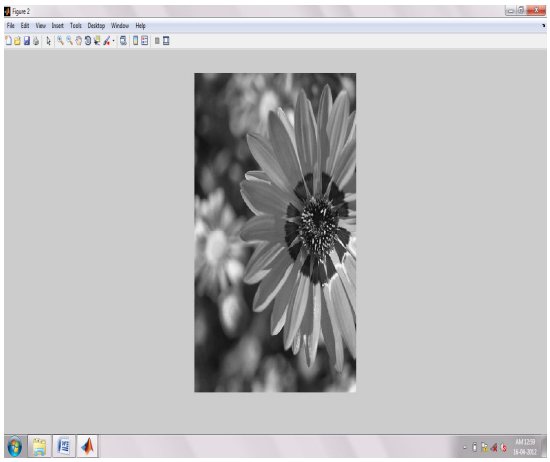

Fig. 2 Gray level Image

Fig. 2 represents as the color input image is converted in to gray level image. The size of the gray level image is 640*480. Fig. 3 represents as the gray image is converted in to resize of the image. So the image size can be reduced. The size of the resized image is 10*10.The resized image consists of 100 pixels (10x10).

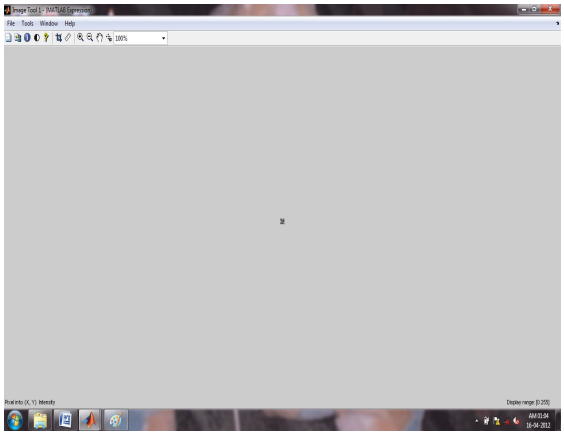

Fig. 3 Re-Sized Image

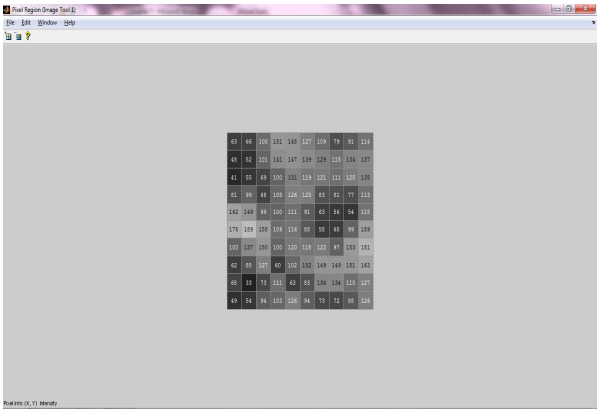

Fig. 4 Pixel Value of an Image

Fig. 4 represents the Pixel value of the resized compressed image. So the image size can be converted in to pixel of the text value. The pixels values are taken and given as input to the prediction template. Each pixel value is shown in the figure.

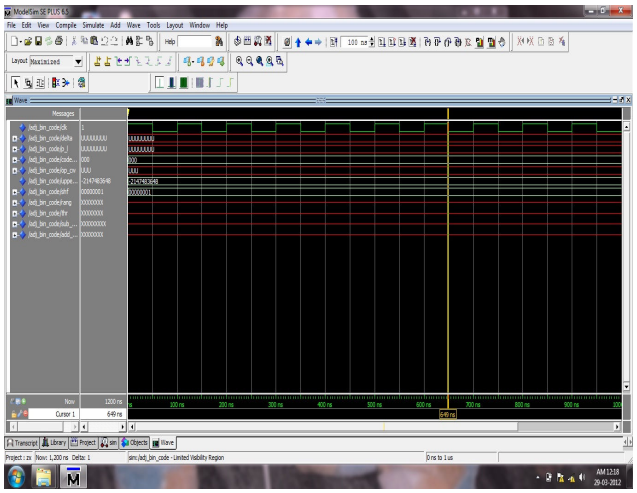

Fig. 5 Output for Simplified Adjusted Binary Code

Fig. 5 represents the output wave form for the simplified adjusted binary code. The input of the simplified adjusted binary code is the output of the intensity processing. A compact probability distribution model is adopted to reduce the arithmetic operation in adjusted binary code. The smaller residual less than threshold is allocated with shorter code word and the longer codeword is assigned to the residual greater than or equal to threshold.

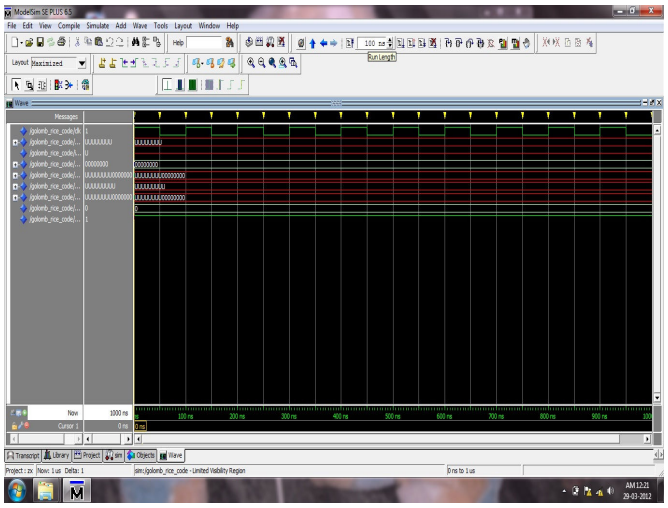

Fig. 6 Output for Golumb Rice code

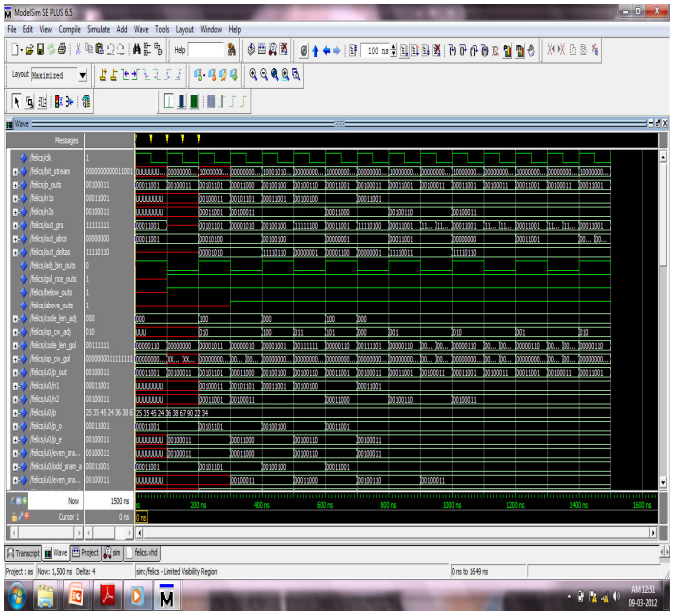

Fig. 7 Output Waveform

Fig. 6 represents the output wave form for the Golumb Rice code and also Fig. 7 represents the final output for FELICS output wave. The input of the FELICS Output wave is the output of Bit stream generator. These input values are applied to the FELICS Output wave and its produced or we measured low power, small area and high speed. Code word and code length is taken from the FELICS output wave. Simplified Adjusted Binary Code reduces the total arithmetic operation from 10 to 4. So the processing speed is increased. The number of Data's in Cumulating table for variable k parameter

is 1024. Whereas the number of data's for fixed k is 256. Therefore the area is also reduced.

A. FELICS Timing Summary

Minimum period= 29.639ns
Maximum Frequency= 33.739MHz
Minimum input arrival time before clock= Nil
Maximum output required time after clock= 6.140ns
Maximum combinational path delay= Nil

B. Design Summary

Logic Utilization

Total Number Slice Registers= 83 out of 13,824
Number used as Flip Flops= 67
Number used as Latches= 16
Number of 4 input LUTs= 203 out of 13,824

Logic Distribution

Number used as logic= 203
Number of bonded IOBs= 16 out of 510
IOB Flip Flops= 13
Total equivalent gate count for design= 2,121
Additional JTAG gate count for IOBs= 816

V. Conclusion and Future Enhancement

The Simplified Adjusted Binary Code and Golumb Rice code is used to reduces the number of arithmetic operation and improves processing speed. Here the Simplified Adjusted Binary Code is used to reduce the total arithmetic operation from 10 to 4. So the processing speed is increased and the number of Data's in cumulating table for variable parameter is 1024. Whereas the number of data's for fixed k is 256. Therefore the area is also reduced. Two-level parallelism and Four-stage pipelining are adopted, to increase the throughput of the Engine.

This method can be further enhanced by multilevel parallelism.

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