

New Design of a Broadband Microwave Zero Bias Power Limiter

K. Echchakhaoui, E. Abdelmounim, J. Zbitou, H. Bennis, N. Ababssi, M. Latrach

Abstract—In this paper a new design of a broadband microwave power limiter is presented and validated into simulation by using ADS software (Advanced Design System) from Agilent technologies. The final circuit is built on microstrip lines by using identical Zero Bias Schottky diodes. The power limiter is designed by Associating 3 stages Schottky diodes. The obtained simulation results permit to validate this circuit with a threshold input power level of 0 dBm until a maximum input power of 30 dBm.

Keywords— Limiter, microstrip, zero-bias.

I. INTRODUCTION

POWER Limiters (PL) are inserted in microwave circuits in order to protect sensitive components such as LNA (Low Noise Amplifier) and magnitude detectors from high power signals or pulses [1]-[10]. Conventional power limiters are made from solid state components especially PIN diodes [5]-[8], MESFET transistors [9]-[10], and Schottky diodes [11]-[13].

The aim of this study is to design a microstrip power limiter circuit. This limiter must respect the following specifications:

- The circuit must have a broad frequency band.
- The power limiter should have a high sensitivity for input power level.
- The circuit must provide at least limiting rate of 15 dB when the received power at the input of the limiter reaches 30 dBm.

In this paper, we are looking to achieve a low cost microstrip power limiter which will be inserted behind a Rectenna system [13] to protect it from high microwave powers. We have chosen a commercial Zero Bias Schottky diode HSMS2820 [14] to design the microstrip power limiter.

II. DESIGN APPROACH

Solid state limiters are mainly based on the reflection and absorption of a portion of the stream of a transmission line with discrete Schottky diodes, PIN diodes or MESFET transistors using similar topologies in Fig. 1 [8], [13]. These

devices must have minimal losses for incident low level signals. The evolution of these losses at higher power must then be proportional to the incident beyond a certain threshold power level [13].

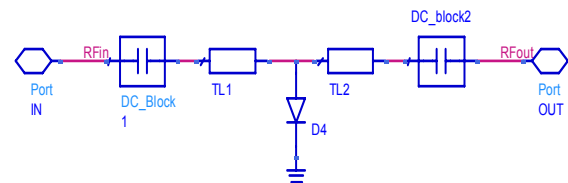


Fig. 1 Power Limiter topology

Usually, power limiters exploit the functionality of the impedance variation of the diode according to the electric current. Thus, the diode used to limit power is inserted in the circuit in anti-parallel form shunted between the transmission line and the common ground. When the power increases, the diode impedance decreases, and starts to absorb some of the received power.

Such circuit requires a bias voltage which allows the diode/MESFET transistors to switch to the forward state. The implementation of a bias voltage in a microwave circuit is not easy. Therefore, two solutions exist by choosing Zero-Bias diodes [8], [13]:

- By using two parallel diodes with an RF choke acting as DC return path and as open circuit for RF incident signal (Fig. 2).

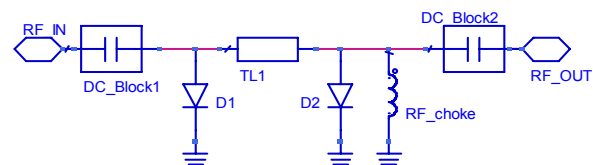


Fig. 2 Parallel diodes with an RF choke

- By using two diodes implemented in antipodal position as presented in Fig. 3. In this structure, each diode acts as return path for the other rectifier diode without the need of an RF choke (Fig. 3).

The last rectifying technique is not applicable for transistors [12], so we have chosen to work in this project with antipodal Schottky diodes another reason is that the use of Schottky diodes is simple and we can use them without bias.

As mentioned before, the commercial diode Avago HSMS2820 has been used to design the power limiter. This diode is a Surface Mount RF Schottky Diodes presented in

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SOT23/143 package [14].

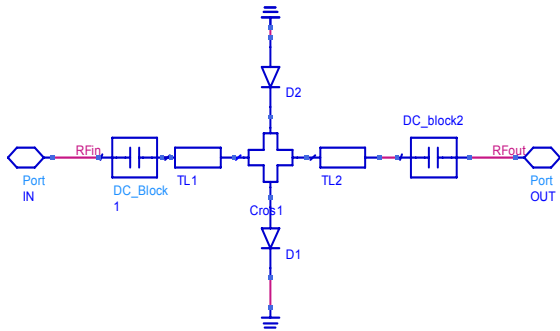


Fig. 3 Anti-dipole diode

Conforming to the datasheet, The HSMS282x family has been optimized for use in RF applications, such as [14]:

- DC biased small signal detectors to 1.5 GHz.
- Biased or unbiased large signal detectors (AGC or power monitors) to 4 GHz.
- Mixers and frequency multipliers to 6 GHz

This Schottky diode is modeled as a capacitance and variable resistance as presented in Fig. 4 [14]. This equivalent circuit can be enriched by packaging equivalent circuit [14]:

- R_j : is the nonlinear Schottky junction resistance. This resistance is proportional to the temperature and inversely proportional to the current passing through the diode.
- $R_j = \frac{8.33 \times 10^{-5} \cdot T}{I_b + I_s}$ where T: the ambient temperature, I_s : the saturation current and I_b : externally applied bias current.
- C_j : junction capacitance representing the contact between the metal and semiconductor.
- R_s : ohmic contact and parasitic series resistances. According to data sheet of the HSMS282x family, $R_s = 6 \text{ ohm}$.

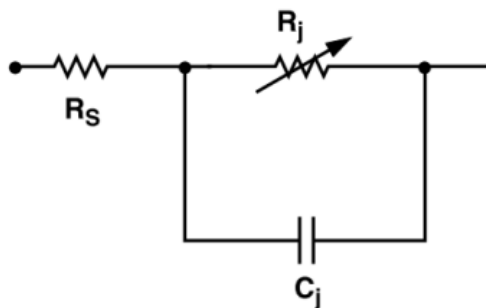


Fig. 4 Linear Equivalent Circuit Model Schottky Diode

To design the microwave power limiter we have used ADS software, for the simple reason that is suitable to RF design and contains in its library the different HSMS282x family. We have optimized three circuits in term of frequency band, insertion loss and attenuation rate when the power exceed the threshold limit.

The circuit is designed by using microstrip technology, based on an FR4 substrate with the following characteristics:

- Dielectric Loss tangent: 0.025

- Relative dielectric constant: 4.4
- Thickness of the substrate: $h = 1.6 \text{ mm}$

A. Power Limiter Design Based On 1 Stage

The first circuit shown in Fig. 5 is based on a single stage of two diodes shunted on a microstrip transmission line.

In order to get the best performances of this circuit, the two diodes must be spaced by around $(\lambda/2)$. In this position, the potential in anode of the diode D1 and the potential in the cathode of the diode D2 will have a phase distance around 180° .

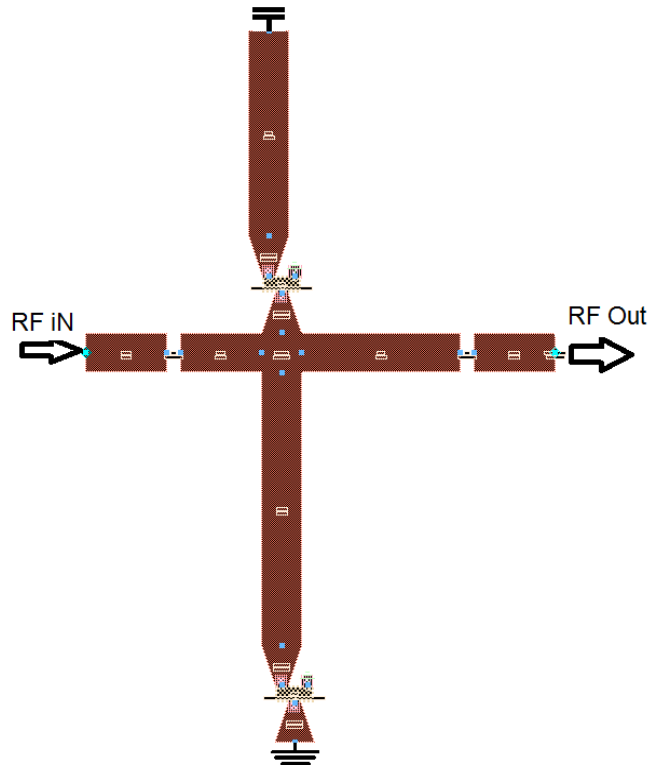


Fig. 5 Layout of power limiter based on one stage diodes

The different simulation results are presented in Figs. 6 and 7.

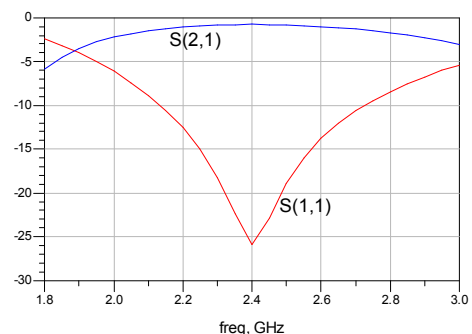


Fig. 6 S-parameters results Vs frequency

As shown by S-Parameters results, the limiter presents good matching input impedance in the ISM band (Fig. 6). The insertion loss is around -0.7dB.

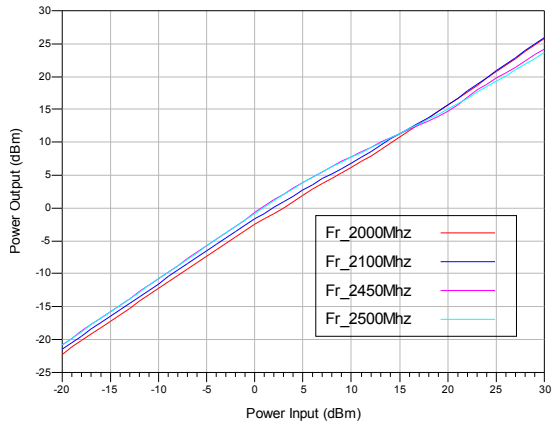


Fig. 7 Output Power Vs Input Power at 2, 2.1, 2.45 and 2.5 Ghz

Despite the fact that this circuit provides the low insertion loss, this design presents some limitations:

- High limiting power threshold: the limitation is activated when incident Power (P_{in}) reaches 5dBm.
- Low isolation at large signal (4.2 to 6.4 dB at $P_{in}=30$ dBm). These Values of protection will not be considered sufficient in many applications.

In order to improve the performances of this circuit, we have designed the second circuit based on two stages of diodes shunted on a microstrip transmission line.

B. Circuit with Two Stages

The simulation of the second circuit composed from 2 stages, is done by inverting the side of diode of one stage as presented in Fig. 8 (b), we obtain more important isolation (up to 18 dB).

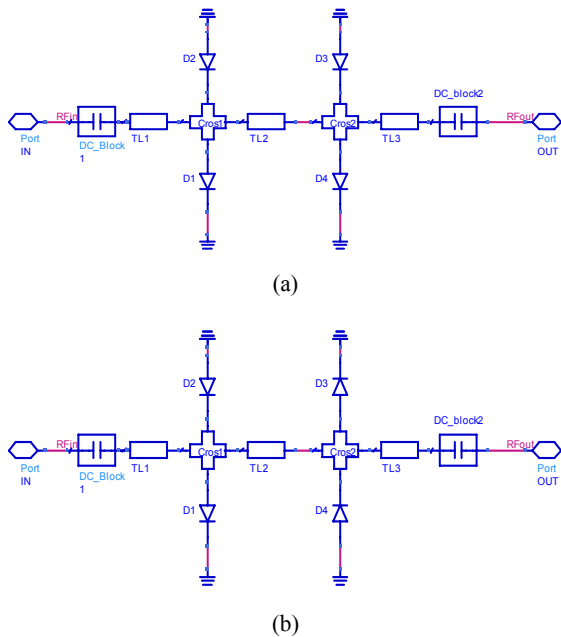


Fig. 8 Zero-bias Power Limiter (2 stages), (a) all diode are in the same side, (b) two stages diodes inverted

The simulation results are presented in Fig. 9 (S-parameters

results) and in Fig. 10 (Output Power Versus Input Power).

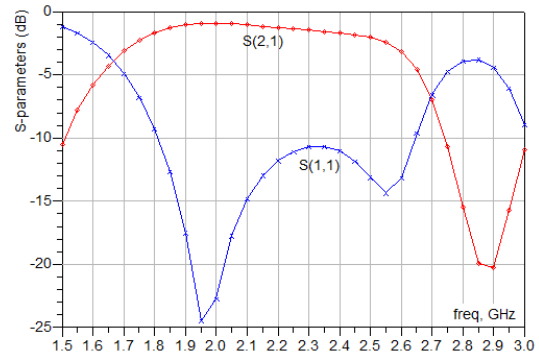


Fig. 9 The S-parameters results Versus Frequency

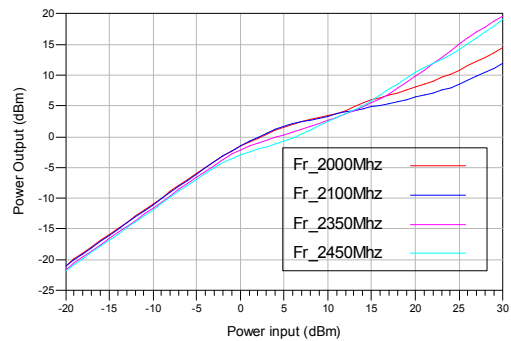


Fig. 10 Output Power Vs Input Power at 2, 2.1, 2.35, and 2.45 Ghz

Compared to one stage circuit, the two stages circuit presents better performance in isolation rate. However, it shows the following constraints:

- Limiting power threshold is around 2.5 dBm
- The isolation rate for 2.45 Ghz frequency is not sufficient (11 dB).

To achieve highest isolation rate, we have also designed and simulated the three stages limiter as presented below.

C. Circuit with Three Stages

The third circuit shown in Fig. 11 is based on three stages of diodes shunted on a microstrip transmission line.

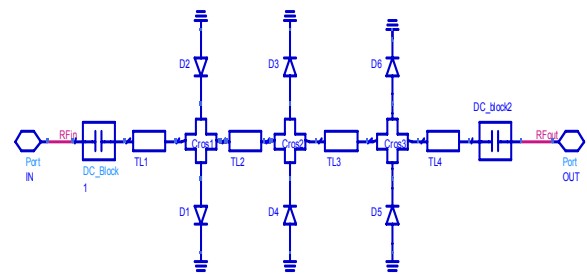


Fig. 11 Zero-bias Power Limiter (3 stages)

The simulation results are presented in Fig. 12 (S-parameters results) and in Fig. 13 (Output Power Versus Input Power).

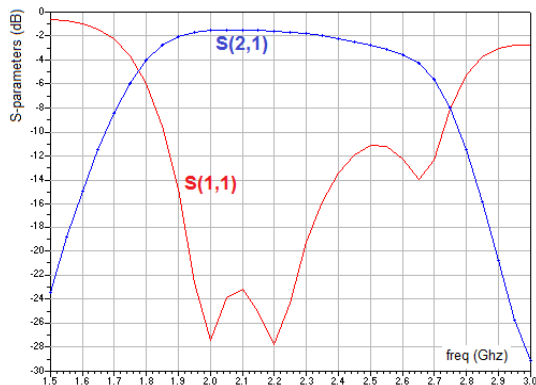


Fig. 12 The S-parameters results Versus Frequency

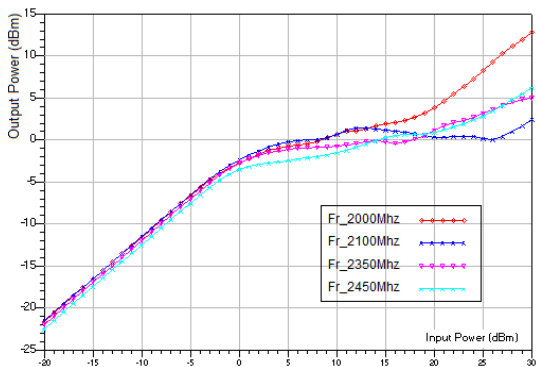


Fig. 13 Output Power versus input power at 2, 2.1, 2.35, and 2.45 Ghz

As shown in the simulation results presented in Figs. 12 and 13, this circuit improves significantly the isolation at large signal (27.5 dB at F=2.1 Ghz) and reduce the limiting power threshold to 0 dBm. However, the insertion loss is slightly increased around 1.5 dB.

III. CONCLUSION

In this paper, we have designed and simulated three microstrip microwave power limiter circuits based on Zero-Bias Schottky diodes. The limiter based on three diodes stages presents quasi ideal limiting power characteristic and achieves better performances in terms of isolation rate and limiting power threshold. The dimensions of the layout generated for this circuit are 58.65 mm x 69.42 mm.

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