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An Approach for Modeling CMOS Gates

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***Abstract*—**A modeling approach for CMOS gates is presented based on the use of the equivalent inverter. A new model for the inverter has been developed using a simplified transistor current model which incorporates the nanoscale effects for the planar technology. Parametric expressions for the output voltage are provided as well as the values of the output and supply current to be compatible with the CCS technology. The model is parametric according the input signal slew, output load, transistor widths, supply voltage, temperature and process. The transistor widths of the equivalent inverter are determined by HSPICE simulations and parametric expressions are developed for that using a fitting procedure. Results for the NAND gate shows that the proposed approach offers sufficient accuracy with an average error in propagation delay about 5%.

***Keywords*—**CMOS gate modeling, Inverter modeling, transistor current model, timing model.

I. Introduction

ACCURATE modeling of CMOS gates is of major importance for the IC technology. Timing and power consumption models are used for making predictions for the operation of the circuits before their construction. By this way, the satisfaction of the specification requirements is ensured during the design procedure avoiding costly, in time and money, manufacturing iterations.

Last years, current based models [1] are used by industry for the timing and power analysis of the integrated circuits. For example, this is the case of the Composite Current Source (CCS) technology [2], [3] of Synopsys. The waveforms of the supply and output currents are captured in all the design corners and are stored in .lib files. This information is used by the simulation compiler to proceed to circuit characterization (e.g. propagation delay, output voltage slew, power consumption). This approach has been proven very effective in modeling the nano-scale effects of current technologies with an accuracy of 2% regarding BSIM. However, the need of storing pre-characterized information for all the design corners requires a circuit simulation step and also leads to large files. The manipulation of these files by the simulation compiler to provide the circuits characteristics implies time-consuming accesses.

Different approaches have been proposed in the literature for gate modeling [4], [5] to avoid circuit simulation and accelerate the characterization procedure. Since the direct analysis of the operation of the gates is a cumbersome problem, these approaches are based on the analysis of the operation of the simple inverter. They try to find an equivalent inverter to have a similar response with that of the gate and use the inverter model to extract the behavior of the gate. The equivalent inverter is determined by mapping the NMOS and PMOS transistor structures of the gates to single NMOS and PMOS transistors, respectively, with an appropriate width. This imposes a complex analysis of the transistor structures and exploits some characteristics of the transistor operation to that can be solved. Such an approach can lead to an equivalent inverter which provides similar output voltage and current waveforms with the gate it corresponds to.

Nano-scale effects have changed significantly the operation of the transistor so that older methods can't further be applied. For example, in [4], [5] the assumption for a conducting series transistor structure (e.g. the NMOS structure in a NAND gate) that only the top transistor can be in saturation is no further valid since of the significant channel length modulation effect. Thus, new approaches have to be defined for gate modeling to take into account the new phenomena imposed by shrinking the transistor dimensions.

In this paper, a modeling approach for CMOS gates based on the use of the equivalent inverter is presented. To evaluate the whole modeling approach, at first, a simple but accurate transistor current model is developed to take into account the nanoscale effects. This is used for the analysis of the operation of the inverter. Analytical expressions for the output voltage, the propagation delay and the output voltage waveform slew of the inverter are provided. Furthermore, it provides the supply and output current values needed in CCS files to exploit the current EDA technology for timing and power analysis. The model is fully parametric regarding input signal slew, τ, output load, C_{out}, transistor widths, W, supply voltage, V_{DD}, and temperature, T.

To specify the efficiency of the equivalent inverter approach in modeling of CMOS gates, the transistor sizes of the equivalent inverter of a NAND gate were determined by simulation. HSPICE simulations in all the design corners, defined by the used library, and for different values of W_n, V_{DD} and T were performed. Transistor widths of the inverter which provides a similar response to the NAND gate were determined. Parametric expressions for the transistor widths were produced by a fitting procedure. Since, they are the most accurate values for the transistor sizes than corresponding methods can provide, the overall approach of the equivalent inverter, as a concept idea, is evaluated. As a case study the industrial oriented NangateOpenCellLibrary [6] for the 45nm PTM technology [7] is used.

II. Transistor Current Model

Analytical expressions have to be derived for the output waveform of the inverter. This means that the differential equation which describes the operation of the inverter has to be solved analytically. Consequently, a simplified but still

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accurate model for the transistor current should be used. Here, a modification of the transistor drain current model presented in [8] has been employed to include analytical expressions for the threshold voltage V_t and the DIBL factor η_{DIBL}. Since the subthreshold current has a significant impact in nanoscale technologies it is taken also into consideration. Also, the modified drain current model is extended to include the temperature dependence of the device parameters.

The modified expressions of the transistor current, we use, are:

$$I_{ds} = \begin{cases} I_o\left(1-\frac{W_m}{W}\right)e^{\frac{V_g-V_t}{n(kT/q)}}\left(1-e^{\frac{-V_d}{(kT/q)}}\right), & \text{Subthreshold} \\ B\left(1-\frac{W_m}{W}\right)\left(\frac{V_g-V_t}{V_{to}}\right)^a \frac{V_d}{V_{dsat}}, & V_d \le V_{dsat} \\ B\left(1-\frac{W_m}{W}\right)\left(\frac{V_g-V_t}{V_{to}}\right)^a \left[1+\lambda\left(V_d-V_{dsat}\right)\right], & V_d > V_{dsat} \end{cases} \quad (1)$$

with

$$V_t = V_{t0} - n_{DIBL}V_d,\ W_m = a_1 + a_2 W \quad (2)$$

where the first expression of (1) represents the subthreshold drain current, while the other two represent the drain current for below (linear) and above (saturation) V_{dsat} operation. The discontinuity between the current of the subthreshold and linear regions has insignificant influence on the output voltage waveform. The expressions for I_o, B and V_{dsat} are given by:

$$I_o = \left(\frac{W}{L}\right)\mu C_{ox}\left(\frac{nkT}{q}\right)^2$$
$$B = \left(\frac{W}{L}\right)\mu C_{ox} V_{to}^2 \quad (3)$$
$$V_{dsat} = K\left(\frac{V_g - V_t}{V_{to}}\right)^m$$

The temperature dependence of mobility, is expressed as

$$\mu \propto T^{-2.4} \quad (4)$$

III. The Inverter Model

In Fig. 1 the structure of the inverter to be analyzed is shown. Parasitic capacitances are also presented. C_m is the coupling capacitance between input and output node, corresponding to gate-to-drain capacitance of both transistors. C_{db} corresponds to drain-to-bulk capacitance and presents a critical role in the accuracy of the model [9]. C_{out} corresponds to output load capacitance.

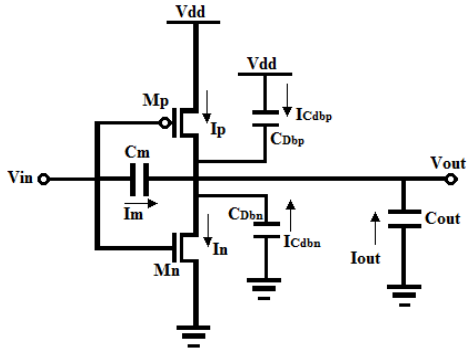

Fig. 1 Studied Topology for the inverter

The operation of this circuit is described by the differential equation resulted by applying the Kirchoff's current law at the output node:

$$I_n + C_{dbn}\frac{dV_{out}}{dt} = I_p - C_{out}\frac{dV_{out}}{dt} + C_m\left(\frac{dV_{in}}{dt} - \frac{dV_{out}}{dt}\right) - - C_{dbp}\frac{dV_{out}}{dt} \quad (5)$$

where I_n, I_p are the transistors currents given by (1). Solving this equation in all the operation regions, an analytical expression for the output voltage node is derived. A parametric ramp is used as input signal, rising or falling. Appropriate average values according to the transistor operation mode are defined for the parasitic capacitances using HSPICE simulations. The derived expressions are parametric according the input signal slew, output load, transistor widths, supply voltage and temperature. Table I shows the design corners defined by the used library and the range of the values of the parameters.

TABLE I
Parameter Corners and Ranges

Input slew, τ (ps)	2.9, 12, 43, 102, 195, 325, 496
Load capacitance, C_{out} (fF)	0.37, 1.9, 3.8, 7.6, 15.1, 30.3, 60.6
NMOS transistor width, W_n (nm), (range)	90 - 400
Supply voltage, V_{DD} (V), (range)	0.7 - 1.25
Temperature, T (°C), (range)	0 - 125

A first version of the inverter model has been presented in detail in [10], where the output voltage expressions in any region of operation are provided. However, in order to adapt the proposed model to an industrial library with a large number of design corners a modification in the solution flow was found to be necessary to keep accuracy in the desired levels. This modification includes the definition of one more region of operation, where both transistors are in saturation and the use of a linear approximation for the term $(V_{GS} - V_T)^a$.

Using the expression of the output voltage, the expression of the output current in C_{out} is given as $I_{out}=C_{out}(dV_{out}/dt)$. The supply current is determined after defining parametric expressions for the parasitic capacitances. In this way, the proposed model becomes compatible to the CCS technology. Closed forms for the propagation delay, the output voltage waveform slope and the short-circuiting power consumption are also provided. A C++ code has been produced for the proposed model and compiled in a Linux environment. For

various cases, an acceleration of 90-150 times compared to HSPICE was determined.

In Fig. 2 the output voltage waveform for a rising input, V_{DD}=1V, T=25°C, τ=102ps, C_{out}= 7.6f and W_n=200nm, is shown. W_{pmos}=1.5W_{nmos}. The corresponding HSPICE simulation result is also shown (solid line).

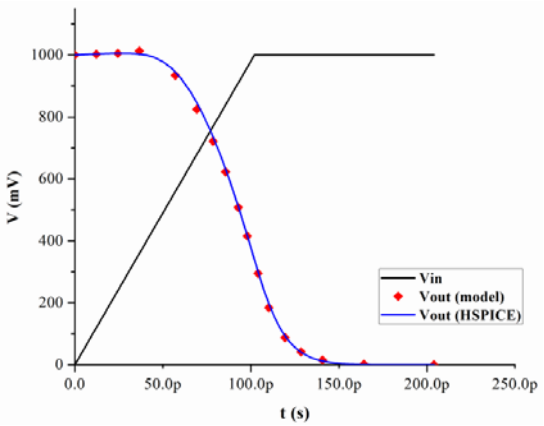

Fig. 2 V_{out} comparison between HSPICE simulations and the proposed model for a rising input case

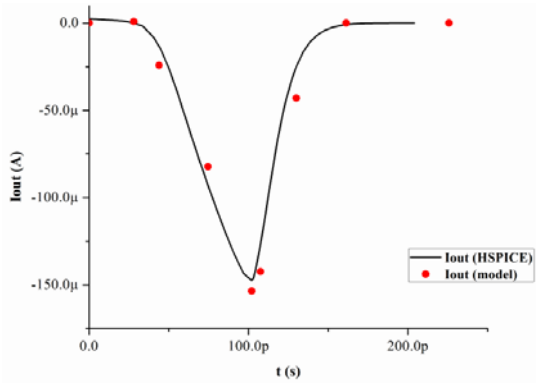

Fig. 3 Output current waveform for the same (Fig. 2) inverter configuration

In Fig. 3 the output current waveform is presented for the same inverter configuration. For both, the accuracy of the method is obvious.

In Table II comparisons for the propagation delay are provided for various design corners and for T=25°C. An average error of 3% with a maximum less than 10% is presented in all the corners for the typical case (V_{DD}=1V, T=25°C). For T=25°C and in whole the range of the V_{DD} the average error increases to 4.5% while for different values of T the error goes to about 8%.

IV. Modeling CMOS Gates

According to the proposed approach the CMOS gate is replaced by an equivalent inverter and the model for the inverter is used to provide the output voltage and current waveform expressions. The equivalent inverter is defined as the one which provides the same propagation delay and presents a supply current similar to that of the gate. A number of simulations are performed for the gate in all the design corners and for different values of the parameters. The appropriate widths of the transistors of the inverter are defined for any configuration. Then a fitting procedure is applied and parametric expressions for the transistor widths are derived.

TABLE II
Evaluation Results Regarding Propagation Delay

$W(nm)$	$C_{out}(fF)$	τ 10ps			τ 100ps		
		HSPICE	Model	Error	HSPICE	Model	Error
V_{DD} = 0.8V							
100	0.5	8.9ps	9.3ps	4.5%	24.7ps	23.2ps	6%
	15	114.6ps	118.2ps	3.1%	136.8ps	141.9ps	3.7%
400	0.5	6.2ps	6.5ps	4.8%	16.4ps	17ps	3.7%
	15	31.4ps	33.2ps	5.7%	54ps	56.7ps	5%
V_{DD} = 1.1V							
100	0.5	6.6ps	6.8ps	3%	10.3ps	9.7ps	5.8%
	15	81.6ps	78.9ps	3.3%	96.7ps	97.6ps	0.9%
400	0.5	4.2ps	4.4ps	4.8%	4.3ps	4.1ps	4.7%
	15	22.3ps	22.3ps	0%	37ps	36.4ps	1.6%

For the 2-input NAND gate, the PMOS transistor width of the equivalent inverter is considered equal to the PMOS transistor of the gate while an appropriate width is determined for the NMOS transistor emulating the behavior of the series transistor structure of the gate. In the equivalent inverter the output load has to slightly be increased to include the impact of the parasitics on the output node of the extra transistor area of the gate. Similar approaches can be used for other gates.

In Fig. 4 the output voltage waveform of the NAND gate for a rising input to the bottom transistor (the other is "1") is compared to that of the equivalent inverter (the model presented in section III is used). The width of the equivalent transistor is calculated by the derived expressions. This is for V_{DD}=1V, T=25°C, τ=102ps, C_{out}= 7.6f and W_n=200nm. In Fig. 5 the output current waveform is presented. The accuracy is obvious for both cases. In Table III evaluation results regarding the propagation delay are provided. An average error around 5% is determined.

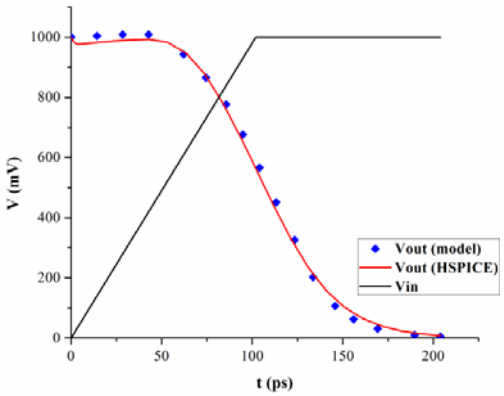

Fig. 4 Output voltage waveform of the NAND gate (HSPICE) for a rising input to the bottom transistor (the other is "1") compared to that of the equivalent inverter

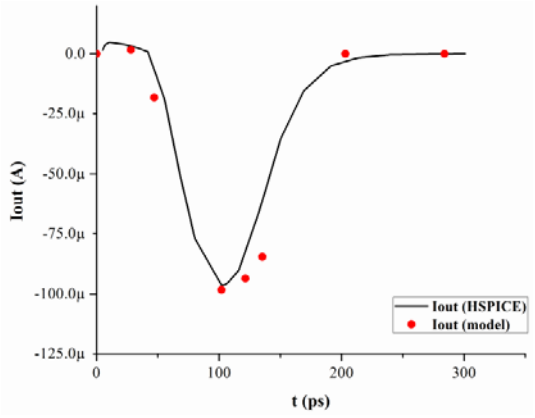

Fig. 5 Output current comparison for the NAND gate (HSPICE) with a rising input to the bottom transistor (the other is "1") and the equivalent inverter

TABLE III
EVALUATION RESULTS FOR MODELING THE NAND GATE REGARDING PROPAGATION DELAY (T=25°C)

		$V_{DD} = 0.7V$					A1 Rising
		τ 10ps			τ 100ps		
$W(nm)$	$C_{out}(fF)$	HSPICE	Model	Error	HSPICE	Model	Error
100	0.5	20.1ps	22.1ps	9.95%	41.9ps	41.4ps	1.2%
	15	276ps	280ps	1.45%	300.8ps	284ps	5.58%
400	0.5	12.9ps	15.3ps	18.6%	30.4ps	33.7ps	10.9%
	15	74.2ps	76.5ps	3.1%	94.1ps	92.8ps	1.38%
		$V_{DD} = 1V$					A2 Falling
		τ 10ps			τ 100ps		
$W(nm)$	$C_{out}(fF)$	HSPICE	Model	Error	HSPICE	Model	Error
100	0.5	15.2ps	14.8ps	2.63%	33.4ps	31.6ps	5.39%
	15	177.1ps	174.4ps	1.55%	196.5ps	192.3ps	2.14%
400	0.5	10.6ps	10.7ps	0.94%	24.9ps	26.6ps	6.83%
	15	49.7ps	50ps	0.6%	69ps	68ps	1.45%

V. Static Power Consumption Model

Static power consumption is very critical in nanoscale technologies and its accurate modeling is of high importance. The equivalent inverter approach can model accurately propagation delay and other timing characteristics as well as switching power consumption. It fails to model reliably the static power consumption since the transistor width of the equivalent inverter is defined to model transient characteristics.

For parametric static power consumption model regarding CMOS gates a more efficient approach is based on the use of power contributors as they are presented in [11].

VI. Conclusions

The equivalent inverter approach for modeling CMOS gates has been evaluated. An analytical and parametric inverter model has been developed and used for this purpose. It is parametric according to the input signal slew, output load, transistor widths, supply voltage, temperature and process. A fitting procedure has been employed to determine the transistor widths of the equivalent inverter. Expressions for the output voltage waveform are provided as well as values for the output and supply currents to be compatible to the CCS technology. The results show that voltage and current waveforms of the gates are predicted with very good accuracy.

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