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Impact of Height of Silicon Pillar on Vertical DG-MOSFET Device

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***Abstract*—**Vertical Double Gate (DG) Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is believed to suppress various short channel effect problems. The gate to channel coupling in vertical DG-MOSFET are doubled, thus resulting in higher current density. By having two gates, both gates are able to control the channel from both sides and possess better electrostatic control over the channel. In order to ensure that the transistor possess a superb turn-off characteristic, the subs-threshold swing (SS) must be kept at minimum value (60-90mV/dec). By utilizing SILVACO TCAD software, an n-channel vertical DG-MOSFET was successfully designed while keeping the sub-threshold swing (SS) value as minimum as possible. From the observation made, the value of sub-threshold swing (SS) was able to be varied by adjusting the height of the silicon pillar. The minimum value of sub-threshold swing (SS) was found to be 64.7mV/dec with threshold voltage (V_{TH}) of 0.895V. The ideal height of the vertical DG-MOSFET pillar was found to be at 0.265 µm.

***Keywords*—**DG-MOSFET, pillar, SCE, vertical

I. Introduction

THE Double-gate Metal Oxide Semiconductor Field Effect transistor (MOSFET**)** has been actively researched especially in terms of minimizing short channel effect (SCE). One of the popular types of double-gate MOSFET is known as vertical DG-MOSFET. The basic architecture of vertical DG-MOSFET consists of a silicon ridge of few tenth of nanometer in thickness, which is regarded as the active area of the MOSFET [1]. It might be recognized as a silicon pillar separating two gates. The channel length of the vertical DG-MOSFET is normally adjusted by ion implantation and diffusion techniques. The advantage of the vertical DG-MOSFET is that the channel length is not dependent on the use of lithography. It can be easily fabricated with both back gates aligned together [2]. The main advantage of this architecture is due to its high possibility in reducing short channel effect (SCE).

Short channel effect (SCE) has become the main problem in conventional MOSFET device structure. SCE occurs when the source and drain region become too close to each other. If the effective channel length (L_{eff}) becomes too short, the depletion region from drain will reach the source region and subsequently reduces the barrier for electron injection. As consequences, leakage current (I_{OFF}) and drain induced barrier lowering (DIBL) will be increased. The way to overcome this problem is by constructing vertical pillar. As the drain region is located on the top of pillar, the effective channel length (L_{eff}) will not be dependent with physical gate length (L_g). Hence, any reduction on physical gate length (L_g) will not affect much on the effective channel length (L_{eff}).

Double-gate architecture was initially implemented in order to pursue the characteristic of a perfect switch. The term perfect switch refers to the transistor's ability to switch instantly from 'OFF' condition to 'ON' condition or vice versa [3]. In other words, a transistor is open, there is no current flow. And when the switch is closed, it is expected that there should be no resistance. As a transistor shrunk in size, switching will become poorer. This happens due to off current is not zero during an open switch. As a result, switching time is increased and the transistor's performance becomes poor. The way to overcome this problem is to design a gate electrode that is wrapped around several sides of the conducting channel, hence improving electrostatic control of the transistor [3].

The excellent switching speed characteristic can be obtained by controlling the subs-threshold swing (SS). Subs-threshold swing (SS) occurs when V_{GS} is smaller than but close to V_{TH} [4]. At this moment, transistor is said to be in sub-threshold or weak inversion region. SS is always regarded as an important parameter which indicating the scalability limits of DG-MOSFET. It actually depict how effectively the drain current's flow could be stopped when gate-to-source current (V_{GS}) is decreased below $V_{TH.}$

The good switch-off characteristic of a vertical DG-MOSFET can be realized by gate to gate capacitive coupling [5]. The voltage of both sides of the gates swing synchronously and then induces the same amount of potential charge within the channel. This will create an excellent electrostatic control of the gate over the sub-threshold leakage current. It shows how much change in the gate voltage is required to change the drain current by one decade. This response characteristic is known as sub-threshold swing and is expressed in (1) [4]:

$$SS = \left[\frac{d(\log_{10} I_{DS})}{dV_{GS}} \right]^{-1} \quad (1)$$

II. Material and Methods

A. N-Channel Vertical DG-MOSFET Device Design Using SILVACO TCAD

P-type silicon with <100> orientation is used as the main substrate for this experiment. Initial silicon was then injected

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by boron with concentration of $1x10^{15}$ atom/cm^3. The silicon was etched in order to form a pillar or a ridge that separates the two gates. The simulation process was followed by the gate oxidation process. The gate oxidation process used the dry oxidation method instead of wet oxidation because the thickness of oxidation can be better controlled through dry oxidation. The thickness of gate oxide was a very important parameter in vertical dimension that determines the gate control. The next step was to dope a substrate ion (boron) into the silicon with concentration of $9.55x10^{12}$ atom/cm^3. This was actually done for the purpose of threshold voltage adjustment in the Vertical DG-MOSFET.

The next simulation process was to deposit polysilicon on top of the gate oxide, and a layer of oxide was developed on top of the polysilicon deposition. The polysilicon and polysilicon oxide was etched away to form a gate polysilicon. The gate was made of polysilicon due to its ability of preventing source/drain ions to be penetrated into a channel region.

Phosphor dosage of $1x10^{18}$ atom/cm^3 was then doped into polysilicon gate. This was done in order to increase the conductivity of polysilicon since polysilicon is a low conductivity metal. The conductivity of the gate would affect the switching frequency of the transistor.

In order to get an optimum performance for Vertical DG-MOSFET device, indium was doped in the substrate. After the process of halo doping, sidewall spacers were deposited. Sidewall spacers were then used as a mask for source/drain implantation. They were actually used to separate the gates with source/drain metal as to prevent them from being short-circuited since there is always process variation occurring in the fabrication process. Arsenic atom with concentration of 1.25×10^{18} was implanted to ensure the smooth current flow in Vertical DG-MOSFET device.

Compensation implantation is utilized later by implanting phosphor dosage of $2.51x10^{12}$ atom/cm^3. This step was taken in order to reduce parasitic effects that can lower the current. The top of the structure was then contacted with aluminum metal. The aluminum layer was deposited on the top of the structure's surface and any unwanted aluminum was etched to develop the contacts [6], [7]. Next, the metallization and etching were performed to form electrode at drain, source and gate.

The final vertical DG-MOSFET device structure was completed by mirroring the right-hand side structure as depicted in Fig. 1. The flowchart of simulation process is illustrated in Fig. 2.

After the devices were built by utilizing **ATHENA** module, the designed device was then simulated in **ATLAS** module in order to extract electrical characteristics such as the I_D versus V_{GS} curve. The subs-threshold swing (SS) value was then extracted from that particular curve [8].

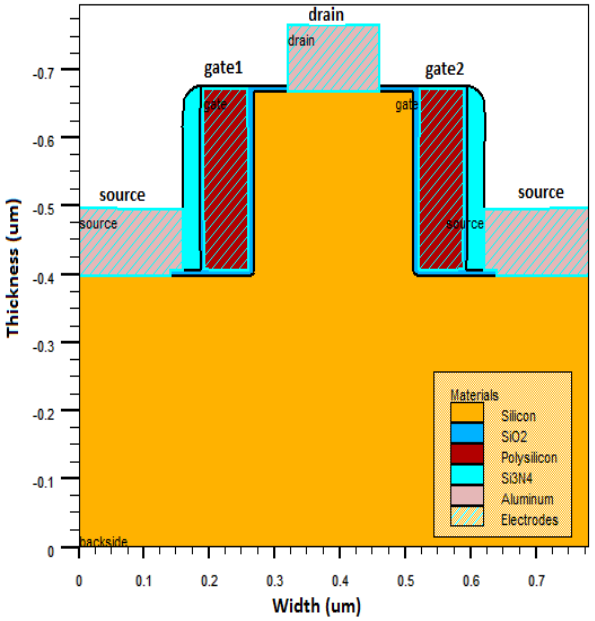


Fig. 1 Structure of Vertical DG-MOSFET device

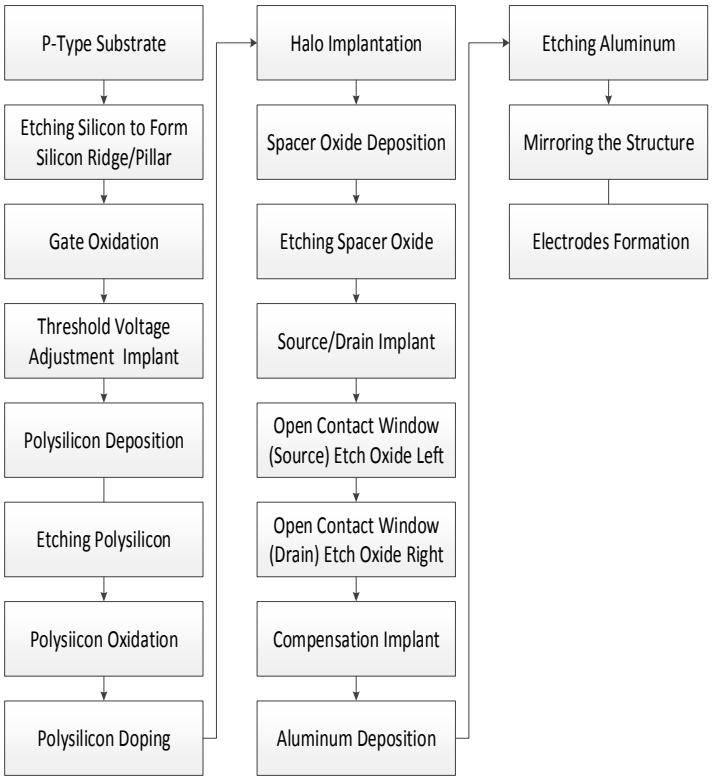


Fig. 2 Vertical DG-MOSFET's Process Simulation Flowchart

B. Device Simulation

Numerical simulation is a very useful method in investigating the physical nature of a vertical DG-MOSFET device [9]. By utilizing ATLAS, the electrical characteristics of a transistor can be determined precisely. Simulation results presented in this study were retrieved using SILVACO TCAD software, ATHENA and ATLAS module.

The initial point for the simulation is a structure represented

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in Fig. 1. The essential input process parameters that have been used in the structure of vertical DG-MOSFET device were substrate implant dose, halo implant tilt angle, gate-oxide diffusion temperature, threshold voltage (V_{TH}) implantation dose, V_{TH} implantation energy, halo implantation dose, halo implantation energy, source/drain (S/D) implantation dose, S/D implantation energy, compensation implantation dose and compensation implantation energy. The amount of input process parameters used in this design was summarized in Table I.

TABLE I
INPUT PROCESS PARAMETERS OF VERTICAL DG-MOSFET DEVICE

Process Parameters	Units	Level
Gate Oxidation Temperature	C^o	930
V_{TH} Implant Dose	atom cm^{-3}	9.55E12
V_{TH} Implant Energy	kev	10
V_{TH} Implant Tilt	degree	7
Pocket-Halo Implant Dose	atom cm^{-3}	1.17E13
Pocket-Halo Implant Energy	kev	170
Pocket-Halo Implant Tilt	degree	24
S/D Implant Dose	atom cm^{-3}	1.25E18
S/D Implant Energy	kev	45
S/D Implant Tilt	degree	80
Compensate Implant Dose	atom cm^{-3}	2.51E12
Compensate Implant Energy	kev	63
Compensate Implant Tilt	degree	7

III. Results and Discussion

The output response's results of the experiment obtained by using ATHENA and ATLAS module were discussed. Later, the optimization in obtaining the minimum sub-threshold swing (SS) value of vertical DG-MOSFET device was done using **numerical** simulation approach.

A. Analysis of Vertical DG-MOSFET Device

Fig. 3 shows the doping concentration across the Vertical DG-MOSFET device. The figure also shows the concentration of silicon, silicon dioxide, polysilicon, silicon nitride and aluminum. Doping concentration is one of the important factors in the fabrication process. This decides the electrical characterization of the MOSFET [10]. A good doping concentration will ensure the transistor works well with excellent gate control and fewer leakage currents.

Fig. 4 shows the graph of sub-threshold drain current (I_d) versus gate voltage (V_G) at drain voltage V_D = 0.05 V and voltage V_D = 1.0 V for Vertical DG-MOSFET device. The value of the off-leakage current (I_{OFF}) and drive current (I_{ON}) can be extracted from the graph.

The initial threshold voltage (V_{TH}) value of this result was at 0.892V and the SS value was at 118.2mV/dec. The initial value of sub-threshold swing (SS) was observed to be quite high. This may significantly affect the switching speed of the vertical DG-MOSFET device. In the next section, several numerical simulations were done in order to obtain the possible minimum value of sub-threshold swing (SS).

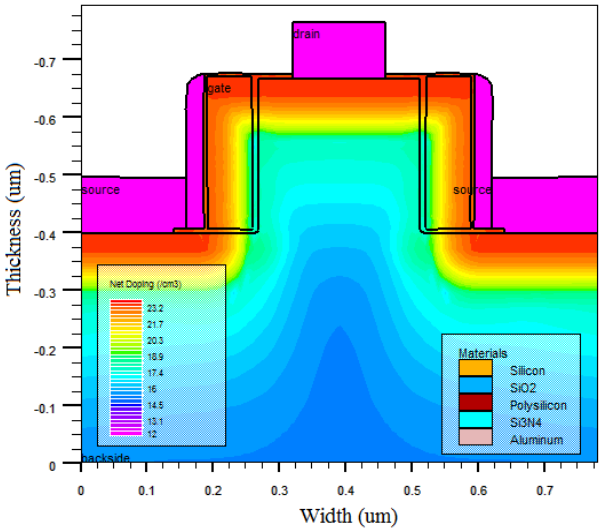


Fig. 3 Contour Mode of Vertical DG-MOSFET device

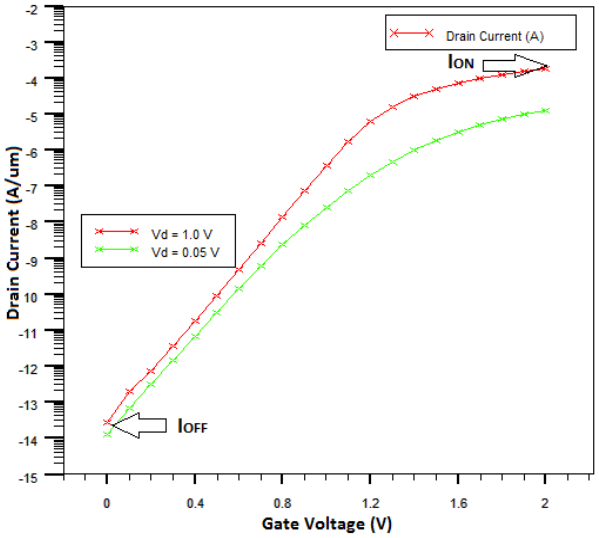


Fig. 4 Subs-Threshold I_D-V_{GS} curve for Vertical DG-MOSFET device

B. Numerical Simulation by Varying the Height of the Vertical DG-MOSFET Pillar

Several simulations were done in order to investigate the impact of silicon pillar's height towards the value of sub-threshold swing (SS). The value of input process parameters such as gate-oxide diffusion temperature, threshold voltage (V_{TH}) implant dose, V_{TH} implant energy, halo implant dose, halo implant energy, source/drain (S/D) implant dose and etc. were fixed as initial values. The observation was only focused on varying the structural parameter which is the height of the silicon pillar depicted in Fig. 5. Eight set of experiments were run and the results are shown in Table II. It was observed that the pillar's height variation had contributed a very random and large effect on the value of SS as illustrated in Fig. 6. However, there were no significant changes in the values of V_{TH}. They were observed to be nearly constant as depicted in

Fig. 6. The range of threshold voltage (V_{TH}) values were observed to be between 0.876V and 1.101V.

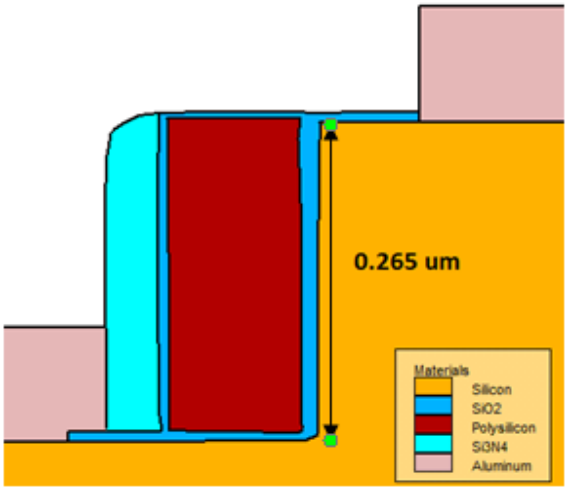


Fig. 5 The height of Vertical DG-MOSFET's Pillar

It was predicted that the values of SS were being affected by other input process parameters. From Table II, it was observed that the minimum value of SS was at 64.7mV/dec with V_{TH} value of 0.895V. Therefore, the suitable height of the **pillar** for vertical DG-MOSFET was found to be at 0.265 µm. Any applied height higher than 0.285 µm will damage the structure of the device. Hence, they were not suitable to be applied for the particular mesh grid definition of the device structure. The comparison value of SS with other researchers is as recorded in Table III [11], [12].

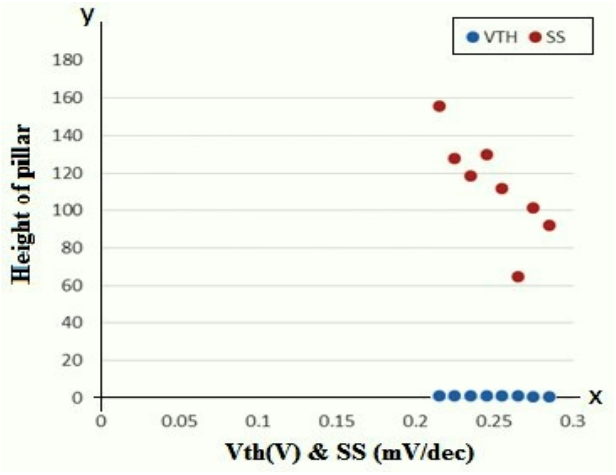


Fig. 6 X-Y Scatter graph for V_{TH} and SS value vs Height of the Pillar

TABLE II
EXPERIMENT RESULTS FOR DIFFERENT HEIGHT OF VERTICAL DG-MOSFET'S PILLAR

Sample of Experiment	Height of the Pillar (µm)	V_{TH} (V)	SS (mV/Dec)
1	0.215	1.011	155.9
2	0.225	0.946	127.6
3	0.235	0.892	118.2
4	0.245	1.101	129.6
5	0.255	0.966	111.8
6	0.265	0.895	64.7
7	0.275	0.876	101.5
8	0.285	0.877	91.9

TABLE III
COMPARISON RESULTS OF SUB-THRESHOLD SWING (SS) VALUE IN VERTICAL DG-MOSFET

Result from this work			Result from other Researcher 1 [11]	Result from other Researcher 2 [12]
Exp. No.	**Height of the Pillar (µm)**	**SS (mV/Dec)**	**SS (mV/Dec)**	**SS (mV/Dec)**
6	0.265	64.7	83	70-80

IV. CONCLUSION

In conclusion, the minimum value of sub-threshold swing (SS) in the vertical DG-MOSFET device was successfully obtained and predicted using SILVACO TCAD's simulation software. There are many physical limitations involved as the pillar gets higher, exceeding the molecular or atomic limitations of the substrate and dopant. Sub-threshold swing (SS) is the main response focused in this research as it is an important factor to decide whether the MOSFET possesses an excellent switch-off characteristic or not. High sub-threshold swing (SS) is to be avoided in order to obtain a higher switching speed response on/off or logic high/low transition. Numerical simulation was utilized by ATLAS module in determining the possible minimum SS value of the vertical DG-MOSFET device. From the observation made, it can be concluded that the minimum value of SS can be retrieved by varying the height of the silicon pillar. However, the retrieved SS values are observed to be random and non-linear due to the effect of input process parameters variation in the device. The minimum value of sub-threshold swing (SS) was found to be at 64.7mV/dec with threshold voltage (V_{TH}) of 0.895V. The ideal height of vertical DG-MOSFET pillar was found to be at 0.265 µm.

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