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Design and Analysis of a Low Power High Speed 1 Bit Full Adder Cell Based On TSPC Logic with Multi-Threshold CMOS

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***Abstract*—**An adder is one of the most integral component of a digital system like a digital signal processor or a microprocessor. Being an extremely computationally intensive part of a system, the optimization for speed and power consumption of the adder is of prime importance. In this paper we have designed a 1 bit full adder cell based on dynamic TSPC logic to achieve high speed operation. A high threshold voltage sleep transistor is used to reduce the static power dissipation in standby mode. The circuit is designed and simulated in TSPICE using TSMC 180nm CMOS process. Average power consumption, delay and power-delay product is measured which showed considerable improvement in performance over the existing full adder designs.

***Keywords*—**CMOS, TSPC, MTCMOS, ALU, Clock gating, power gating, pipelining.

I. Introduction

OVER the years significant progress has been made in optimizing digital systems in terms of power consumption, area and speed. Design tradeoffs often have to be made to balance these parameters to achieve optimum performance.

An adder is one of the most important components in digital systems like microprocessors and Digital Signal Processors. It is an integral part of the Arithmetic and Logic Unit (ALU) and Floating Point Unit (FPU) of a processor and also in address generation in case of cache or memory access. Hence, the speed and power consumption of the adder must be optimized for better performance.

In the first part of this paper we propose a 1 bit full adder cell designed in dynamic CMOS logic. We have used the True Single Phase Clock (TSPC) technique to achieve high speed operation over the conventional CMOS designs. Reduction of dynamic power consumption through clock gating technique is also discussed.

In the second part of the paper, the Multiple Threshold CMOS (MTCMOS) concept is used to reduce static power consumption of the adder. A high threshold voltage sleep transistor is used to reduce leakage current when the cell is in standby mode. The speed and power consumption of the adder is compared with other designs, which showed better performance of the proposed design.

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II. TSPC Based Full Adder Cell

A. TSPC Logic

The TSPC logic is a dynamic CMOS circuit technique. The dynamic logic is often considered a superior design technique as a logic function can be evaluated using only NMOS or PMOS transistors in contrast to using both in static CMOS logic [5]. Reduction in transistor count leads to reduction in silicon area and lower circuit delays.

Dynamic circuits are based on precharge and evaluate logic [9]. A PMOS transistor is used to precharge the load followed by evaluation of the logic function. It uses a clock signal, which, when '0', precharges the load, and when '1', evaluates the logic. NMOS and PMOS blocks can be cascaded to achieve pipelined operation. However, in domino and NORA logic two clock signals in opposite phases are required for the NMOS and PMOS blocks. This can create clock skew problems. Using TSPC logic alleviates the problem. It cascades NMOS and PMOS blocks interspaced with clocked CMOS latches.

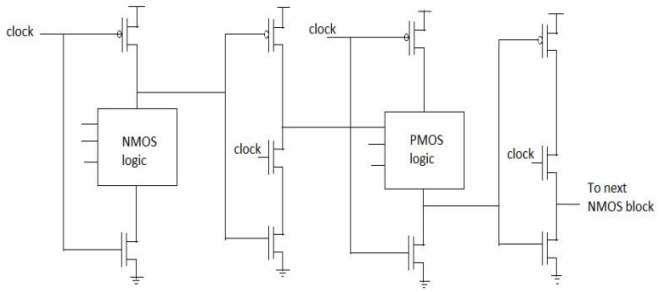


Fig. 1 A pipelined TSPC CMOS system

When the clock is zero, the NMOS block precharges the output node while the PMOS block evaluates. When the clock is one, opposite happens. The latches help preserve the previous output states.

B. 1 Bit Full Adder Cell Based On TSPC Logic

A low power TSPC Full Adder is proposed in [4] which require a total of 36 transistors for both N-type as well as P-type, of which are 6 clock transistors. In this paper we design a more compact full adder cell in the NMOS logic block using 21 transistors, which gives a reduction of 41.67% in silicon area. A corresponding PMOS block can similarly be designed and cascaded with the NMOS block to achieve pipelined

operation. The full adder cell has two parts: the sum and the carry. The truth table of the full adder is shown in Table I.

TABLE I
TRUTH TABLE OF FULL ADDER

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The carry is evaluated using a bridge configuration and the output is taken from a clocked CMOS latch. The intermediate inverted output is fed to the Sum block. The sum output is also taken from a clocked CMOS latch. When the clock signal is zero, both the output of the NMOS and PMOS blocks are precharged by V_{dd}. During this time the latch outputs store the previous values. When clock goes one, both the carry and the sum block evaluate and the latches become transparent. The latches give the correct inverted output after evaluation. The designed circuit is shown in Fig. 2.

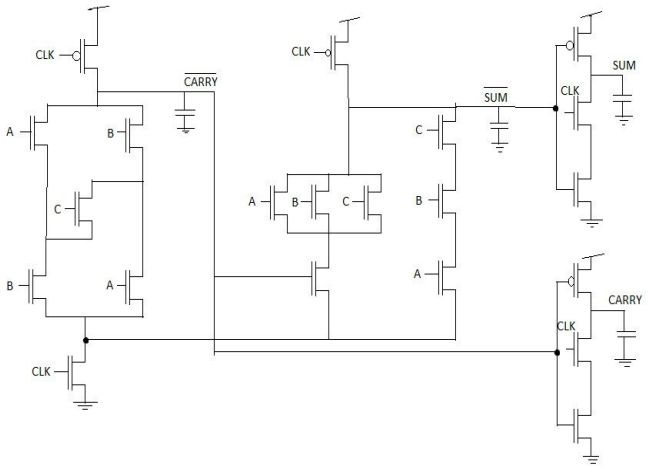


Fig. 2 TSPC full adder circuit

The performance of this adder circuit is compared with several standard full adder cells [1]. In [3] a compact 8 transistor adder is proposed which utilizes a 3 transistor XOR gate. However, the design suffers from a logic fault in carry output for a particular state. Our proposed adder contains 21 transistors of which are 5 clock transistors. The conventional static CMOS full adder cell has 28 transistors and consumes significant power and has considerable delay. Among the other works compared with, is the Static-Energy Recovery Full Adder (SERF) which requires 10 transistors. It does not contain a direct path to the ground and can re-apply the load charge to the control gate (energy recovery), thus consuming very low power. Another design denoted CLRCL (complementary and level restoring carry logic), features a lower operating voltage, higher computing speed, and lower energy operation and also has 10 transistors. An 8 transistor full adder cell is also compared with, which is based on multiplexer logic. The circuit suffers from threshold voltage drop at the output which is solved to some extent by choosing appropriate W/L ratios for the NMOS and PMOS respectively.

C. Simulation and Results

The circuit is simulated in TSPICE using TSMC 180nm process. The output load is taken as 100fF for both sum and carry. The simulation is done at 1.8V and 200 MHz. The circuit has a latency of 2.5ns, during which the output nodes precharges through the PMOS pull-up transistors. The simulated output is shown in Fig. 3.

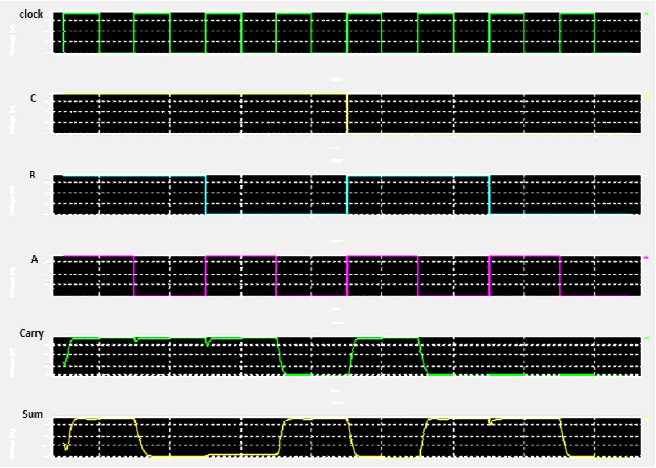


Fig. 3 Simulated output waveform of the TSPC full adder

TABLE II
AVERAGE POWER CONSUMPTION OF THE TSPC FULL ADDER AND PREVIOUS WORKS

Full adder cell	Average power consumption(μW)
28T static CMOS	104.40
SERF	84.30
CLRCL	78.18
TSPC full adder	78.13
8T full adder	67.63

TABLE III
DELAY COMPARISON OF THE TSPC FULL ADDER AND PREVIOUS WORKS

Full Adder Cell	Delay(ns)
SERF	0.765
CLRCL	0.642
8T	0.496
28T static CMOS	0.366
TSPC full adder	0.349

The average power consumption of other full adders is compared with our proposed design in Table II. The delay parameter is calculated from the time the clock signal reaches 50% of the supply voltage level to the time the output reaches the same voltage. The longest delay in all input combinations is the worst case delay and is enumerated in Table III for each design. We can see that TSPC adder is much faster than the SERF adder and also consumes lesser power. However,

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compared to the 8T adder, it has higher power consumption. This is due to large clock loads and high signal transition activities during the precharge mechanism [6].

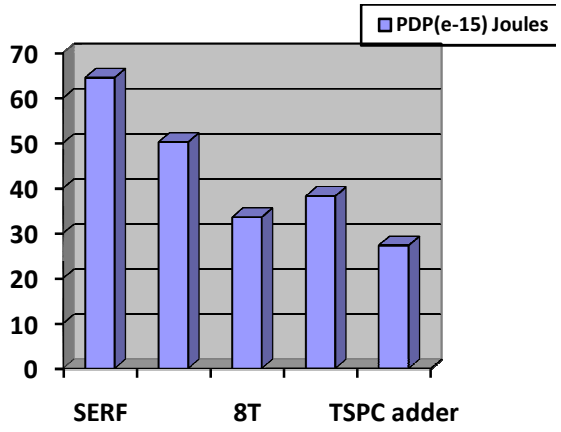


Fig. 4 Comparison of power-delay product among different adder cells

The power-delay product of our proposed adder is compared with other adders in Fig. 4. From the analysis we can see that the TSPC based full adder has the lowest power-delay product and hence superior performance. However, this comes at the price of higher silicon area due to 21 transistors compared to SERF, CLRCL and 8T adder cells.

III. Using MTCMOS Technique on the TSPC Full Adder

As we scale down to sub-micron technologies, the value of leakage current is increased, as some of the SPICE parameters like gate length, oxide thickness and threshold voltage is changed [7]. Thus, efficient methods to reduce leakage power consumption are necessary. An advantage of the TSPC full adder is that it provides natural clock gating feature. Using clock gating, the adder can be temporarily suspended from operation when not needed. This just requires turning off theclock signal. Thus, unnecessary clocking of transistors is prevented, leading to lower dynamic power consumption. However, this method, does not address the static power consumption of the circuit, which is greatly contributed by the sub-threshold leakage current.

MTCMOS technique involves using a high threshold voltage sleep transistor connected to the ground rails or the power rails [2]. The lower V_t transistors are used to design the actual circuit while the high V_t sleep transistors form an interface for the circuit with the ground and power rails. The current flowing through the sleep transistor can be expressed as [10],

$$I_{sleep} = 0.05\mu_n C_{ox}(W/L)(V_{dd} - V_{tL})(V_{dd} - V_{tH}) \quad (1)$$

V_{tL} indicates the threshold voltage of the transistors used to design the main circuit. V_{tH} indicates the threshold voltage of the sleep transistor. $V_{tL}$is kept low to achieve high speed operation of the circuit in normal mode of operation. V_{tH} is kept high as it decreases the current through the sleep transistor during standby mode. The (W/L) ratio indicates the size of the sleep transistor. Equation (1) assumes the circuit can tolerate 5% degradation in delay performance with the presence of the sleep transistor.

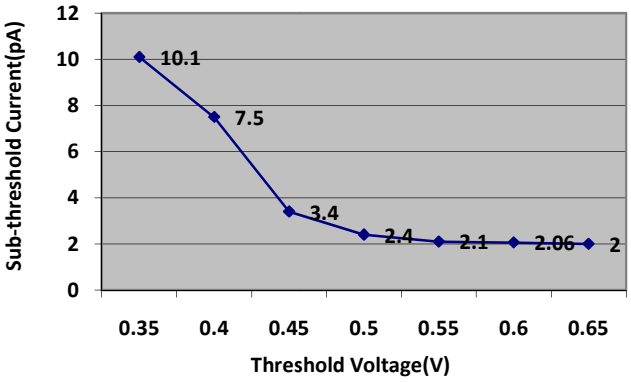


Fig. 5 Variation of Sub-Threshold Current with Threshold Voltage

The change in sub-threshold current with threshold voltage for an NMOS transistor in TSMC 180nm technology process is shown in Fig. 5. We can see that, with increase in threshold voltage, the sub-threshold current decreases [8]. During normal mode of operation, sleep transistors are kept on, thus connecting the main circuit with supply and ground. During standby mode of operation, the sleep transistors are turned off, thus isolating the main circuit from the supply and ground, thus no current is drawn from the supply to the ground which leads to lower static power consumption. Low V_t transistors are needed for high speed operation, however they have significant sub-threshold current conduction. To reduce sub-threshold conduction, which is a major component of leakage power, high V_t sleep transistors are used.

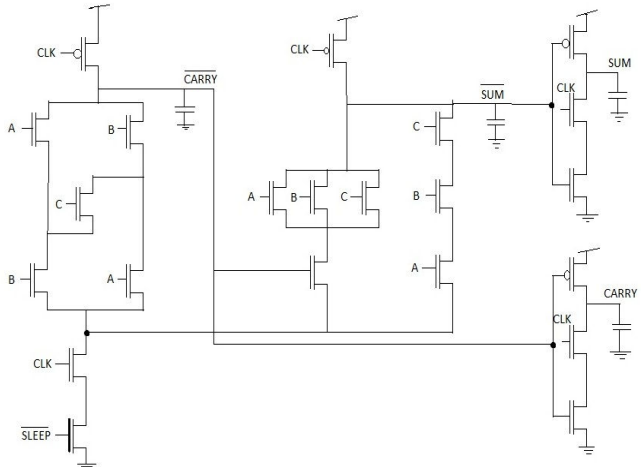


Fig. 6 TSPC based adder with high V_T sleep transistor connected to ground

In this circuit the high V_t sleep transistor is connected to the ground rail. When the input of the transistor is '1', the circuit

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operates in normal mode. When the input is '0', the circuit is cutoff from the ground rail and operates in standby mode.Since there is no direct path between supply and ground, this reduces the sub-threshold leakage current and lowers the static power consumption in standby mode. During this time the clock signal goes from '0' to '1' and remains high in evaluate state. A conventional precharge cycle is used to switch from the standby mode back to the normal mode of operation.

TABLE IV
COMPARISON OF STATIC POWER CONSUMPTION WITH AND WITHOUT SLEEP TRANSISTOR

TSPC adder cell	Static power consumption(μW)
Without sleep transistor	28.80
With sleep transistor(normal mode)	27.45
With sleep transistor(standby mode)	1.034

Table IV shows us the static power consumption of the TSPC based adder with and without sleep transistor as well as in standby mode when the sleep transistor in off state. We can see that by using the high V_t sleep transistor, the static power dissipation is reduced by 96.4% during the standby mode, over the circuit which does not employ sleep transistor. The average power consumption during active mode is also reduced to 75.73μW. However, adding an extra sleep transistor slightly increases the capacitance which in turn increases the delay to 0.370ns during normal mode of operation [6].

IV. PERFORMANCE

The proposed adder can operate at a minimum voltage of 0.95V at 200Mhz with a 30fF load. The width of NMOS transistors is taken as 0.9um and of PMOS transistors 1.8um. The width of the sleep transistor is taken as 4um. The adder cell can also be designed for a PMOS block and cascaded with the NMOS block for a pipelined operation with higher throughput. The NMOS block adder cell uses only one PMOS transistor for precharge and all NMOS transistors are used as a pull down network. NMOS transistors have a lower on-resistance, occupy lesser area and are consequently faster than the PMOS pull-up network.

V. CONCLUSION

A dynamic full adder cell based on TSPC logic has been designed and the power and delay of the cell has been compared with existing full adder cells which showed its superior performance over the other full adders, in terms of power consumption and delay. The adder is then modified to achieve minimum static power consumption using MTCMOS technique. The average power consumption of the cell in normal mode of operation has been found to be 75.73μW and delay of 0.370ns. The power consumption is significantly reduced to 1.034μW during standby mode of operation. The proposed adder can operate at low voltages and achieve good speeds.

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