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Explicit Delay and Power Estimation Method for CMOS Inverter Driving on-Chip RLC Interconnect Load

Susmita Sahoo, Madhumanti Datta, and Rajib Kar

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***Abstract*—**The resistive-inductive-capacitive behavior of long interconnects which are driven by CMOS gates are presented in this paper. The analysis is based on the π-model of a RLC load and is developed for submicron devices. Accurate and analytical expressions for the output load voltage, the propagation delay and the short circuit power dissipation have been proposed after solving a system of differential equations which accurately describe the behavior of the circuit. The effect of coupling capacitance between input and output and the short circuit current on these performance parameters are also incorporated in the proposed model. The estimated proposed delay and short circuit power dissipation are in very good agreement with the SPICE simulation with average relative error less than 6%.

***Keywords*—**Delay, Inverter, Short Circuit Power, π-Model, RLC Interconnect, VLSI

I. Introduction

AS the minimum feature size for integrated circuits is scaled downwards, the resistive component of the interconnect load become comparable to the gate output impedance and a single lumped capacitor is no longer a valid gate load model. In order to incorporate the increased role of the resistance and to determine the load behavior and consequently the propagation delay of the driving CMOS gates, accurate equivalent load models have to be used. A model expression for CMOS inverter driving capacitive load was first introduced by Burns [1] and Hedenstierna and Jeppson et. al. extended the work to include input waveform slope effect [2]. Since both these works are based on the Shockley model, extensive studies are required to model the circuit behavior in deep-submicron region. A simple yet realistic α-power MOSFET model [3] and n-power MOS model [4] are introduced which include the carrier velocity saturation effect and closed form expressions are derived for delay, short circuit power dissipation and transient voltage of CMOS inverter. But while deriving the output voltage expression for [3] [4], the short-circuit current, gate-drain coupling capacitance is neglected and output is derived only for fast ramp inputs.

Susmita Sahoo is with the Department of Electronics & Communication Engg., National Institute of Technology, Durgapur, West Bengal, 713029 (e-mail: susmitas1987@gmail.com).

Madhumanti Datta is with the Department of Electronics & Communication Engg., National Institute of Technology, Durgapur, West Bengal, 713029 (e-mail: madhumanti_datta@rediffmail.com)

Rajib Kar is with the Department of Electronics & Communication Engg., National Institute of Technology, Durgapur, West Bengal, 713029 (e-mail: rajibkarece@gmail.com)

The delay model proposed in [5] uses α-power MOS model and the short-circuit current has been considered. But the output voltage and current are assumed to be piece-wise linear which leads to inaccuracy of this model. An accurate and analytical delay model for CMOS driver driving capacitive load is derived in [6] for all regions of ramp input which overcomes all the above mentioned weaknesses. Explicit expressions for the propagation delay of CMOS gates driving RC load have been derived in [7]-[9]. But these models present significantly large error due to the fact that they are based on the simplified assumptions for the transistor operation and use simple models for the representation of the interconnect loads. A model for delay calculation of CMOS inverter driving CRC π-load has been presented in [10]. This method pre-characterizes an equivalent resistance for each gate and formulates a two-dimensional look up table for the waveform of a voltage source which drives the resistance. This technique, however, requires re-characterization if the operating conditions viz, supply voltage and temperature range are changed. In [11], an analytical method with an emphasis on the circuit power dissipation has been proposed for the CMOS inverter driving a CRC π load which requires less characterization effort and less computational time by replacing each gate to a simple inverter circuit and calculates the gate delay by analytical method. In order to find analytical expressions for the propagation delay and the output waveform shape, an interconnect load may be modeled in different ways [12].

A model for the estimation of propagation delay of a CMOS inverter driving a load, modeled by a resistor in series with a capacitor is derived in [7]. However, the driving transistor has been considered to operate always in linear mode, the influence of short circuit current is also ignored and the simplified case of step input has been examined, thus sacrificing accuracy.

In order to replace the RC load, an effective capacitance is calculated by an iteration procedure based on simplified assumptions in the shape of the output response [8]. The real output waveform has been approximated by the charging / discharging of the effective capacitance, until the time instant where the output voltage becomes equal to $V_{DD}/2$. Capturing the remaining portion of the output response is achieved by a simple resistive model.

A time varying Thevenin equivalent model has been proposed in [9] for the estimation of the gate delays. The gate is replaced by an equivalent circuit model composed of a

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linear voltage source and a linear resistor, where their values are determined by using the same empirical factors and thus reducing the accuracy, especially for submicron technologies. A good approximation for an RC interconnect load is obtained with the π model, achieving an error as low as 3% in delay calculations [12]. Analytical expressions for the propagation delay and the output waveform can be obtained once the load is replaced by its π equivalent and the corresponding system equations are solved. This method is extended in [13], where a CMOS inverter driving RC interconnect load is considered and propagation delay and short circuit power dissipation is estimated with an error of less than 4%.With the increase in signal frequency and decrease in the transistor sizes, the importance of interconnects have become a dominant factor in determining the circuit performance in deep submicron technology. At low frequencies, the interconnect lines can be modeled either as lumped or distributed RC circuit model. But in today's deep submicron technology, as the signal frequency is rapidly increasing, one can't ignore the effects of the on-chip inductance. A multi-ramp model with general RLC interconnects as a load is proposed in [14] which accurately predict both the 50% delay and the overall output waveform. In [15], an effective capacitance of a distributed *RLC* load for estimating short-circuit power is presented for different transition time of ramp input, but it ignores the effect of fast ramp and slow ramp. In this paper, novel closed form formulae have been proposed for the estimation of the delay and the short circuit power dissipation for CMOS inverter driving the on-chip RLC interconnect for both fast ramp and slow ramp.

II. Transient Response Modeling

A circuit, composed of an inverter driving an RLC equivalent π-model, is considered where the gate-to-drain coupling capacitance, C_m, is also taken into account (Fig. 1). The α-power law model [1], which considers the velocity saturation effect of short channel devices, is used for the transistor current representation:

$$I_D = \begin{cases} 0 & V_{GS} \le V_{T0} \quad cutoff-region \\ k_l (V_{GS}-V_{T0})^{a/2} V_{DS} & V_{DS} < V_{D-SAT} \quad linear-region \\ k_s (V_{GS}-V_{T0})^{a} & V_{DS} \ge V_{D-SAT} \quad saturation-region \end{cases} \quad (1)$$

Where, $V_{D\text{-}SAT}$ is the drain saturation voltage [1], k_l, k_s are the trans-conductance parameters, α is the velocity saturation index and V_{T0} is the zero bias threshold voltage.

A rising ramp input with transition time τ is applied to the transistor gates. The case for a falling ramp is symmetrical. The differential equations that describe the operation of the circuit, as shown in Figure 1, in the loop of the π sub-circuit are obtained by Kirchoff's voltage law.

$$V_d = V_L + RC_L \frac{dV_L}{dt} + LC_L \frac{d^2V_L}{dt^2} \quad (2)$$

Kirchoff's current law in the transistors drain node can be expressed as,

$$i_n + i_d + i_L - i_m - i_p = 0$$

So,
$$\frac{dV_L}{dt} + C_2 \frac{d^2V_L}{dt^2} + C_3 \frac{d^3V_L}{dt^3} - C_4 \frac{dV_{in}}{dt} + \frac{i_n}{C_1} - \frac{i_p}{C_1} = 0 \quad (3)$$

Where,

$C_1 = C_d + C_m + C_L$,

$C_2 = \frac{RC_L(C_d + C_m)}{C_1}$, $C_3 = \frac{LC_L(C_d + C_m)}{C_1}$, $C_4 = \frac{C_m}{C_1}$

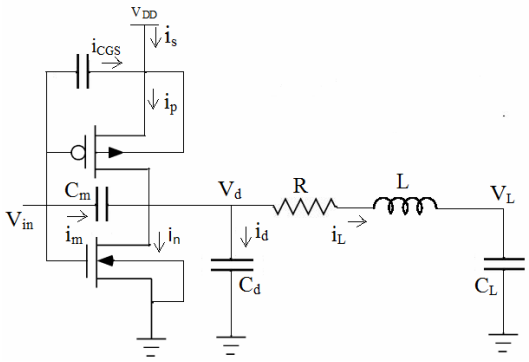


Fig. 1 CMOS Inverter Driving Equivalent π-Model of RLC Interconnect

In order to solve the differential equation (Eq. 3) analytically, the parasitic current through the PMOS transistor is initially considered to be negligible. The effect of the parasitic current component though PMOS transistor onto the output response will be determined towards the end of this section.Two typical cases for input ramps have been considered here:

(a) Fast Ramp (Time constant (RC_L or L/R) < τ)

(b) Slow Ramp (Time constant (RC_L or L/R) > τ).

For fast ramp input, the NMOS transistor is in saturation when the input reaches to its final value. For slow ramp input, the NMOS transistor is in linear region when the input reaches to its final value. In order to obtain the output voltage expression analytically, four different regions of operation are considered.

A. Fast Ramp Input

1) Region 1 ($0<t<t_1$)

The NMOS transistor is in cut-off region because $V_{in}<V_{T0}$ and hence, (3) becomes:

$$\frac{dV_L}{dt} + C_2 \frac{d^2V_L}{dt^2} + C_3 \frac{d^3V_L}{dt^3} - C_5 = 0 \quad (4)$$

with the initial conditions $V_L(0) = V_{DD}$, $\frac{dV_L}{dt}(0) = 0$ and $C_5 = C_4 \frac{V_{DD}}{\tau}$. The output waveform expression can be given as,

$$V_L(t) = V_{DD} + C_5 t - C_5 C_2 + \frac{C_5}{\xi_1 + \xi_2}\left(\frac{1}{\xi_1^2} e^{-\xi_1 t} + \frac{1}{\xi_2^2} e^{-\xi_2 t}\right) \quad (5)$$

Where $\xi_1, \xi_2 = \frac{-C_2 \pm \sqrt{(C_2^2 - 4C_3)}}{2C_3}$

This expression describes the small overshoot of the output

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waveform due to the coupling capacitance C_m. Generally for the case of driving long interconnection lines the overshoot value is almost negligible since $C_m<<C_d$, and V_{out} can be considered to be equal to V_{DD} without significant error in this region. This region extends to the time instant $t_1 = \frac{V_{T0}\tau}{V_{DD}}$, where $V_{in} = V_{T0}$.

2) Region 2 ($t_1<t<\tau$)

The NMOS device operates in saturation and the input signal is still in saturation. Equation (3) becomes:

$$\frac{dV_L}{dt} + C_2\frac{d^2V_L}{dt^2} + C_3\frac{d^3V_L}{dt^3} - C_4\frac{dV_{in}}{dt} + \frac{K_s}{C_1}\left(\frac{V_{DD}}{\tau}t - V_{T0}\right)^a = 0 \quad (6)$$

This cannot be solved analytically. In order to obtain an analytical expression for the output in this region, the current component is approximated by a second order Taylor series with sufficient accuracy at $t=\tau/2$, where, $V_{in}=V_{DD}/2$ and given as,

$$\frac{i_n}{C_1} = A_0 + A_1 t + A_2 t^2$$

The differential equation can be solved which results the following expression for the output waveform:

$$V_L(t) = \varsigma_1 + \varsigma_2 t + \varsigma_3 t^2 + \varsigma_4 t^3 + \varsigma_5 e^{-\xi_3 t} + \varsigma_6 e^{-\xi_4 t} \quad (7)$$

Where,

$$\varsigma_1 = -A_1 + 2A_2C_2,$$

$$\varsigma_2 = -2A_0^{'} + 4A_2C_3 + 2A_1C_2 - 4A_2C_2^2,$$

$$\varsigma_3 = -2A_0^{'}C_2 + 6A_1C_3 - 24\varsigma_2C_2 + 2A_1C_2^2 - 4A_2C_2^3 - 8A_2C_2C_3,$$

$$\varsigma_4 = -8A_0^{'}C_2^2 + 8A_0^{'}C_3 + 4A_1C_2 + 16A_1C_2C_3 - 8A_2C_2^2 - 8A_2C_2^2C_3 - 16A_2C_3^2 - 8!C_2\varsigma_3 - 24\varsigma_2\left(6!C_2^2 + 2C_3\right),$$

$$\varsigma_5 = \frac{-A_0^{'}\xi_3^2 - A_1\xi_3 - 2A_2}{\xi_3^2\left(\xi_3 + \xi_4\right)},$$

$$\varsigma_6 = \frac{-A_0^{'}\xi_4^2 - A_1\xi_4 - 2A_2}{\xi_4^2\left(\xi_3 + \xi_4\right)},$$

$$A_0^{'} = \left(A_0 - \frac{C_4V_{DD}}{\tau}\right) and$$

$$\xi_{3,4} = \frac{-C_2 \pm \sqrt{\left(C_2^2 - 4C_3\right)}}{2C_3}$$

3) Region 3 ($\tau<t<t_2$)

The input has reached to its final value and the NMOS transistor is still in saturation. Equation (3) becomes:

$$\frac{dV_L}{dt} + C_2\frac{d^2V_L}{dt^2} + C_3\frac{d^3V_L}{dt^3} + \frac{K_s}{C_1}\left(V_{DD} - V_{T0}\right)^a = 0 \quad (8)$$

So, the output waveform can be calculated as,

$$V_L(t) = K_1C_1 - K_1t + \varsigma_7\left(\frac{1}{\xi_5^2}e^{-\xi_5 t} + \frac{1}{\xi_6^2}e^{-\xi_6 t}\right) \quad (9)$$

Where,

$$K_1 = \frac{K_s}{C_1}\left(V_{DD} - V_{T0}\right)^a,$$

$$\varsigma_7 = \frac{-K_1}{\left(\xi_5 + \xi_6\right)}$$

This region extends until the time instant t_2, when the NMOS transistor exits saturation. The time instant t_2 is calculated by (10).

$$V_d(t_2) = V_{D-SATN}(t_2)$$
$$= V_L(t_2) + RC_L\frac{dV_L}{dt}(t_2) + LC_L\frac{d^2V_L}{dt^2}(t_2) \quad (10)$$

This can be solved without any approximation. V_{D-SATN} is the drain saturation voltage of the NMOS device.

4) Region 4 ($t>t_2$)

The NMOS transistor operates in linear mode and hence, (3) becomes:

$$\frac{dV_L}{dt} + C_2\frac{d^2VL}{dt^2} + C_3\frac{d^3V_L}{dt^3} + \frac{K_l}{C_1}\left(V_{DD} - V_{T0}\right)^{a/2}\left(V_L + RC_L\frac{dV_L}{dt} + LC_L\frac{d^2V_L}{dt^2}\right) = 0 \quad (11)$$

So, the output response can be modeled as,

$$V_L(t) = \varsigma_8 e^{-\xi_7 t} + \varsigma_9 e^{-\xi_8 t} + \varsigma_{10} e^{-\xi_9 t} \quad (12)$$

Where,

$$\xi_7 = \frac{-\chi_2}{3\chi_1} - \frac{K_4}{3\chi_1} - \frac{\chi_2^2 - 3\chi_1\chi_3}{3\chi_1K_4},$$

$$\xi_8 = \frac{-\chi_2}{3\chi_1} + \frac{K_4\left(1+i\sqrt{3}\right)}{6\chi_1} + \frac{\left(\chi_2^2 - 3\chi_1\chi_3\right)\left(1-i\sqrt{3}\right)}{6\chi_1K_4},$$

$$\xi_9 = \frac{-\chi_2}{3\chi_1} + \frac{K_4\left(1-i\sqrt{3}\right)}{6\chi_1} + \frac{\left(\chi_2^2 - 3\chi_1\chi_3\right)\left(1+i\sqrt{3}\right)}{6\chi_1K_4},$$

$$\chi_1 = C_3,$$

$$\chi_2 = C_2 + K_2LC_L,$$

$$\chi_3 = 1 + K_2RC_L,$$

$$K_3 = \sqrt{\left(2\chi_2^3 - 9\chi_1\chi_2\chi_3 + 27\chi_1^2K_2\right)^2 - 4\left(\chi_2^2 - 3\chi_1\chi_3\right)^3},$$

$$K_4 = \sqrt[3]{\frac{1}{2}\left(K_3 + 2\chi_2^3 - 9\chi_1\chi_2\chi_3 + 27\chi_1^2K_2\right)},$$

$$\varsigma_8 = \frac{1}{\left(\xi_7 + \xi_8\right)\left(\xi_7 + \xi_9\right)},$$

$$\varsigma_9 = \frac{1}{\left(\xi_7 + \xi_8\right)\left(\xi_8 + \xi_9\right)}$$

$$and\,\varsigma_{10} = \frac{1}{\left(\xi_7 + \xi_9\right)\left(\xi_8 + \xi_9\right)}$$

B. Slow Ramp Input

The operating conditions of the structure in region 1 and 2 are the same to that of fast inputs; however, region 2 extends from time t_1 to time t_2, where $t_2<\tau$.

1) Region 3 ($t_2<t<\tau$)

The NMOS transistor operates in linear mode while the input is still a ramp one. The differential equation describing the output response in this region can be modeled as:

$$\frac{dV_L}{dt}+C_2\frac{d^2V_L}{dt^2}+C_3\frac{d^3V_L}{dt^3}-C_5+ \frac{K_l}{C_1}(V_{in}-V_{T0})^{a/2}\left(V_L+RC_L\frac{dV_L}{dt}+LC_L\frac{d^2V_L}{dt^2}\right)=0 \quad (13)$$

This can not be solved analytically. For this reason, V_{in} is replaced by its average value $\tilde{V}_{in}=\frac{V_{in}(t_2)+V_{DD}}{2}$. This is a valid approximation, since for most of the practical cases, the duration of this region is very small and thus V_{in} takes values very close to that of average value.

Hence, the solution of (13) can be written as,

$$V_L(t)=\frac{C_5}{K_5}+\varsigma_{11}e^{-\xi_{10}t}+\varsigma_{12}e^{-\xi_{11}t}+\varsigma_{13}e^{-\xi_{12}t} \quad (14)$$

Where,

$$K_5=\frac{K_l}{C_1}\left(\tilde{V}_{in}-V_{T0}\right)^{a/2},$$

$$\xi_{10}=\frac{-\rho_2}{3\rho_1}-\frac{K_7}{3\rho_1}-\frac{{\rho_2}^2-3\rho_1\rho_3}{3\rho_1K_7},$$

$$\xi_{11}=\frac{-\rho_2}{3\rho_1}+\frac{K_7\left(1+i\sqrt{3}\right)}{6\rho_1}+\frac{\left({\rho_2}^2-3\rho_1\rho_3\right)\left(1-i\sqrt{3}\right)}{6\rho_1K_7},$$

$$\xi_{12}=\frac{-\rho_2}{3\rho_1}+\frac{K_7\left(1-i\sqrt{3}\right)}{6\rho_1}+\frac{\left({\rho_2}^2-3\rho_1\rho_3\right)\left(1+i\sqrt{3}\right)}{6\rho_1K_7},$$

$$\rho_1=C_3,$$

$$\rho_2=C_2+K_5LC_L,$$

$$\rho_3=1+K_5RC_L,$$

$$K_6=\sqrt{\left(2{\rho_2}^3-9\rho_1\rho_2\rho_3+27{\rho_1}^2K_5\right)^2-4\left({\rho_2}^2-3\rho_1\rho_3\right)^3},$$

$$K_7=\sqrt[3]{\frac{1}{2}\left(K_6+2{\rho_2}^3-9\rho_1\rho_2\rho_3+27{\rho_1}^2K_5\right)},$$

$$\varsigma_{11}=\frac{1}{(\xi_8+\xi_9)(\xi_8+\xi_{10})},$$

$$\varsigma_{12}=\frac{1}{(\xi_8+\xi_9)(\xi_9+\xi_{10})},$$

$$and\,\varsigma_{13}=\frac{1}{(\xi_8+\xi_{10})(\xi_9+\xi_{10})}$$

Region 4 can be solved in a similar manner as discussed for the case of the fast input.

III. Effect of Short Circuit Current on Propagation Delay

In the previous section, the current through the PMOS transistor, called short circuit current, has been considered to be negligible. Generally, this is a valid assumption because the capacitive and inductive load in long interconnection line is large enough so that the output voltage doesn't change significantly until the time the PMOS transistor becomes off. This signifies that the drain-to-source voltage of the PMOS transistor remains small and its current component also takes small values. Consequently, in order to simplify the mathematical analysis, the short circuit current is ignored and it does not have any significant effect on the accuracy of the analysis which has already been presented. In this section, the effect of the short circuit current on the estimation of the propagation delay of gates driving long interconnections is discussed.

The short-circuit current through the PMOS transistor exists in the interval (t_{ov}, t_p); where t_{ov} is the time where the voltage overshoot at the output of the inverter ceases. That is due to the fact that during the voltage overshoot, the PMOS current is flowing towards V_{DD} and thus no current path exists between V_{DD} and ground. Time t_{ov} can be calculated by setting the voltage expression for the inverter output, V_d in region 2 equal to V_{DD}. t_p is the time when the PMOS transistor turns off (when $V_{in}=V_{DD}-|V_{TP}|$). The existence of the PMOS current results in a decrease of the discharging current and thus an increase in the propagation delay. It acts like an amount of charge Q_e initially stored in the output node and which has to be removed through the NMOS transistor. Consequently, the equivalent charge can be calculated by integrating the current of the PMOS device over an interval of t_{ov} to t_p. Considering that the PMOS transistor operates for half of the interval (t_{ov}, t_p) in linear mode and that the current waveform is symmetrical around the middle of this interval [6], Q_e can be calculated as:

$$Q_e=\int_{t_{ov}}^{t_p} i_p\,dt=2\int_{t_{ov}}^{\frac{t_{ov}+t_p}{2}} K_l\left(\frac{V_{DD}}{\tau}t-V_{TP}\right)^{\frac{a}{2}}|V_d-V_{DD}|dt \quad (15)$$

The PMOS drain-to-source voltage $|V_d-V_{DD}|$ derived in the previous section is used in this integral.

In this way, the increase in propagation delay is found as the time required to remove the equivalent charge Q_e. An average value for the discharging current, I_{dis}, should be used. However, it can be approximated by the NMOS transistor current at time $t_p/2$ as $I_{dis}=i_n|t_p/2|$, which can be derived from the previous analysis. Thus, the time required to remove this extra charge, t_{ad}, which causes the additional propagation delay can be calculated as, $t_{ad}=\frac{Q_e}{I_{dis}}$.

IV. Estimation of Short Circuit Power Dissipation

The short-circuit power which is dissipated during the output switching is due to the current i_s, can be found by applying Kirchoff's current law at the source of the PMOS transistor.

$$i_s=i_p-i_{C_{GS}} \quad (16)$$

Where, $i_{C_{GS}}$ is the current through the gate-to-source coupling capacitance and is given by, $i_{C_{GS}}=C_{GS}\frac{dV_{in}}{dt}$.

Energy starts to dissipates at time t_s, when i_s starts flowing towards the source of the PMOS transistor. Time t_s can be calculated by setting i_s=0 using linear region expression for the PMOS current. The PMOS transistor starts its operation in linear mode and then enters into the saturation at

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approximately $t_{sat} = \frac{t_{ov} + t_p}{2}$ [6], where, i_p and consequently i_s reach their maximum value. Assuming that the PMOS current and consequently i_s is symmetrical around t_{sat}, the dissipated energy due to short-circuit current is given by,

$$E_{sc} = 2V_{DD} \int_{t_s}^{t_{sat}} i_s dt \tag{17}$$

So, the short circuit power dissipation for a symmetrical driver and for a system clock frequency f, can be calculated as,

$$P_{sc} = 2\alpha f E_{sc} \tag{18}$$

Where, α is the switching activity of the output node.

The logic stages following a large RLC load will dissipate significant amount of short-circuit power due to the degraded waveform which they receive as input. Connecting the 20% and 80% point of the output waveform, an effective ramp input for the following stages is obtained which can be used in the corresponding formula as given in (1) for the calculation of the short-circuit power dissipation in these stages.

V. Simulation Results and Discussions

A comparison of the output voltage response, V_L, calculated by using the proposed method as given by (5), (7), (9), (12), (14) with the SPICE result for both fast ramp and slow ramp input signal has been shown in Figure 2 for 0.18 μm technology; W_n=240nm and W_p=180nm. The average error for fast ramp is 4.874% with maximum error of 6.35% and minimum error of 1.98% and similarly the average error for slow ramp is 4.76% with maximum error of 6.13% and minimum error of 2.61%, which justifies the accuracy of the proposed model.

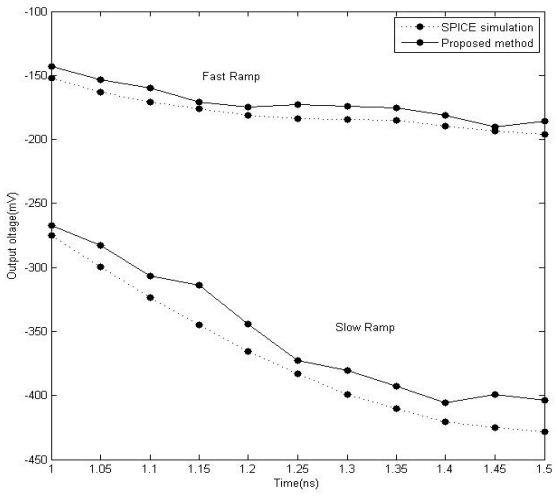


Fig. 2 Comparison of Output Waveform between Simulated and Calculated values for (a) Slow Ramp (τ=0.5ns, R=400Ω, L=300nH, C_d/C_L=1.5pF) and (b) Fast Ramp (τ=0.5ns, R=100Ω, L=50nH, C_d/C_L=5pF)

A. Delay Calculation

Since the output waveform expression for each of the regions of operation is known, propagation delay can be calculated as the time from the 50% of the rising /falling input to 50% of the rising/falling output waveform. Using this definition, the 50% propagation delay has been calculated for several R, L, C_L/C_d values. The variation of load capacitance with delay for different values of R and L are shown in Table 1 for both fast as well as for slow ramp signal. The variation of load inductance with propagation delay is presented in Table II for different values of load resistance and capacitance for both fast and slow ramps. Using the output voltage equations derived above, the proposed delay is calculated and has been compared with SPICE delay where the average relative error is within 6%.

The variations of delay with load capacitance for different values of R and L for both fast and slow ramps are graphically represented in Figure 3 and Figure 4, respectively. For fast ramp input, the average error is 5.013% with maximum error of 6.01% and minimum error of 4.12%, similarly for slow ramp, the average error is 4.67% with maximum error of 6.49% and minimum error of 1.98% have been achieved which show that the proposed delay model closely follows the SPICE delay.

The variations of delay with load inductance for different values of load resistance and capacitance for fast and slow ramps are graphically represented in Figure 5 and Figure 6, respectively. For fast ramp the average error is 4.93% with a maximum error of 5.81% and a minimum error of 4.31% have been achieved. Similarly for slow ramp, the average error is 3.88% with maximum error of 5.76% and minimum error of 1.98%, which shows that the proposed delay varies closely with SPICE delay. From the graphs it is evident that as the time constant of RLC load i.e. (RC_L or L/R) increases, the 50% delay also increases.

B. Short-Circuit Power Calculation

When the input voltage waveform deviates from the ideal step input and has nonzero rise and fall time, both NMOS and PMOS transistor will simultaneously conduct a certain amount of current during the switching event since both the transistors will form a conducting path between V_{DD} to ground. This is called short-circuit current. This short-circuit power dissipation will be negligible for high load inductance and capacitance value which is evident from Table 3 and Figure 7 and Figure 8. Comparisons between the short-circuit energy calculated by using the proposed method with SPICE for different values of C_L, R and L is shown in Table 3, and the average relative error is 4.797% with maximum error of 6.61% and a minimum error of 1.57%.

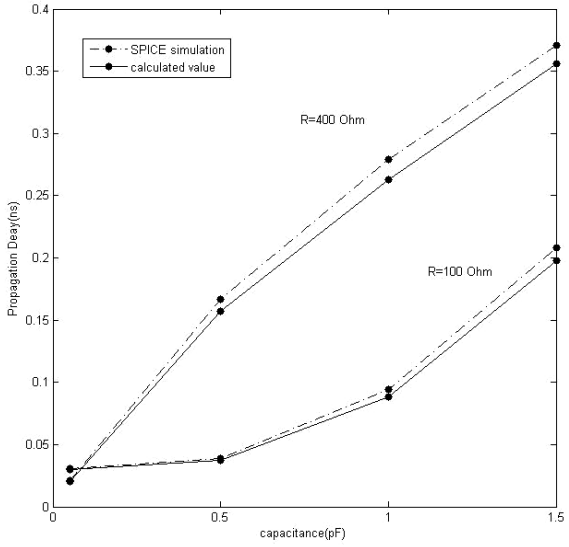


Fig. 3 Load Capacitance vs. Delay for Different Values of Load Resistance for Fast Ramp with *L*=50 nH

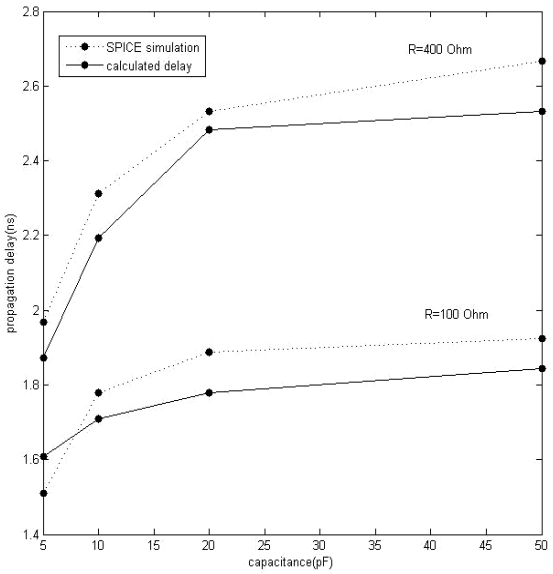


Fig. 4 Load Capacitance vs. Delay for Different Values of Load Resistance for Slow Ramp with L=200 nH

TABLE I
LOAD CAPACITANCE VS PROPAGATION DELAY FOR L=50 NH AND L=200 NH FOR FAST AND SLOW RAMP SIGNAL, RESPECTIVELY

Fast Ramp							Slow Ramp						
	Propagation Delay (ns)							Propagation Delay(ns)					
	R=100Ω			R=400Ω				R=100Ω			R=400Ω		
C_L (pF)	SPICE Result (ns)	Proposed Method (ns)	Error (%)	SPICE Result (ns)	Proposed Method (ns)	Error (%)	C_L (pF)	SPICE Result (ns)	Proposed Method (ns)	Error (%)	SPICE Result (ns)	Proposed Method (ns)	Error (%)
0.05	0.031	0.029	4.35	0.021	0.020	4.31	5	1.510	1.608	6.49	1.968	1.873	4.83
0.5	0.039	0.037	5.01	0.167	0.157	6.01	10	1.779	1.709	3.95	2.313	2.192	5.21
1.0	0.094	0.088	5.98	0.279	0.263	5.67	20	1.889	1.779	5.78	2.533	2.483	1.98
1.5	0.208	0.198	4.65	0.371	0.356	4.12	50	1.925	1.844	4.17	2.666	2.533	4.98

TABLE II
INDUCTANCE VS PROPAGATION DELAY FOR C_L/C_D=0.5 PF AND C_L/C_D=50 PF FOR FAST AND SLOW RAMPS RESPECTIVELY

Fast Ramp Propagation Delay(ns)							Slow Ramp Propagation Delay(ns)						
	R=100Ω			R=400Ω				R=100Ω			R=400Ω		
L (nH)	SPICE Result (ns)	Proposed Method (ns)	Error (%)	SPICE Result (ns)	Proposed Method (ns)	Error (%)	L (nH)	SPICE Result (ns)	Proposed Method (ns)	Error (%)	SPICE Result (ns)	Proposed Method (ns)	Error (%)
20	0.029	0.028	4.79	0.136	0.129	4.59	200	1.825	1.753	3.96	1.613	1.522	5.76
40	0.871	0.083	5.21	0.156	0.149	4.31	400	1.873	1.821	2.75	1.560	1.529	1.98
100	0.261	0.247	4.89	0.311	0.292	0.31	600	1.907	1.813	4.91	1.812	1.741	3.92

In Figure 7, the variation of energy with load capacitance for both the proposed method and SPICE for different values of R is shown which shows that with increase in capacitance value, the energy becomes negligible. In Figure 8, the variation of energy with load inductance for both the proposed method and SPICE for different values of R is shown which shows that with increase in inductance value, the energy becomes negligible.

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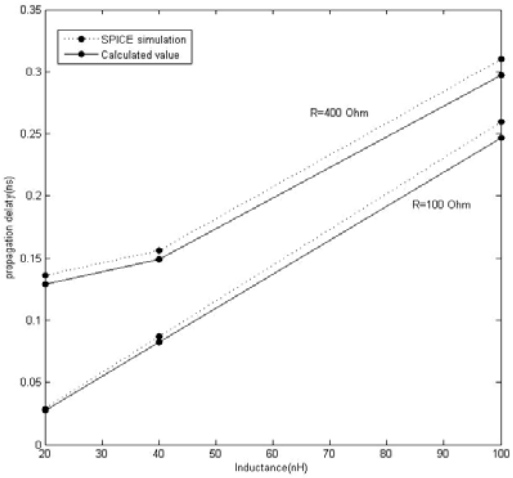


Fig. 5 Load Inductance vs. Delay for Different Values of Load Resistance for Fast Ramp with C_L=0.5 pF

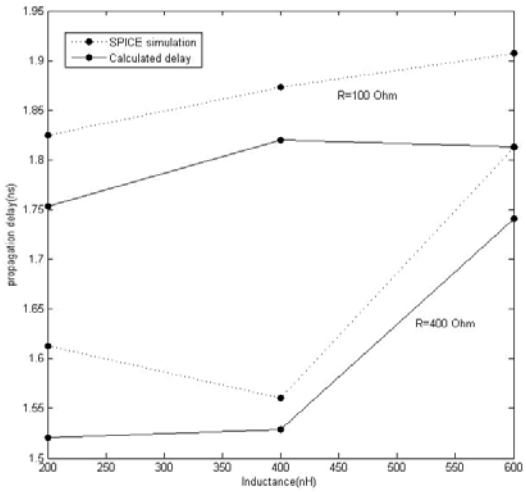


Fig. 6 Load Inductance vs. Delay for Different Values of Load Resistance for Slow Ramp with C_L=50 pF

TABLE III
VARIATION OF SHORT-CIRCUIT ENERGY WITH C_L/C_D AND L FOR DIFFERENT VALUES OF R

	Short-Circuit energy(fJ) for L=50 nH							Short-Circuit energy(fJ) for C_L/C_d=5 pF					
	R=100Ω			R=400Ω				R=100Ω			R=400Ω		
C_L (pF)	SPICE Result (fJ)	Proposed Method (fJ)	Error (%)	SPICE Result (fJ)	Proposed Method (fJ)	Error (%)	L (nH)	SPICE Result (fJ)	Proposed Method (fJ)	Error (%)	SPICE Result (fJ)	Proposed Method (fJ)	Error (%)
0.5	295.950	286.657	3.14	270.148	265.148	1.57	20	327.825	306.156	6.61	343.110	328.459	4.27
1.0	264.581	252.012	4.75	210.816	197.724	6.21	50	295.950	281.359	4.93	358.545	344.167	4.01
1.5	197.501	188.987	4.31	170.155	163.808	3.73	100	203.121	190.872	6.03	217.875	204.148	6.30
2.5	183.510	173.614	5.39	155.185	147.518	4.94	200	3.762	3.549	5.65	25.170	23.801	5.44
5.0	95.750	91.662	4.27	58.545	56.104	4.17	400	0.551	0.524	4.81	1.783	1.686	5.41

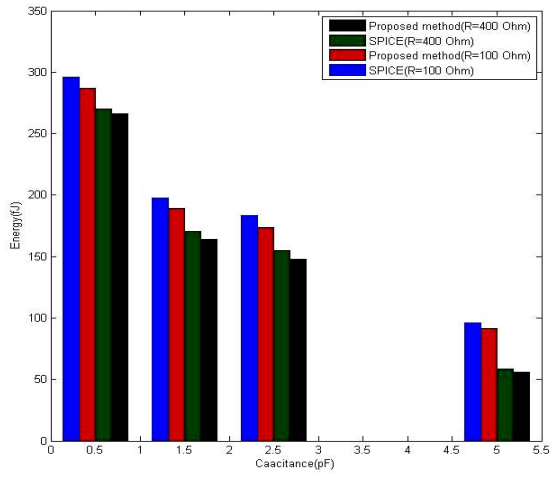


Fig. 7 Capacitance vs. Energy for Different Values of R for L=50nH

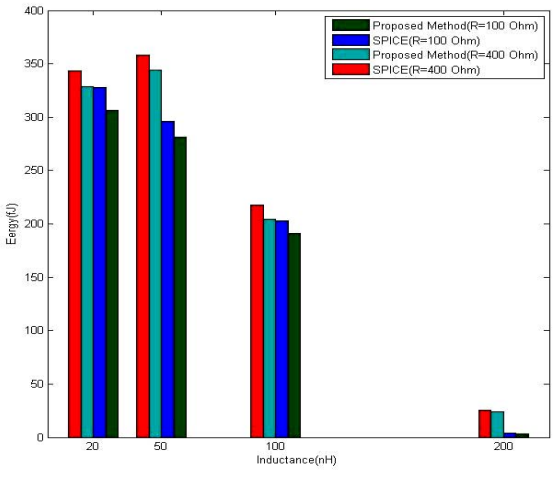


Fig. 8 Inductance vs. Energy for Different Values of R for C_L/C_d=5pF

VI. CONCLUSION

The 50% propagation delay and short-circuit power dissipation of a CMOS inverter driving a π-model RLC load is calculated by solving a set of differential equations. Accurate analytical solutions of these equations have been derived for different regions of operation of CMOS inverter for both fast ramp and slow ramp inputs. The 50% delay calculated by the proposed method has been compared with that of the SPICE result and the average error for fast ramp and slow ramp are found to be 4.97% and 4.275%,

respectively. Short circuit power dissipation calculated by the proposed method is compared with SPICE and the average error is found to be as low as 4.797%. Thus, it is evident that the proposed method can provide a new perspective on delay and short circuit power dissipation calculation of CMOS driver driving RLC interconnect with higher accuracy.

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