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A New Hardware Implementation of Manchester Line Decoder

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***Abstract*—** In this paper, we present a simple circuit for Manchester decoding and without using any complicated or programmable devices. This circuit can decode 90kbps of transmitted encoded data; however, greater than this transmission rate can be decoded if high speed devices were used. We also present a new method for extracting the embedded clock from Manchester data in order to use it for serial-to-parallel conversion. All of our experimental measurements have been done using simulation.

***Keywords*—**High threshold level, level segregation, low threshold level, smoothing circuit synchronization..

I. INTRODUCTION

THE transmission of data requires high degree of synchronization between the transmitter and receiver; in other words, the receiver has to work with the same clock as that of the transmitter in order to detect the transmitted data correctly. This is simply done by sending the data and clock streams into separate links. This technique is called asynchronous transmission and can only be applied for short transmission distances. Otherwise, both the transmitted data and clock will reach the receiver at different time leading to a failure when detecting the transmitted data. Another transmission technique, called synchronous transmission, allows long distance transmission capability by embedding the clock into the data in order to achieve only one link of transmission. One of those techniques is called Manchester encoding technique. This technique has several advantages among them are: simplicity, no DC component, synchronization and error detection capability. Most of the decoding circuits of this technique implements programmable devices, or Phase Locked Loop (PLL) devices. In this paper, we introduce a new simple technique for decoding Manchester data by just using simple devices. Section II describes the decoder and how it works. Section II is divided into three subsections, where each section describes a particular circuit, implemented by using Multisim 10 software program [1]. Section III describes how we can extract the clock from Manchester data. The last section presents our concluding remarks.

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II. MANCHESTER DECODER

The idea of decoding the Manchester data is simply to make use of the encoded data itself. We can note from Fig. 1 that the encoding of the transition from 0 to 1 or vice versa (Mode A) has more time duration than the rest of the signal. Also, the same small duration of other transitions (Mode B) means that the encoding data has the same value (0 or 1) until Mode A occurs again. From these two observations, we can give the decoder the ability to realize what the original data was by simply dividing the Decoder into three stages, which are explained as follows:

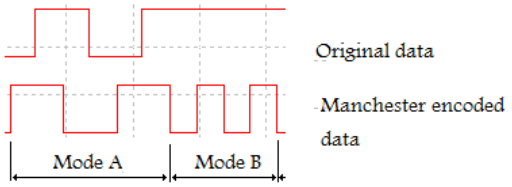


Fig. 1 Manchester data format

A. Smoothing the Encoded Data

Smoothing means making a slower transition from low to high or vice versa, compared with the original transition. This is simply done by using a charging and discharging theorem; i.e., using a capacitor and a resistor as shown in Fig. 2. We have to choose a time constant of a resistor-capacitor, τ, so that the capacitor has to reach a value in Mode A more than that in Mode B for both charging and discharging modes, although there are more than one value of τ that can be used, but we use the following assumption:

$$\tau = \frac{T}{\ln(9)} \quad (1)$$

$$\tau = R * C \quad (2)$$

Where
R: is the resistance.
C: is the capacitance.
T: is the maximum time duration of the Manchester encoded data.

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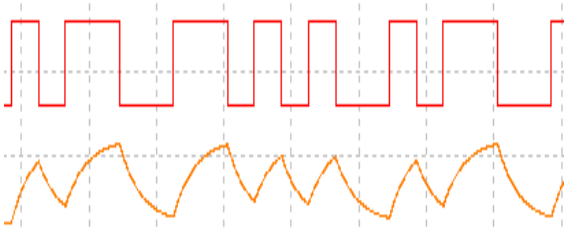


Fig. 2 (a) Manchester data before and after smoothing

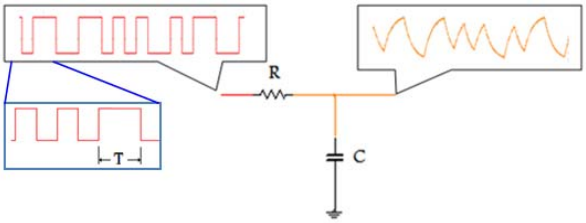


Fig. 2 (b) Stage 1 Circuit (Smoothing Circuit)

B. Low and High Level Segregation

To make use of the previous resulted output, we use two comparators: one is for the highest value and the other is for the lowest value. Fig. 3(a-c) shows the idea and the circuit used in this stage.

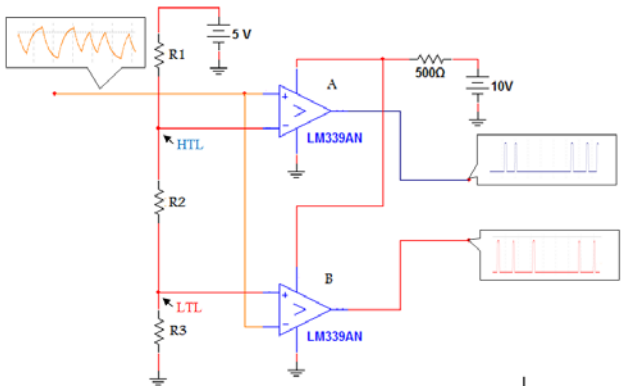


Fig. 3 (a) Stage 2 Circuit (Level segregation Circuit)

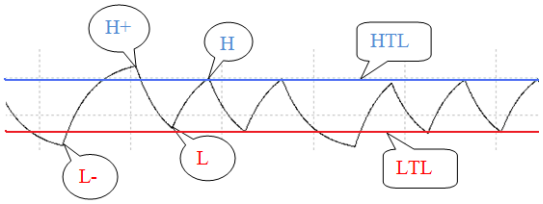


Fig. 3 (b) Indicates the threshold levels for both Comparators A and B, and the maximum and the minimum value of the smooth signal for both Modes A and B

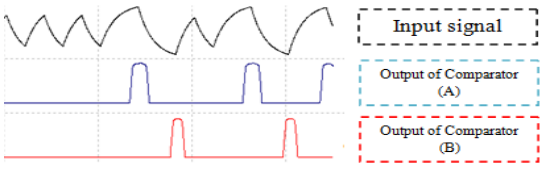


Fig. 3 (c) The output of Comparators A and B after comparing their input signal with HTL and LTL respectively

$$\max(H) \leq HTL << \min(H+) \quad (3)$$

$$\max(L-) << LTL \leq \min(L) \quad (4)$$

Where:
HTL: High Threshold Level.
LTL: Low Threshold Level.

The resistances of R1, R2, and R3 depend on the threshold voltage level required for comparison, as it is depicted from Equations (3) and (4). For high level comparison, Comparator A should compare its input with a threshold voltage level close to the Level H but lower than Level H+. For low level comparison, Comparator B should compare its input with a threshold voltage level close to Level L but higher than Level L-; as the threshold levels are far away from both H+ and L- since more time is available for the comparators to respond to changes of the smoothed signal, as shown in Fig. 4.

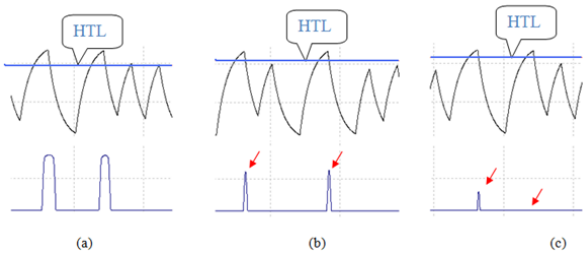


Fig. 4 The effect of choosing the value of the high threshold level on the output of Comparator A; (a) is the best case (HTL ≈ H); (c) is the worst case (HTL>>H)

We have implemented this circuit using Multisim 10 software program. The time period of the encoded data is about 8μs (Mode B). Table I indicates samples from the highest and the lowest values for both H and L (note: The simulated received signal has DC components; i.e., there is no voltage value less than zero volt).

TABLE I
INDICATES VALUES OF MAXIMUM AND MINIMUM SAMPLES OF THE SMOOTH SIGNAL

Voltage level	Sample 1 (Volts)	Sample 2 (Volts)	Sample 3 (Volts)	Sample 4 (Volts)
H+	4.505	4.54	4.601	4.58
H	3.76	3.74	3.714	3.814
L-	0.546	0.474	0.397	0.481
L	1.3	1.526	1.317	1.255

According to Table I and referring to (3) and (4), we have adjusted HTL and LTL to 3.89 and 1.1 volts respectively by assigning the values 1KΩ, 2.54KΩ, and 1KΩ to the resistances R1, R2, and R3 respectively.

C. The Decoder

J-K flip flop (ff) is used as the final stage of this decoding circuit, since it has the ability to realize whether the encoding data is low or high by testing the outputs of the two comparators. The clock for this device has been taken from the

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Manchester encoded data (i.e., before smoothing) using an XOR gate, where one of its inputs is directly passing the encoded data, and the other input is passing the same data but with a small delay performed by two NAND gates connected together in a serial format. Fig. 5 indicates how J-K ff works with the previous stages.

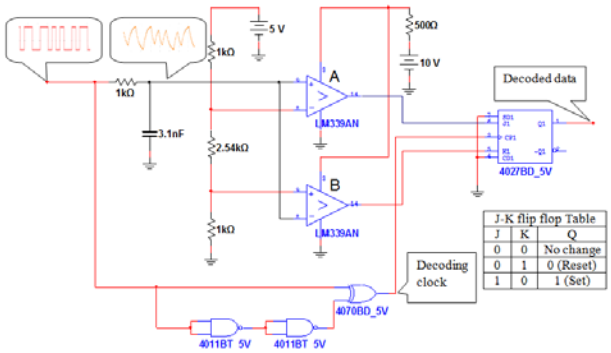


Fig. 5 Indicates the final stage of the Decoder; the output of Comparators A and B are connected with J-K ff in Ports J and K respectively; the Clear and Set ports are connected to the ground

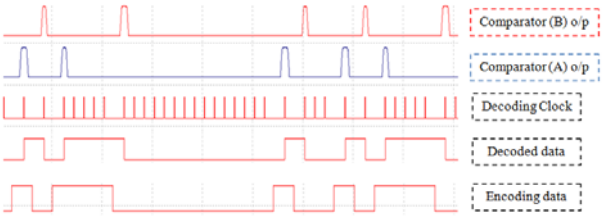


Fig. 6 shows the output of the decoded data and the related signals

It is important to note that the ability of this circuit to decode Manchester data depends on the properties of the used comparators such as: transition speed, time response, and sensitivity. Although this circuit showed a perfect ability for decoding in simulation for up to about 5.5µs mode B time period or 90Kbps (see the appendix) using commercial comparators (LM339) [2], if the frequency increases beyond this value this decoder will not be able to decode Manchester data any more due to the parameter of this device.

III. Extracting the Clock

Although we have successfully extracted the original data from Manchester data, we have not extracted the clock yet. However, we cannot immediately apply an XNOR gate between the received data and the decoded data, because there is a delay between both of them as shown in Fig. 7.

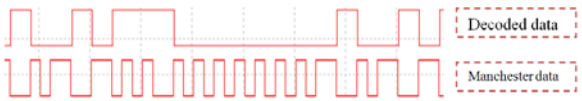


Fig. 7 Time comparison between the Manchester and decoded data

We can note from Fig. 7 that the transition of Manchester data is not at the middle of the decoded data. The reason for this delay is from the RC circuit and the two comparators. So, in order to compensate for this delay, we have applied another delay to the Manchester data using the same resistance and capacitance value. As of the smoothed circuit, a buffer is installed before this stage to separate the two circuits from each other. After this stage, the signal enters into the same circuit used for extracting the decoding clock (two NAND gates and one XOR gate), and the resulted output enters into the toggle J-K ff to divide the previous frequency by 2. Fig. 8 shows the circuit used for extracting the clock.

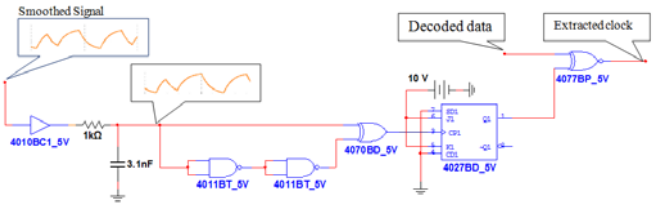


Fig. 8 The used circuit for extracting the clock from Manchester

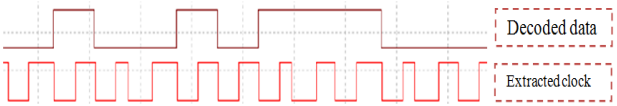


Fig. 9 The resulted extracted Clock

Although the extracted clock does not have the same time duration for all of its pulses as shown from Fig. 9, but it has showed the capability for serial to parallel converting (see the appendix).

IV. Conclusion

In this paper, we have introduced a simple circuit for decoding Manchester data without using any programmable devices. Furthermore, we have successfully extracted the clock from Manchester encoded data. Giving the ability for parallel to serial conversion using Multisim 10 software program, the achieved maximum data rate for this decoding circuit is about 90kbps. However, because this circuit depends on the comparator parameters, we do consider that the transmission rate can be further increased if high speed comparators are used. The main disadvantage of this circuit is the high amplitude dependence, and hence, the applicable transmission distance and the received voltage have to be taken into consideration before receiving any data.

References

[1] NI Multisim, Version 10.0.144, 2007National instruments.
[2] www.national.com/ds/LM/LM339.pdf

APPENDIX



Fig. 9. The required time for sending 8 bits of data (88.844μs / 90kbps), and the ability of the receiver to decode these encoded data at this speed

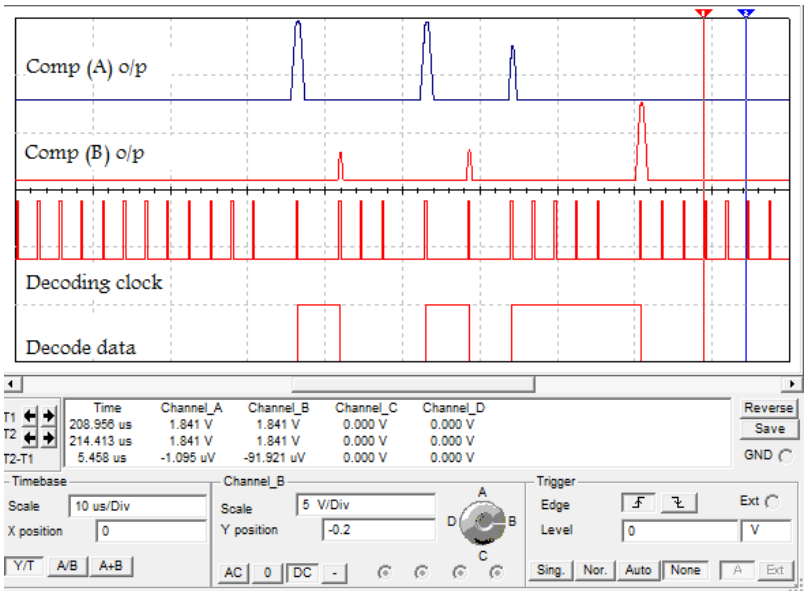


Fig.10 Oscilloscope output showing a successful decoding for up to 90kbps of transmission speed

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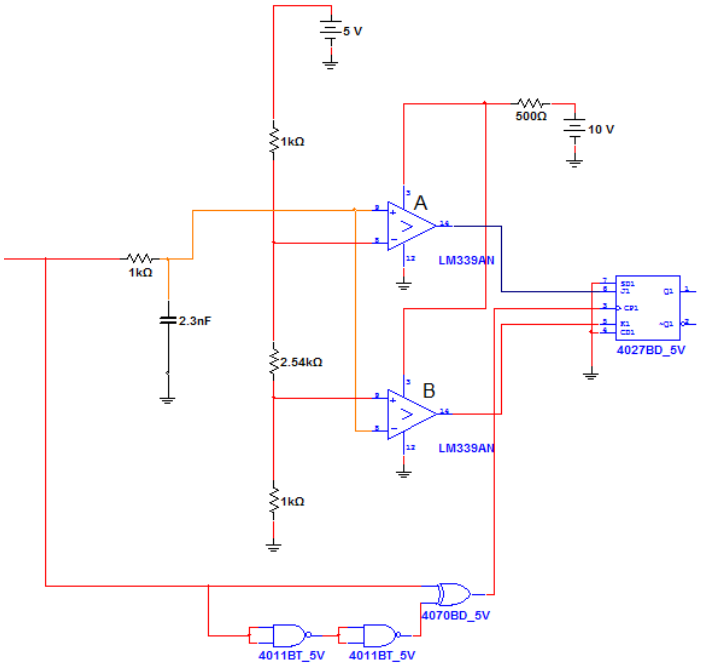


Fig. 11 Resistance and capacitance used for Manchester decoding circuit for decoding of 90Kbps of encoded data

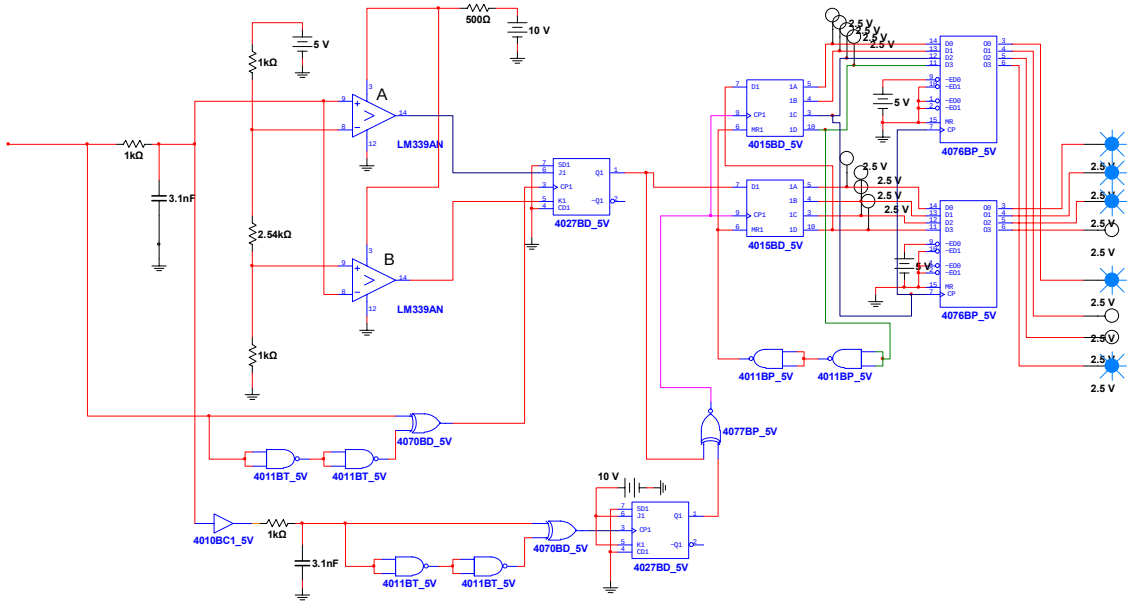


Fig. 12 The resulted output when the decoded data and the extracted clock has been applied into the serial to parallel converter circuit, the encoding data was 10010111