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Design of High Gain, High Bandwidth Op-Amp for Reduction of Mismatch Currents in Charge Pump PLL in 180 nm CMOS Technology

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***Abstract*—**The designing of charge pump with high gain Op-Amp is a challenging task for getting faithful response .Design of high performance phase locked loop require ,a design of high performance charge pump .We have designed a operational amplifier for reducing the error caused by high speed glitch in a transistor and mismatch currents . A separate Op-Amp has designed in 180 nm CMOS technology by CADENCE VIRTUOSO tool. This paper describes the design of high performance charge pump for GHz CMOS PLL targeting orthogonal frequency division multiplexing (OFDM) application. A high speed low power consumption Op-Amp with more than 500 MHz bandwidth has designed for increasing the speed of charge pump in Phase locked loop.

***Keywords*—**Charge pump (CP) Orthogonal frequency division multiplexing (OFDM),Phase locked loop (PLL), Phase frequency detector (PFD), Voltage controlled oscillator (VCO),

I. Introduction

A PLL based charge pump has been used to design because of its wide capture range and zero phase offset which is shown in Figure 1. The operation of this circuit is basically a feedback control system that controls the phase of a voltage controlled oscillator (VCO). Phase locked loop (PLL) consist of a phase frequency detector (PFD), loop Filter (LPF), charge pump (CP) and voltage controlled oscillator (VCO). Basically PLL has been using **i**n wireless communication wherever orthogonal frequency division multiplexing (OFDM) requires very compact and perfect synchronization of signal frequency. Orthogonal frequency division multiplexing (OFDM) is a special case of multicarrier transmission, where a single data stream is transmitted over a number of lower rate subcarriers [1]. A PLL is a part of this multi-carrier modulation system. Designing a GHz phase locked loop for multi-carrier communication with high stability using 0.18um CMOS technology is also a challenge in CMOS. Phase locked loop is mostly used in wireless communication and data recovery circuits. At present for above-mentioned application a low voltage low area and high performance integrated circuits are used which complicates the implementation of such type of integrated circuit.

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By parasite capacitance between the input and the output of the stage, slew rate can be approximately evaluated by SR = 2I o/Cc [2]. Here section-I completed the introductory part of the system. Section–II describes Phase Detector of PLL system. Section-III describes basics of charge pump. Section –IV describes the conventional Charge Pump. Section – V describes proposed High Gain Op-Amp. Section-VI describes proposed Charge Pump. Section-VII gives result and waveforms and last section-VIII gives conclusion

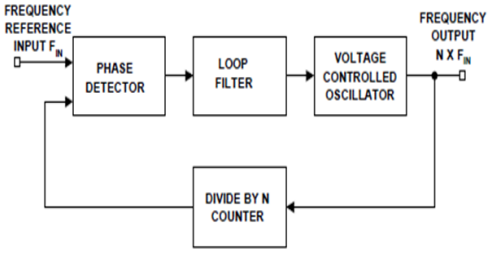


Fig. 1 Basic Phase Locked Loop

II. Phase Detector

A phase detector compares two input signals and produces an error signal, which is proportional to their phase difference. To form a phase-locked loop (PLL), the phase error output of PFD is fed to a charge pump and then to loop filter, which integrates the signal to get a sharper and smooth signal so that the disturbances at the input of VCO get minimized. If Vc reaches a stable equilibrium then the filter capacitor state variables have also reached the equilibrium. Therefore when considering the stability of a high order system, we need only monitor °e and Vc [9]

III. BASIC OF CHARGE PUMP

Basically CP consists of a current source, a current sink and switches. The CP is usually followed by a passive loop filter that changes the output current to a VCO control voltage; this voltage affects the charge pump output voltage. A charge pump in a PLL is an electronic switch that gives an output current, depending on the control signals from the phase detector. Figure 2 shows the circuit diagram of a conventional charge pump. To design a high performance Charge Pump a output resistance should be high because variation in currents that is mismatching in currents is inversely proportional to output resistance, which is helpful to reduce the current sensitivity to the drain-source voltage variation and improve current matching [3].

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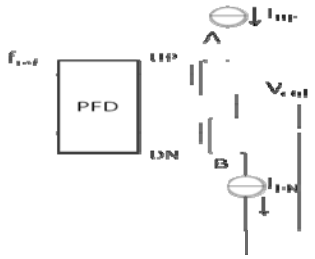


Fig. 2 Basic Charge Pump

PLL performance deteriorates due to non-ideal CP effects such as current mismatch and current noise. Mismatch between charging and discharging currents introduces a steady state phase error as well as reference spurs [4] .Current mismatch comes from device mismatch, channel-length modulation, and parasitic capacitors. It provides high output impedance. The gain at low frequencies is kept large so the PLL can lock to the desired frequency at all process, voltage and temperature (PVT) conditions [5]. Compensation techniques such as common mode feedback (CMFB) do not suppress the differential mismatch errors between charging and discharging current when the differential output voltage is not zero current will be larger than the discharging current on the other side [6].

IV. Conventional Charge Pump

In an conventional Charge Pump 13 transistors have used to implement the Charge Pump, in addition with this Op-Amp used to maintain Vmir and Vvco voltage has used 12 transistors .This circuit is helpful to minimize the current mismatch with the penalties in area and power dissipation [13]. To recover this we applied current and width equation and have found different Ron for different values of width of various transistors .The conventional Charge Pump has shown in figure 3.

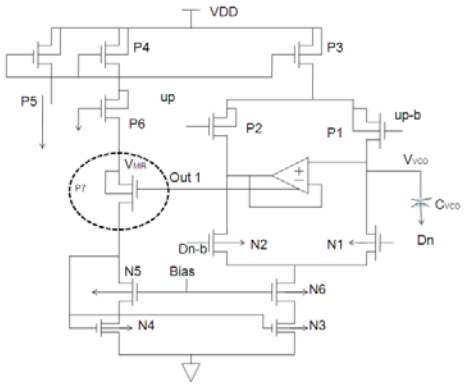


Fig. 3 Conventional Charge Pump

V. PROPOSED HIGH GAIN OP-AMP

The two stage op-amp has been used to design high gain amplifier and has introduced the important concept of compensation. The goal of compensation is to maintain stability The output has also voltage rate limit called slew rate which is generally determined by the maximum current available to charge or discharge the capacitance. The overall feedback amplifier gain is large, which equals the product of the gains of two amplifiers formed by two transistors. This large amplifier gain increases the current mirror output resistance significantly [3]. Settling time can completely determined from the location of the poles and zeros in the small signal equivalent circuit where as slew rate can be determined from the large signal condition of the circuit. Generally for designing two stages Op-Amp cascading of voltage to current and current to voltage amplifier stages can be used. The first stage current of a differential amplifier converting the differential input voltage to differential currents and the second stage current of differential amplifier converts current to voltage. If the discharging current mirror uses a cascade topology, the charging/discharging current curve in the effective output range will become flatter [8].If Vc reaches a stable equilibrium then the filter capacitor state variables have also reached the equilibrium. Therefore when considering the stability of a high order system, we need only monitor °e and Vc [9]. The rule to size the capacitance Cc1 can be easily carried out by merging expressions and to obtain both the desired settling time by means of z as supposed in and phase margin [10]. While the longer channel length may mitigate the channel length modulation effect, the increased parasitic capacitance coupling between the inputs and output of the charge pump may degrade the transient response of the charge pump via charge injection and charge sharing [11]. The same design is shown in figure 4. One of the compensation method is miller compensation is which a single capacitor C connected from output to input terminal [12]. If either the zero or the pole moves toward the origin of the complex frequency plane, the phase margin will be degraded. The rule to size the capacitance can be easily carried out by merging expressions and to obtain both the desired settling time by means of impedance as supposed in and phase margin [10]

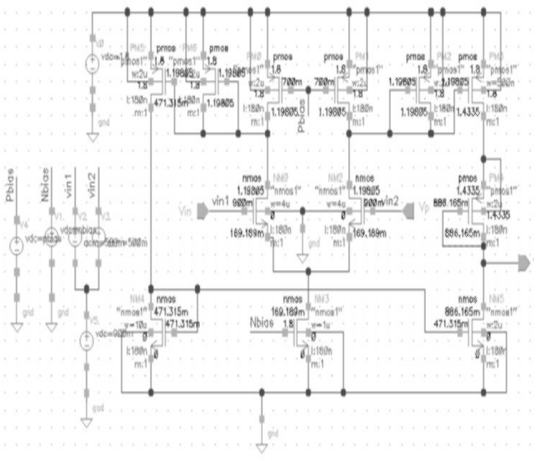


Fig. 4 Proposed High Gain Op-Amp

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VI. Proposed Charge Pump

In the actual implementation of a differential charge pump, the output current pulse forms glitches whose magnitude increases with the speed of the input signal. The high-speed glitch is generated by charging or discharging the gate-to-drain capacitance (Cgd) of the output transistors, which directly injects current into the output node. When this happens, the gate-to-drain capacitance increases and it induces glitch current [2].To minimize the glitch, always keep the output transistors in saturation region. Even more, it maximizes the switching speed of the charge pump if the output transistors work in saturation region instead of triode region. Thus, the glitches on the discharging current induced by the switching cancel each other. The charge pump circuits have non idealities, since the charge pump translates the digital timing information into an analog quantity for voltage-controlled oscillator (VCO) tuning, the non ideal behavior of the Charge Pump can contribute significantly to the PLL output-jitter. A new CP based on gain-boosting which reduced the channel length modulation effect. This output impedance is similar to triple-cascode output impedance but with less consumed voltage headroom. It is suitable for channel length modulation effect elimination but still have the problem of non-equal I Up and I Down [7].

While the longer channel length may mitigate the channel length modulation effect, the increased parasitic capacitance coupling between the inputs and output of the charge pump may degrade the transient response of the charge pump via charge injection and charge sharing[11] In the conventional Charge Pump circuit, an Op-Amp has been used was giving the high power dissipation because it was designed with large width of the transistor NM3 connected before output stage of Op-Amp .The two output taken from the proposed Charge Pump have been used to supply the voltage to low pass filter and second output back to the transistor .The transistors at the output have been working in the saturation region as per the proper selection of the width of all the transistor used in the circuit . We applied current and width equation and have found different Ron for different values of width of various transistors. On the basis of potential divider Vds and Vth and current equation we optimize the width of different transistors, which are shown in Table 1,and the new circuit of Charge Pump with new values of W/L has shown in the figure 5.The figure 6 shows the symbolical representation of complete Charge Pump.

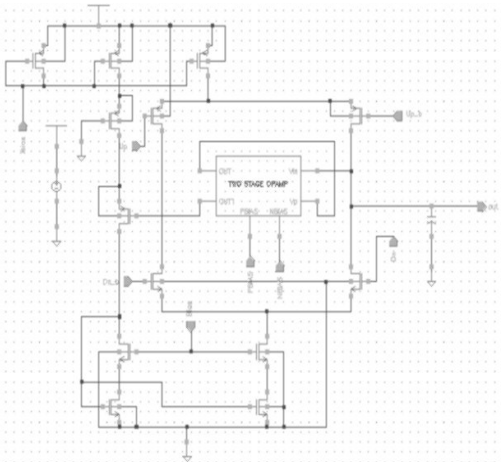


Fig . 5 Proposed Charge Pump.

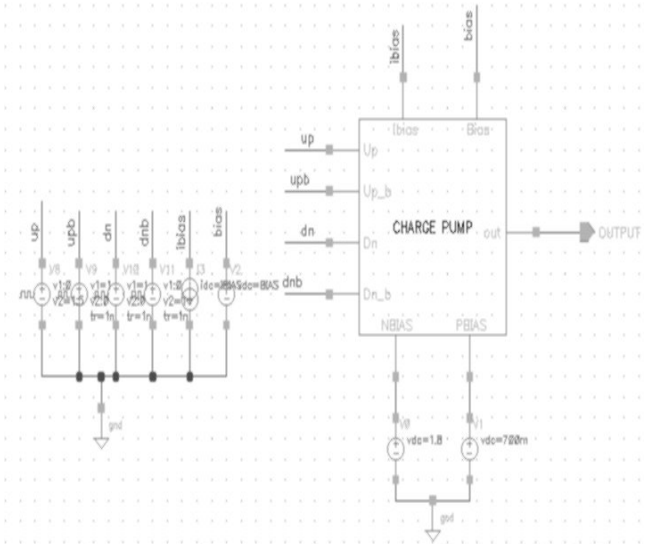


Fig . 6 Symbol of Proposed Charge pump.

VII. Result And Waveforms

The proposed high performance Charge Pump it has designed using 0.18 um CMOS Technology and circuit has simulated by CADENCE Virtuoso. In order to get all transistors in saturation W/L set at different aspect ratio with constant length 180 nm throughout the circuit. The selection of width of all transistors is on the basis of getting minimum area and power dissipation. A perfect matching low current as compared to conventional charge pump has presented. The frequency response of Op-Amp and output waveform of Charge Pump operated at 1.8 V has been shown in figure 7 and 8 respectively.

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TABLE I
WIDTH PARAMETER OF OP-AMP AND CHARGE PUMP

Op-Amp		Charge Pump	
Transistor	**Width in um**	**Transistor**	**Width in um**
NM0	4	PM0	4
NM2	4	PM1	4
NM3	1	PM3	2
NM4	8	PM4	4
NM5	2	PM5	10
PM0	2	PM6	2
PM1	2	PM7	4
PM2	2	NM1	8
PM3	0.5	NM2	8
PM4	2	NM3	4
PM5	2	NM4	4
PM6	2	NM5	4
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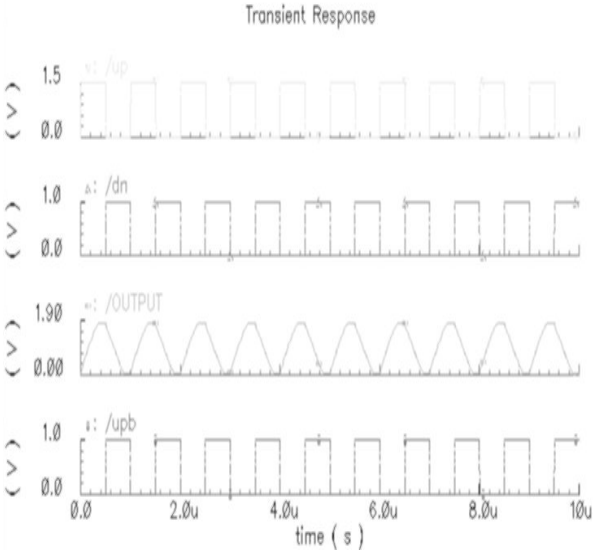


Fig . 8 Output Waveform of Charge Pump.

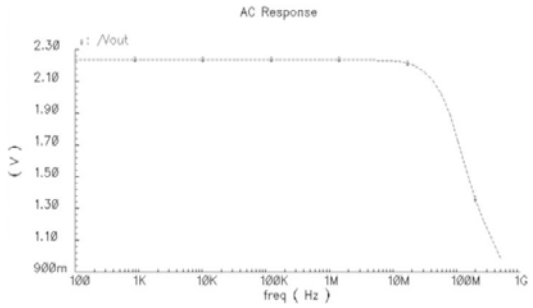


Fig .7 Frequency Response of Op-Amp.

VIII. CONCLUSION

A high performance Charge Pump Phase locked loop has been designed in 0.18 um CMOS Technology using CADENCE Virtuoso tool. A new high gain Op-Amp with low power dissipation has designed and introduced in the Charge Pump Phase Locked loop. The presented Charge Pump can be operated for more than 500 MHz bandwidth.

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