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Multi Band Frequency Synthesizer Based on ISPD PLL with Adapted LC Tuned VCO

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***Abstract*—**The 4G front-end transceiver needs a high performance which can be obtained mainly with an optimal architecture and a multi-band Local Oscillator. In this study, we proposed and presented a new architecture of multi-band frequency synthesizer based on an Inverse Sine Phase Detector Phase Locked Loop (ISPD PLL) without any filters and any controlled gain block and associated with adapted multi band LC tuned VCO using a several numeric controlled capacitive branches but not binary weighted. The proposed architecture, based on 0.35µm CMOS process technology, supporting Multi-band GSM/DCS/DECT/ UMTS/WiMax application and gives a good performances: a phase noise @1MHz -127dBc and a Factor Of Merit (FOM) @ 1MHz -186dB and a wide band frequency range (from 0.83GHz to 3.5GHz), that make the proposed architecture amenable for monolithic integration and 4G multi-band application.

***Keywords*—** GSM/DCS/DECT/UMTS/WiMax, ISPD PLL, keep and capture range, Multi-Band, Synthesizer, Wireless.

I. Introduction

THE key assumption in the multi-band receiver architecture is the multi-band frequency synthesizer which presents the local oscillator used to set the receiver in the desirable band, and to cover all the appropriate band, this statement cannot be achieved excepted by using a large band frequency synthesizer.

The voltage-controlled oscillator is an essential building block of the frequency synthesizer. However, VCO realized by the CMOS technology still remains some challenges in designing its RF module. The most critical performance specification for an oscillator is the phase noise, and by focusing on the VCOs architectures, the CMOS ring oscillators are an easy-to-integrate alternative and they have a benefit of a wide tuning range [1], but they exhibit inferior phase noise performance for a given power dissipation [2] and thus are not amenable in Local Oscillator application.

The harmonic oscillators offer very good jitter and phase noise performances but typically require the use of an LC tank, which need large area and menace the monolithic integration, but the LC VCO remain the optimal solution for a multi band Local Oscillator application.

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Many studies explore the tuning range of LC VCO and meet the multi-band requirement, and in order to enlarge the tuning range of the LC VCO, Hsia [1], Hajimiri [2], Seung [3], Razavi [5], Fong [6], and are interest at the capacitive part of the resonator circuit, and they conceived the multi band VCO by utilizing binary weighted switched capacitor, but all the generated frequencies bands are relied and concentrated to cover all the tuning range continuously, that assure a good frequency coverage but it limit the frequency range and the applications.

Noticing that the bands of the different standards like GSM, DCS, UMTS, WiMax are not ridden, our idea is to modify the LC VCO architecture used by Seung and Hsia in multi standard application, this modification reside in generate a separated bands by using a several numeric controlled capacitive branches but not binary weighted to enlarge the frequency coverage according the desired band.

In other hand, the conception of this VCO isn't the only way to design a multi-band synthesizer but also the synthesizer may be has an effective architecture. For thus, and due to the high performance of the Inverse Sine Phase Detector Phase Locked Loop (ISPD PLL) [7], our work is to combine the advantages of the ISPD PLL and the multi band LC tuned VCO to conceive a new architecture of multi band frequency synthesizer, since, the suppressed filter in the ISPD PLL makes the synthesizer able to operate in a large-band-frequency without using any gain block, and minimizes the lock up time of the circuit.

This structure gives the synthesizer the robustness of the ISPD PLL and the phase noise performances of the LC tuned VCO and it became completely integrated in the same wafer and its performances are proved in many publications [7], [8], [9]. This architecture is applied in 4G wireless receiver and it's proved by Multi-band GSM/DCS/DECT/UMTS/WiMax example, and simulated by employed the RF-simulation tools: Advanced Design system (ADS).

II. Proposed Multi Band Frequency Synthesizer

The proposed multi-band synthesizer use the ISPD PLL architecture associated with digital controlled multi-band tuned LC VCO and two other digital controlled blocks which control the steps selection in the selected band and the variation of the step selected to make the synthesizer able to

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operate at different bands which are usually didn't have the same characteristics.

Compared to the synthesizer based on standard PLL, the ISPD offer the synthesizer a large frequency coverage range without using any controlled gain block [7], that simplify the circuit's architecture and make it amenable for monolithic integrated application.

Further more, the mains parts of the proposed frequency synthesizer are the ISPD circuit and the multi-band VCO circuit, and the performances of the synthesizer are depending to the performances and robustness of there parts.

The key assumptions and approximations of the ISPD involved with employing the mathematical description of the ISPD characteristic. A new mathematical description of the ISPD characteristic is already studied and designed in previous study [7].

So, the conception of the proposed synthesizer is reduced to conceive and optimize the Multi-Band VCO which will determine the performances of the Local Oscillator circuit.

A. Optimization of adapted LC tuned VCO

The adaptation of the LC VCO architecture, for the GSM/DCS/DECT/UMTS and WiMax application, reside mainly on the determination of the number of switched capacitors branches needed to cover all the desired bands and the capacitors values.

The adapted VCO core consists of cross-coupled transistors MPI, MP2, MN3 and MN4, to drive the LC tanks to generate full-swing output voltages, spiral inductor and a capacitance block to induce the required oscillation frequencies. The capacitance block is made by a varactor to assure the continuously variation of the frequency and a switched capacitors to assure the discrete variation of the bands (figure 2).

Seen to the non linear variation of the frequency according to the capacitance (when the capacitance value increase, the slope of the frequency variation decrease), and in order to surpass the risk of the worst coverage of the minimal frequency band (GSM), we chose to divide the GSM coverage in two under-bands: the first can cover the uplink frequency range and the second can cover the downlink frequency range. Therefore, we need generate four bands: the first to cover the WiMax standards (2.5GHz to 3.5GHz), the second to cover the DCS/DECT/UMTS standards (1.71GHz to 2.1GHz), the third and the fourth to cover respectively the uplink and the downlink bands of the GSM standard.

So, in order to optimize the VCO architecture, both the varactor circuit, using of two capacitive branches is sufficient to cover four frequency bands, since the numeric command voltage "vc1" and "vc2" can take four numeric combinations, knowing that the low and the high logical states are respectively equivalent to 0V and 3V.

Concerns Our conception's algorithm, we start with sizing the active circuit according to constraints of 0.35µm process technology as supply voltage and the polarization current, after that we conceive the resonator circuit calibrated to cover the maximal frequency band (WiMax), then we pass to size the switching capacitances in order to assure the coverage of the minimal frequencies band (GSM).

To minimize the corner frequency of $1/f^3$ phase noise, the active circuit (negative resistance) is indispensable to have a symmetrical CMOS structure with the identical transconductance on the PMOS and NMOS transistors [4].

In the other hand, the grid length (L) must be in general the smallest possible to decrease the thermal noise and to increase the transition frequency of the transistor (either L=0.35µm).

The main constraint imposed on the sizing of the varactor circuit, it is that it must allow the coverage of the largest frequency band, so, the capacitance variation of the varactor can determined by:

$$\Delta C_{\text{var}} \geq \max\left\{\Delta C_{WiMax}, \Delta C_{DCS/DECT/UMTS}, \Delta C_{GSM,B1}, \Delta C_{GSM,B2}\right\} \quad (1)$$

Where ΔC_{WiMax} is the needed capacitance variation to cover the WiMax band; that is similar with $\Delta C_{DCS/DECT/UMTS}$, $\Delta C_{GSM,B1}$ and $\Delta C_{GSM,B2}$.

The Inversion mode (I-MOS) and the accumulation mode (A-MOS) MOS vractor structures present many advantages compared to the MOS structure like a wide and monotonous capacitance variation [4], but the choice of the structure A-MOS involved to replace the p+ diffusions by a n+ diffusions, that impose a technology constraints. Then, in order to conceive a flexible and adaptable circuit by all technologies, it is amenable to use the I-MOS varactor structure.

In our application, we used a varactor structure composed by two PMOS transistors, each functions in I-MOS capacitance. This structure offers more stability opposite to temperature effects [10].

The sizing of the two branches capacitances is can deduced by calculating the maximal total capacitance value needed ($C_{total,max}$), including the parasitic capacitances of the active circuit, and the minimal total capacitance value needed ($C_{total,min}$). So, by determine the equivalent capacitance variation of the two branches, the sizing of the first branch must switch the VCO from the WiMax band to the DCS/DECT/UMTS band and the sizing of the second capacitance branch must switch the VCO from the DCS/DECT/UMTS band to the GSM band.

The sizes of the resonator circuit's components are shown at the following table.

TABLE I
RESONATOR'S COMPONENTS SIZES

	Notation	values
Inductor	L	2.3pF
Varactor	MP7, MP8	500 µm /2 µm
1st capacitive Branch	C1	1.5pF
	MN9	100 µm /20 µm
2nd capacitive Branch	C2	15pF
	MN10	450 µm /30 µm

B. Simulation Results

Fig. 3 shows the simulation results of the varactor's capacitance according to the tuned voltage, show that the varactor permits to cover linearly a capacitance range going from 0.7pF to 1.97pF what gives 67.7% frequency coverage.

Fig. 4 shows the simulated oscillation frequency versus the

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control voltage of the proposed VCO as a function of the respective switching combinations. As can be seen in Fig. 4, the VCO can cover the GSM standard at tow separate bands (from 0.83GHz to 0.938 GHz and 9.43GHz to 1GHz) and the DCS/DECT/UMTS standards at one band (from 1.69GHz to 2.21GHz) and the WiMax fixe standard also at one band (from 2.27GHz to 3.5GHz). So, the overall frequency tuning range is 20% at the GSM band and 30% at the DCS/DECT/UMTS band and 50% at the WiMax band.

The phase noise performances of the proposed multi band VCO, are simulated with the ADS tools, which integrates the "Leeson" model.

TABLE II
PHASE NOISE AND FOM SIMULATED VALUES OF THE PROPOSED MULTI BAND VCO

Bandes	Frequency GHz	Phase Noise @1MHz	FOM @1MHz
WiMax	2.27	-127.155 dBc	-186.08 dB
	3.5	-124.1 dBc	-186.786 dB
DCS/UMTS	1.69	-122.885 dBc	-179.247 dB
	2.21	-118.416dBc	-177.108 dB
GSM	0.83	-120.236 dBc	-170.422 dB
	1	-117.246 dBc	-169.05 dB

The Figs. 5 and 6 show the phase noise simulation at maximal and minimal frequencies (0.83GHz and 3.5GHz). The Table II shows the simulated values of phase noise and Factor Of Merit (FOM) (using fong expression [6]) of the proposed VCO at 1MHz Offset frequency, at the different generated bands. As can be seen in these results that the best phase noise of the proposed multi band VCO is -127dBc at 2.27GHz and the best FOM is -186dB.

C. Frequency Synthesizer Performances

The conception of the multi band VCO present the most important stage in the conception of our multi band frequency synthesizer based multi on ISPD PLL, whereas the roles of the other constitutions of the synthesizer are to control its grappling to the desired band and to vary the frequency jump according to the synthesis frequency-step. Therefore, we cannot disregard the effects of there components, for this reason, we simulated the behavior of the whole synthesizer, by using the conceived VCO.

Figure 7 shows the lock up time of the proposed multi band synthesizer at the WiMax band is 8ns.

Knowing that the lock up time of the synthesizer based on classic PLL is in order of 30ns [7], we can evaluate our multi band synthesizer as fast.

The keep and capture ranges are important characteristics of the frequency synthesizer, they describe its frequency performances. Generally, the keep range is limited by the linearity of the VCO, whereas the capture range depends of the gain and the speed of the synthesizer.

To simulate the keep and capture ranges of the proposed synthesizer, we varied the frequency of the input reference signal by using another VCO controlled by the "Freq_command" signal (Fig. 8).

Knowing that the sensibility of the VCO in the WiMax band is 615MHz/V, Fig. 8 shows that the keep range of the proposed multi band synthesizer applied in WiMax band is:

$$\Delta f_{keep,WiMax} = K_{VCO} \times \left(V_{keep,\max} - V_{keep,\max}\right) = 0.615 \times (3.54 - 1.25) = 1.4GHz \quad (9)$$

And its capture range is:

$$\Delta f_{capture,WiMax} = K_{VCO} \times \left(V_{cap,\max} - V_{cap,\max}\right) = 0.615 \times (3 - 1.86) = 0.7GHz \quad (10)$$

The Table III summarizes the keep and capture ranges of the proposed synthesizer at the different generated bands.

TABLE III
FREQUENCY SYNTHESIZER PERFORMANCE

Band	Lock up time	Keep range	Capture range
WiMax	8ns	1.4GHz	0.7GHz
DCS/DECT/UMTS	12.7ns	587MHz	101.4MHz
GSM	14ns	73MHz	30MHz

According to the Table III, we can conclude that the synthesizer, with its keep range, can cover the totality of all the desired bands (GSM/UMTS/DCS/DECT/WiMax) with a good and large capture range.

Fig. 9 and 10 show the spectrums simulations of the proposed multi band synthesizer respectively at minimal and maximal frequencies of each band.

So, the simulation results show that by using the frequency synthesizer based on ISPD PLL without any filters and without any controlled gain block, we can cover the GSM/DCS/DECT/UMTS/WiMax bands with a good performances and a wide band frequency range, that make the proposed architecture receiver based on ISPD PLL amenable for monolithic integration and multi-band application.

III. CONCLUSION

Due to the good performances of the adapted multi-band LC VCO, the frequency synthesizer architecture based on ISPD PLL presented high performances and good potentiality to cover GSM/DCS/DECT/UMTS and WiMax bands. Moreover, the simplicity of this architecture allows saving area and power in favour of 4G programmable single chip - multimode - very high scale integration.

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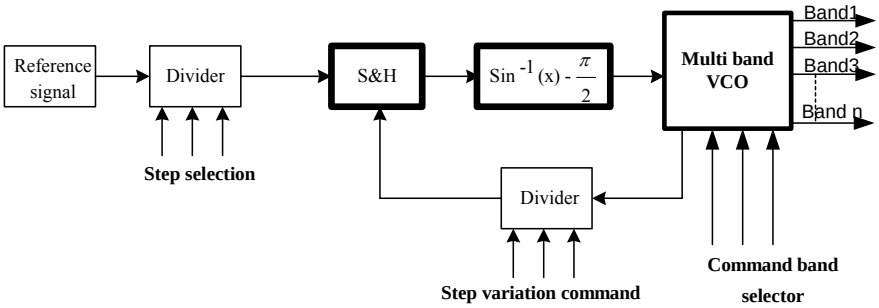
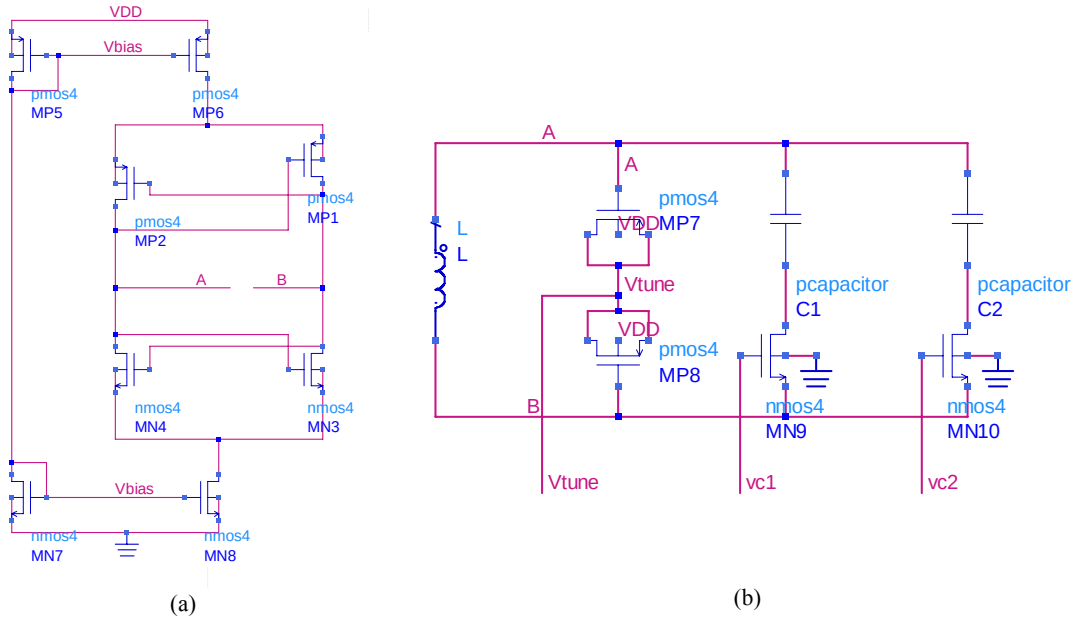


Fig. 1 Architecture of the proposed multi-band frequency synthesizer



(a) (b)

Fig. 2 Transistor schema of the multi-band VCO: (a) Active circuit; (b) Resonator circuit

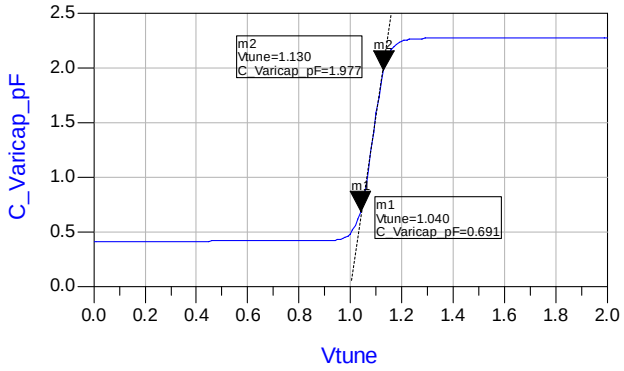


Fig. 3 Simulated varactor's capacitance variation vs the tuning voltage

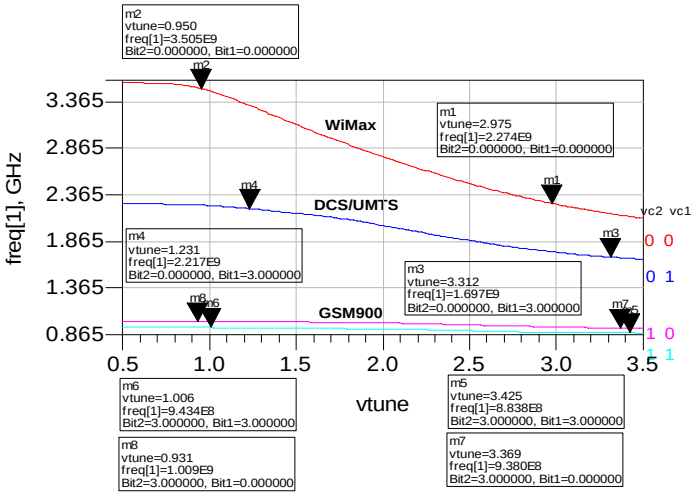


Fig. 4 Simulated oscillation frequency versus the control voltage of the proposed VCO as a function of the respective switching combinations

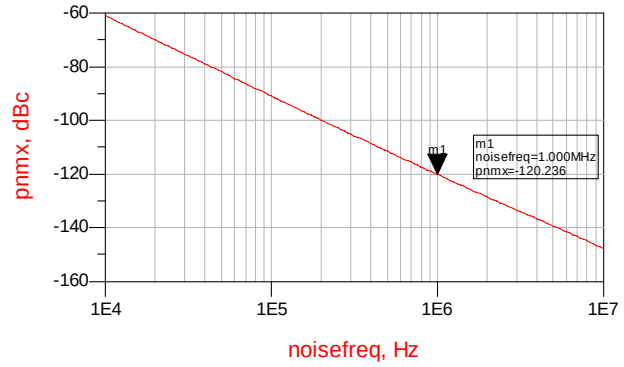


Fig. 5 Phase Noise simulation at f_{VCO}=0.883GHz

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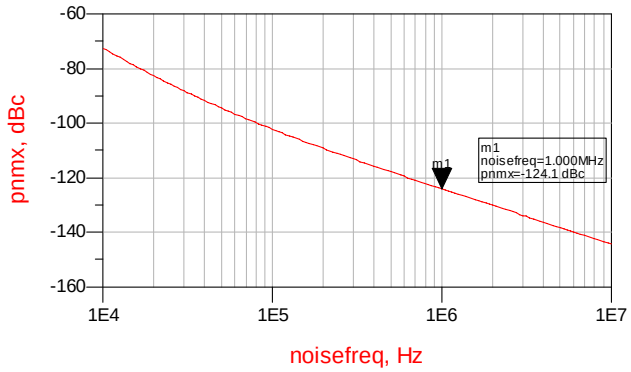


Fig. 6 Phase Noise simulation at f_{VCO}=3.5GHz

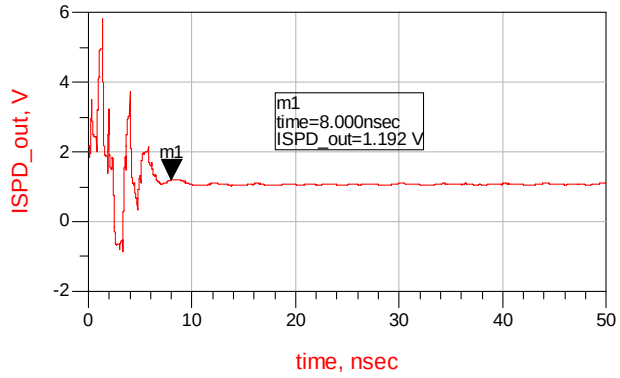


Fig. 7 Lock up time simulation of the multi band synthesizer at WiMax Band

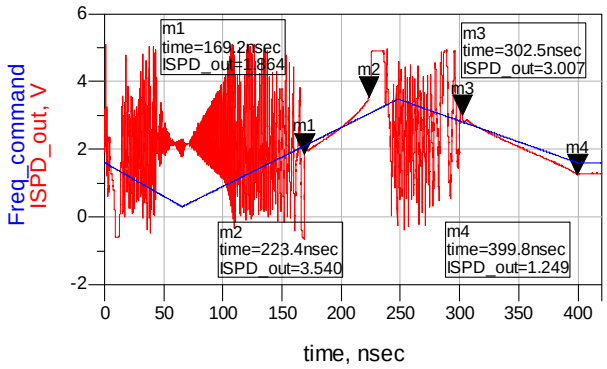


Fig. 8 Keep and capture range simulation of the proposed frequency synthesizer applied in WiMax band

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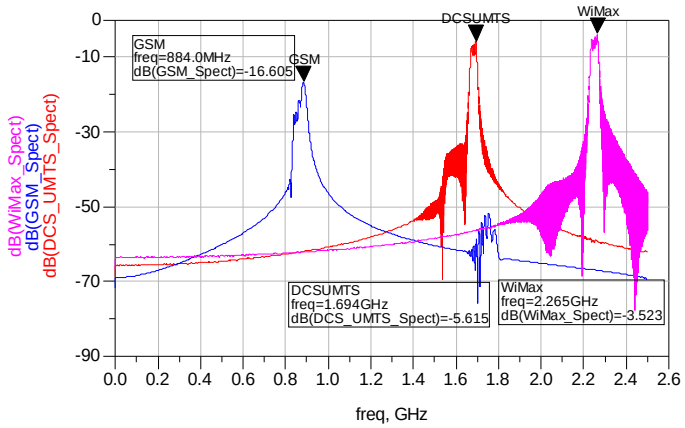


Fig. 9 Simulated spectrum of the multi band synthesizer at the minimal frequencies of each band

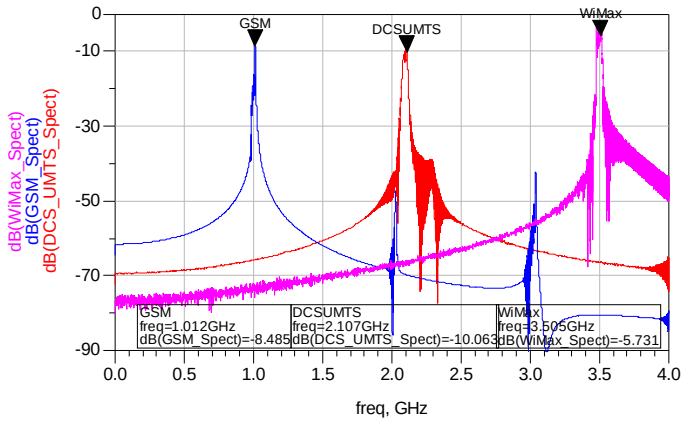


Fig. 10 Simulated spectrum of the multi band synthesizer at the maximal frequencies of each band

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