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Level Shifted Carrier Signal Based Scalar Random Pulse Width Modulation Algorithms for Cascaded Multilevel Inverter Fed Induction Motor Drive

M. Nayeemuddin, T. Bramhananda Reddy, M. Vijaya Kumar

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***Abstract*—**Acoustic noise becoming ever more obnoxious radiated by voltage source inverter fed induction motor drive in modern and industrial applications. The drive utilized for industrial and modern applications should use "spread spectrum" innovation known as Random pulse width modulation (PWM) algorithms where acoustic noise emanates through the machine should be critically concerned. This paper illustrates three types of random PWM control algorithms with fixed switching frequency namely 1) Random modulating PWM 2) Random carrier PWM and 3) Random modulating-carrier PWM. The spectrum plots of the motor stator current demonstrate the strength and robustness of the proposed PWM algorithms. To affirm the proposed algorithms, experimental tests have been conducted using dSPACE rt1104 control board on a v/f control three phase induction motor drive fed by DC link cascaded multilevel inverter.

***Keywords*—**Multilevel inverter, acoustic noise, CSVPWM, total harmonic distortion, random PWM algorithm.

I. Introduction

VARIABLE speed drives have achieved a state where they have turned into a key part in numerous modern applications [1]. The fundamental reasons are their enhanced computerization execution, and furthermore the cost is consistently diminishing. However the voltage source inverter fed AC drive produces noise during its operation. This is an unfavorable phenomenon. Noise is harmful to human health and is cumbersome. A man picks up sounds in the compass of 20 Hz to 20 kHz. The noise caused by the drive is in the orbit of 5 to 15 kHz, which is in the audiable range of human; the noise of high intensity may cause hearing loss.

A noise with more than 80 dB is considered as dangerous noise. Noise can be diminishments of up to 20 dB, when the magnitude of the stator flux in the motor drive was reduced [2]. However, noise reduction can be done either by creating an ideal PWM to straightforwardly diminish the harmonic distortion, or by increasing the switching frequency closer to the ultrasonic range where the human ear cannot hear, however this is restricted to low power converters (< 10 kW) due to switching frequency device.

Dr. Nayeemuddin. M is with Electrical Engineering Department, G. Pulla Reddy Engineering College (Autonomous), Kurnool, India (e-mail: nayeemgprec@gmail.com).

Dr. T. Bramhananda Reddy is with Electrical Engineering Department, G. Pulla Reddy Engineering College (Autonomous), Kurnool, India.

Dr. M. Vijaya Kumar is with the Electrical Engineering Department, JNTUA University, Ananthapuramu, India.

It is accepted that force due to noise is equal to square of the magnetic induction in the gap. The magnitude of the harmonic voltage is influenced by the noise level. PWM algorithm influences the characteristic of the harmonic spectrum of current and voltage. Acoustic noise can be decreased by randomizing change of the voltage spectrum in the range of higher harmonics. This can be achieved by randomizing the pulse pattern and such control strategies are known as random PWM algorithms [3]-[5]. This paper presents three different types of random PWM algorithms for cascaded multilevel inverter fed induction motor drive.

1) Random modulating PWM algorithm
2) Random carrier PWM algorithm
3) Random modulating-carrier PWM

II. Proposed Random PWM Algorithm

The voltage source inverter fed induction motor drives are utilized in most industries and modern applications and they operate at a switching frequency at 1 kHz to 20 kHz. Hence it is audible to human, the noise of high strength and long-lasting results in hearing loss. Continuous PWM and Discontinuous PWM based level shifted based scalar PWM algorithms are developed in the literature for voltage source inverter fed induction motor drives [4]. By escalating the switching frequency, acoustic noise can be decreased; however, in the meantime, it increases the switching losses and efficiency. Recognizing the recommended solutions for the lessening of whistling noise (acoustic noise), it is discovered that this acoustic noise is because of high energy concentration at and around the harmonic spectrum of the switching frequency [5]. Subsequently, to moderate these impacts the energy concentrated at and around the harmonic spectrum of switching frequency should be minimized.

There are fundamentally two types of random PWM algorithms, random pulse position modulation and random carrier frequency modulation algorithms. In CSVPWM, it is noticed that the time periods (T1, T2, Tz) are consistent for all pulses [6], [7]. In random pulse position algorithm pulse position is randomized, however switching frequency is kept constant.

In random carrier frequency modulation algorithm carrier frequency is varied over a wide band. With randomly varying switching frequency and randomly varying pulse position algorithms, spread spectra can be accomplished. However, continuous variation in the switching frequency requires complex filter design [8], [9]. Hence, for easier filter design

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and reducing complexity in implementation, fixed switching frequency random PWM (RPWM) techniques are gaining importance. This paper focuses on constant switching frequency RPWM algorithms. In the proposed algorithms PWM signals are generated either, by randomizing the modulating reference signal or by randomizing carrier signal or both.

A. Random Modulator PWM Algorithms (RMPWM)

In RMPWM algorithms, modulating reference signal is randomized. To generate modulating signals for three-phase cascaded multilevel inverter fed AC drive, three phase reference sinusoidal signals which are phase shifted by 120^{O} are considered as given in (1):

$$V_i = V_p * Sin\ (w_e t - 2(j-1)\pi/3) \quad (1)$$

where i=a,b,c and j=1,2,3 (i = j).

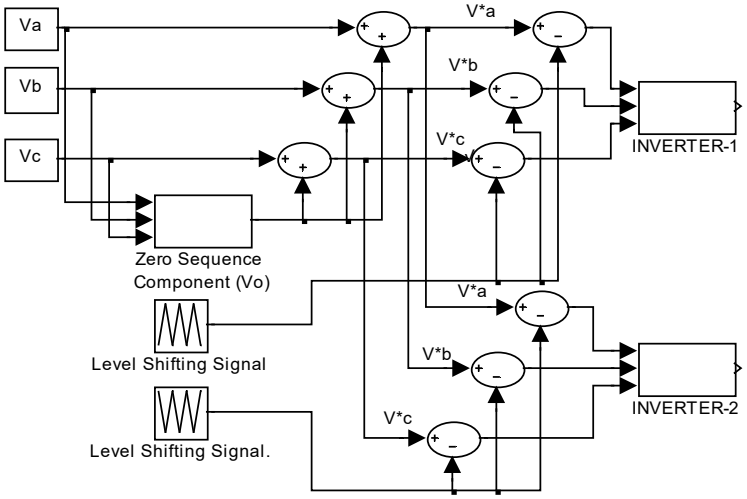


Fig. 1 Block diagram of carrier comparison based PWM employing zero sequence injection principle

The concept of injected zero sequence signal is incorporated in the proposed algorithm; the modulating signal can be obtained by adding the zero sequence component to the three phase reference sinusoidal signals.

A generalized expression that generates the zero sequence components V_0 as a function of V_M, V_m and Z_0 is given by [10]

$$V_{zs} = -[(1-2*Z_0) + Z_0 * V_M + (1-Z_o) * V_m] \quad (2)$$

where

$$Z_0 = \frac{T_7}{T_0 + T_7} \quad (3)$$

By using the zero sequence component, various PWM Modulators can be generated and expressed in terms of V_0 and reference signal as

$$\overset{*}{V}_i = V_i + V_{zs} \quad (4)$$

T_0+T_7 = T_z gives the total freewheeling time (zero state time) of the inverter; V_M and V_m are the maximum and minimum values of the three phase reference signal (V_i). When Z_0 = 0.5, and Z_0 = random(1) from (2) results in the conventional space vector PWM algorithm and RMPWM algorithm respectively. Random is a function which generates a random number between 0 and 1. The modulating signals shown in Figs. 2 and 3 are compared with high frequency level shifting triangular signals to generate the PWM control signals for inverter-I and inverter-II.

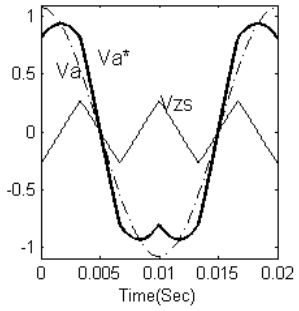


Fig. 2 Sin signal (V_a), zero sequence signal (V_{zs}) and Modulating signal (V_a*): CSVPWM algorithm

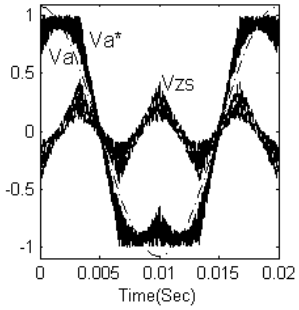


Fig. 3 Sin signal (V_a), zero sequence signal (V_{zs}) and Modulating signal (V_a*) : RMPWM algorithm

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B. Random Carrier PWM Algorithms (RCPWM)

In the proposed RCPWM algorithm, modulating reference signals (UN randomized) will be compared with randomly varying level shifted carrier signals. As shown in Fig. 4, positive and negative level shifting carrier signals with fixed frequency are considered. The decision among positive and negative carrier signals relies up on random generator. The random generator generates a high or low pulse (0 or 1) with a frequency equivalent to that of switching frequency which is kept fixed.

If the random generator generates 1 then carrier selector chooses positive or else it generates 0 then the carrier selector chooses a negative level shifting carrier signals. Thus, relying upon random generator, the yield of carrier selector is a mix of both positive and negative level shifting carrier signals.

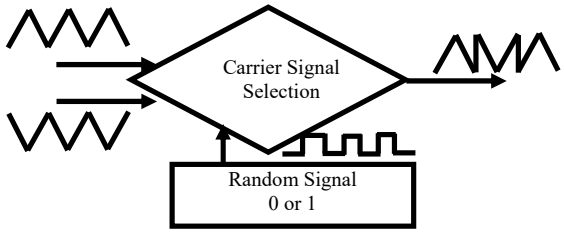


Fig. 4 Block diagram describing the basic principle of carrier selection.

C. Random Modulator-Carrier PWM Algorithms (RMCPWM)

In the preceding two randomized control algorithms, either modulating signal or level shifting carrier signals are randomized. Presently in this algorithm with the idea of diminishing the magnitudes of harmonics at and around the side bands of switching frequencies, both modulating signal and carrier signals are randomized as discussed in previous sections. Fig. 5 illustrates the random modulating-carrier PWM algorithm for cascaded 3-level inverter configuration.

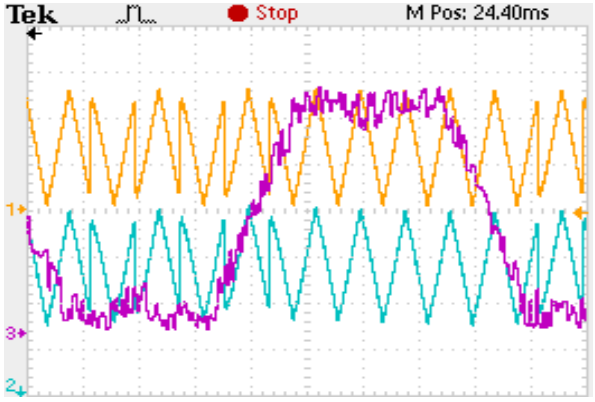


Fig. 5 Random M-C PWM algorithm

III. Cascaded Three Level Inverter Fed Induction Motor Drive Description

In this paper, a 3-level inverter has been proposed with a configuration. In this circuit configuration, 3-level pole voltage is obtained by cascading two 2-level inverters as shown in Fig. 6. In this circuit DC-link capacitors do not carry the motor currents and hence the voltage fluctuations in the neutral point are truant. From Fig. 6, it might be noticed that the phases of inverter-1 are connected with the DC-input terminals of the corresponding phases in inverter-2.

An isolated DC-power supply voltage of Vdc/2 is fed to each inverter. The notations V_{a1o}, V_{b1o}, Vc_{1o} individually denote the output voltages of inverter-1 with respect to the point 'O'. Similarly, the notations V_{a2o}, V_{b2o}, V_{c2o} individually denote the pole voltages of inverter-2 with respect to the point 'O'.

In inverter-2 of any phase, the pole voltage of V_{dc} is obtained when top switching device of that phase in inverter-2 is turned on or the top switching device of the corresponding phase in inverter-1 is turned on. Similarly the pole voltage of $V_{dc}/2$ of inverter-2 of any phase is obtained when the top switching device of that phase in inverter-2 is turned on or the bottom switching device of the corresponding phase in inverter-1 is turned on. Furthermore, the pole voltage of zero in inverter-2 of given phase is obtained, if the bottom switching device of the corresponding phase in inverter-2 is turned on. Therefore, the pole voltage of 0, $V_{dc}/2$ and V_{dc} which is the feature of a three level inverter is obtained.

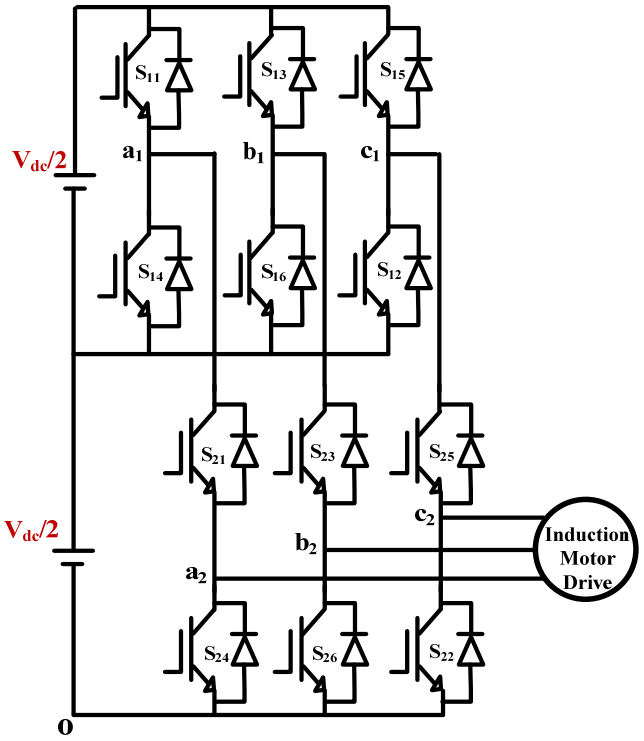


Fig. 6 Proposed three-level cascaded inverter configuration

The main advantage of the proposed cascaded inverter is that if any of the top switching devices of inverter-1 fails, it can be operated as a conventional 2-level inverter. This is accomplished by turning on the bottom switching devices of Inverter-1, i.e. the devices S14, S16 and S12 (Fig. 6) and only the devices of Inverter-2 (S21 through S26) are utilized.

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Another advantage is to obtain three level output, it requires only two DC power supplies of $V_{dc}/2$ each while the H-bridge topology requires three isolated DC power supplies (of $V_{dc}/2$ each).

TABLE I
POLE VOLTAGE OF INVERTER-2

Switches turn on Inverter-I	Switches turn on Inverter-2	Pole voltage of nverter-2
S14 or S16 or S12	S21 or S23 or S25	V_{dc}
S14 or S16 or S12	S21 or S23 or S25	$V_{dc}/2$
S11 or S13 or S15	S22 or S24 or S26	0
S11 or S13 or S15	S22 or S24 or S26	0

IV. EXPERIMENTAL RESULTS

To validate the performance of proposed Scalar RPWM algorithms, experimental tests have been conducted on v/f controlled AC drive. Fig. 7 shows the hardware measurements of positive and negative level shifting carrier signals at constant frequency of 500 Hz. Random generator generates either positive or negative logic signal based on which level shifting carrier signal is selected as shown in Figs. 8 and 9. For the analysis and comparison of results, the harmonic spectra of line voltage and current for cascaded 3 level inverter are shown. The zoomed portions of harmonics at and around switching frequency are shown from Figs. 27-42.



Fig. 7 Modulating reference and level shifting carrier signals: CSVPWM

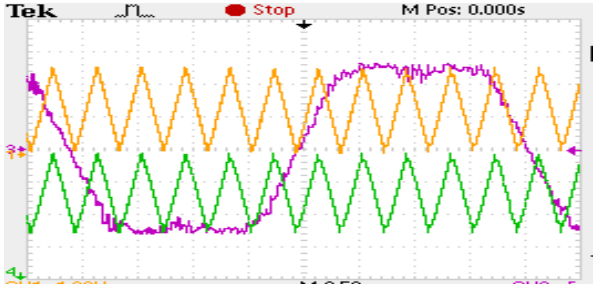


Fig. 8 Modulating reference and level shifting carrier signals: RMPWM

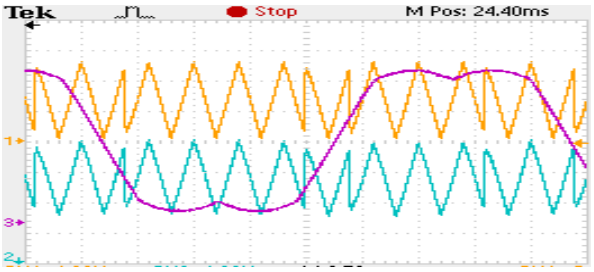


Fig. 9 Modulating reference and level shifting carrier signals: RCPWM

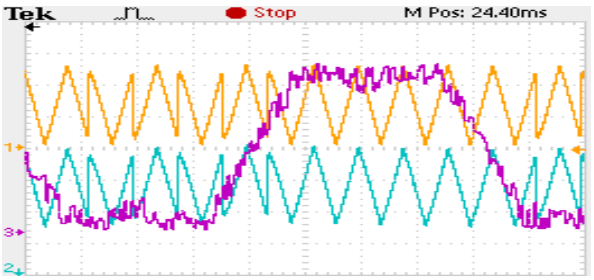


Fig. 10 Modulating reference and level shifting carrier signals: RMCPWM

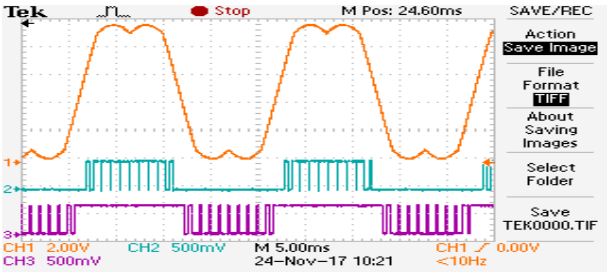


Fig. 11 SVPWM: Modulating Signal, Pulses for Inverter-I & II

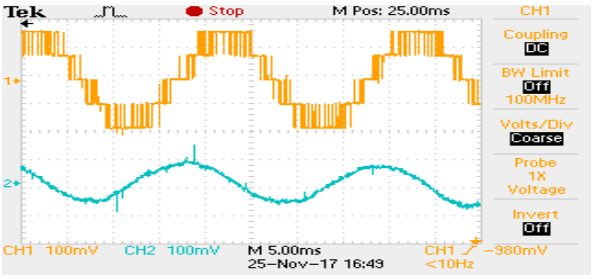


Fig. 12 SVPWM: Line Voltage, Stator Current

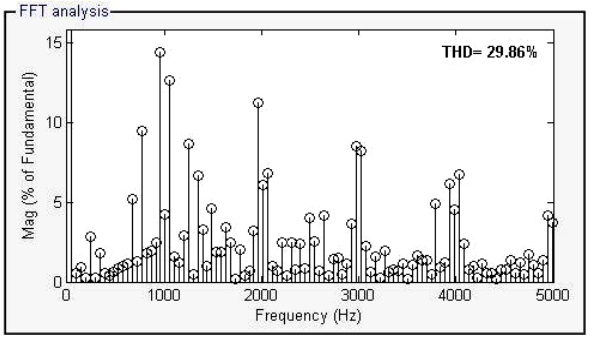


Fig. 13 SVPWM:: Harmonic distortion of line Voltage

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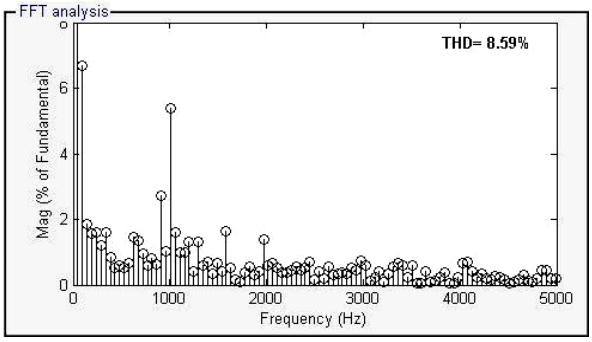


Fig. 14 SVPWM: Harmonic distortion of stator current

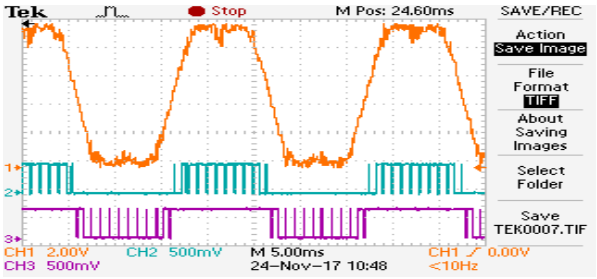


Fig. 15 RMPWM: Modulating Signal, Pulses for Inverter-I & II

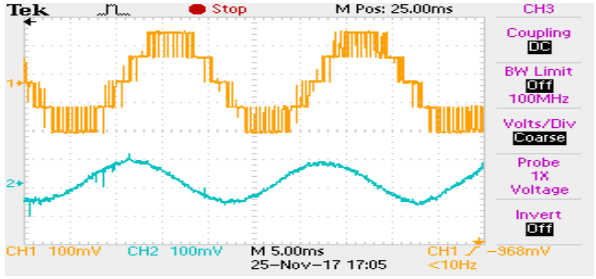


Fig. 16 RMPWM: Line Voltage, Stator Current

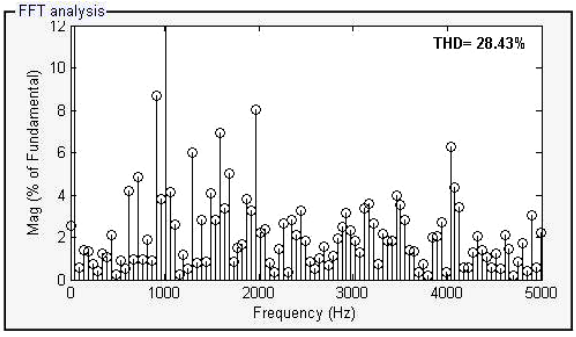


Fig. 17 RMPWM: Harmonic distortion of line Voltage

TABLE II
COMPARISON OF LINE CURRENT THD & HARMONIC SPECTRUM

S.No.	Control Algorithm	THD	
		Voltage	Current
1	CSVPWM	29.46%	8.59%
2	RMPWM	28.43%	7.90%
3	RCPWM	27.64%	7.16%
4	RMCPWM	24.96%	6.43%

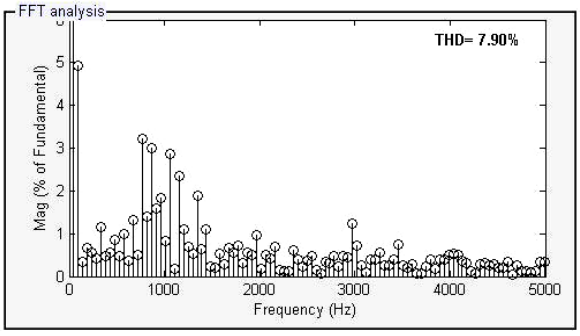


Fig. 18 RMPWM: Harmonic distortion of stator current

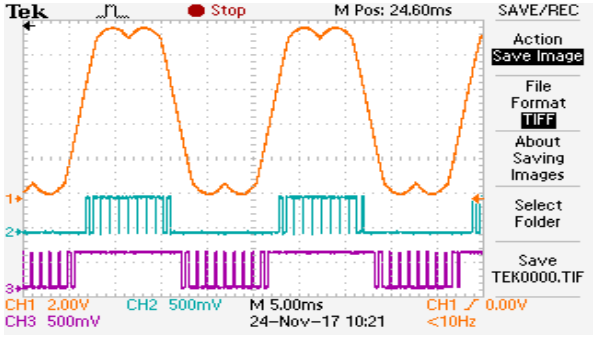


Fig. 19 RCPWM: Modulating Signal, Pulses for Inverter-I & II

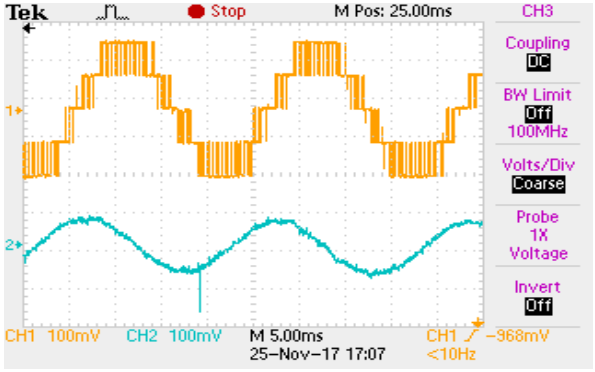


Fig. 20 RCPWM: Line Voltage and Stator Current

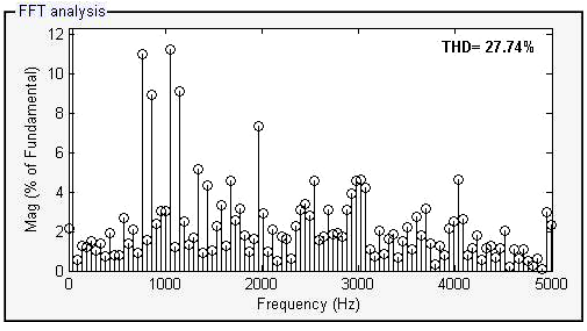


Fig. 21 RCPWM: Harmonic distortion of line Voltage

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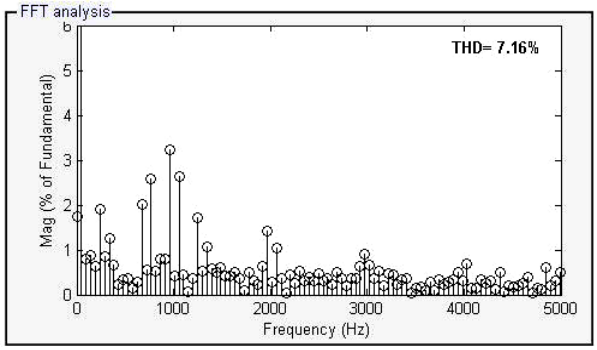


Fig. 22 RCPWM: Harmonic distortion of stator current

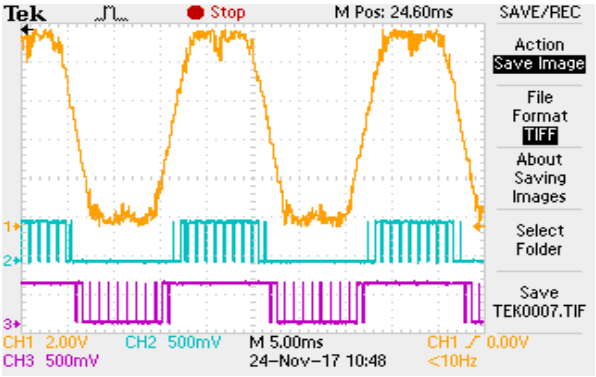


Fig. 23 RMCPWM: Modulating Signal, Pulses for Inverter-I & II

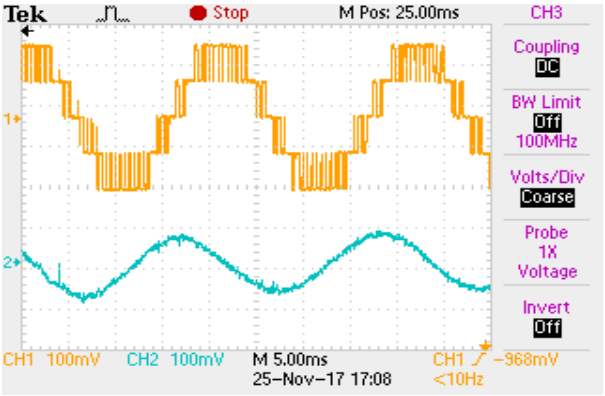


Fig. 24 RCMPWM: Line Voltage and Stator Current

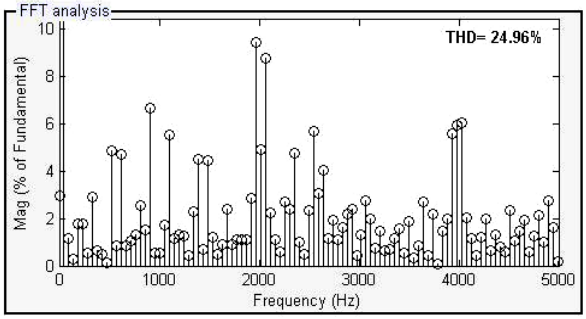


Fig. 25 RCPWM: Harmonic distortion of line Voltage

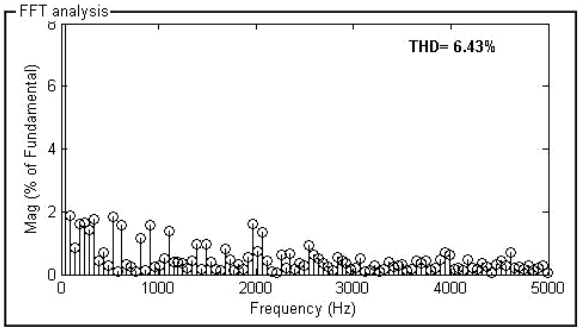


Fig. 26 RCPWM: Harmonic distortion of stator current

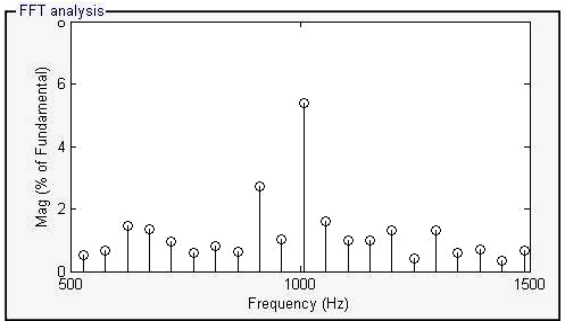


Fig. 27 SVPWM: Zoomed Portions at and around 1 kHz

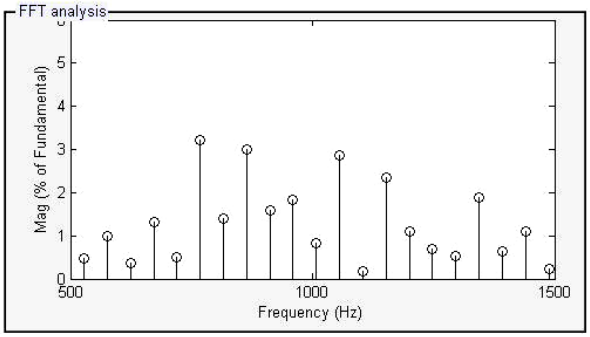


Fig. 28 RMPWM: Zoomed Portions at and around 1 kHz

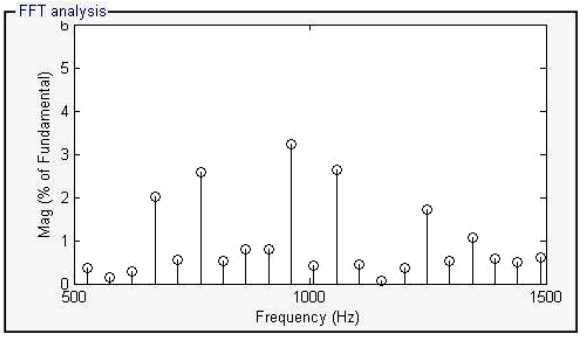


Fig. 29 RCPWM: Zoomed Portions at and around 1 kHz

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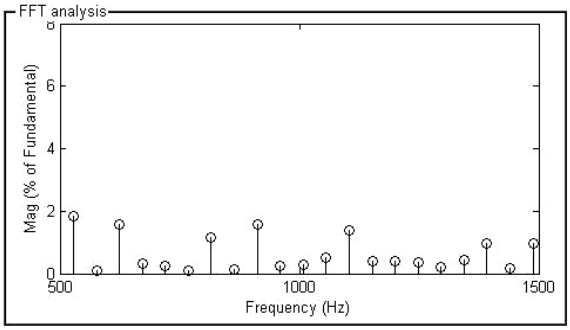


Fig. 30 RMCPWM: Zoomed Portions at and around 1 kHz

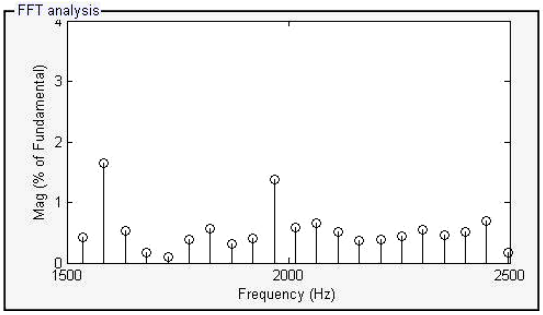


Fig. 31 SVPWM: Zoomed Portions at and around 2 kHz

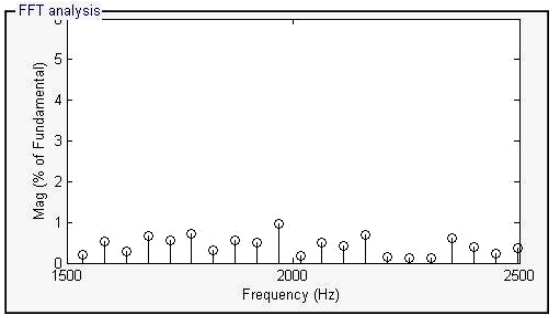


Fig. 32 RMPWM: Zoomed Portions at and around 2 kHz

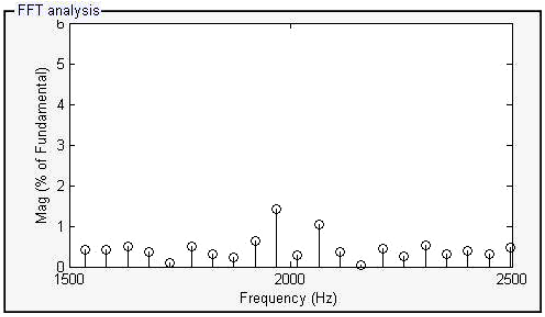


Fig. 33 RCPWM: Zoomed Portions at and around 2 kHz

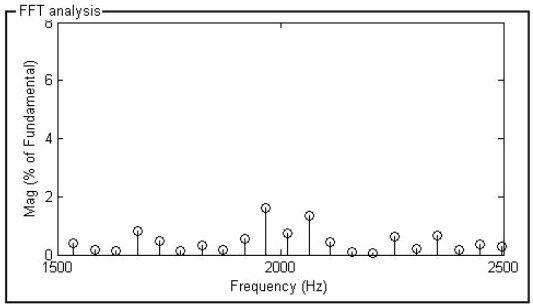


Fig. 34 RMCPWM: Zoomed Portions at and around 2 kHz

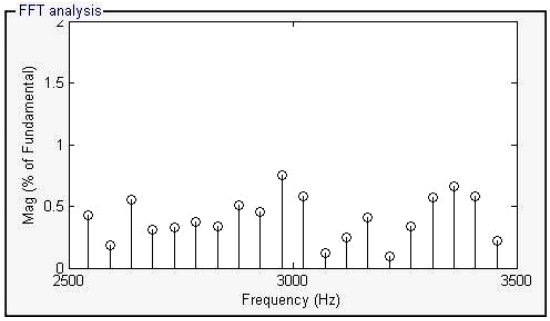


Fig. 35 SVPWM: Zoomed Portions at and around 3 kHz

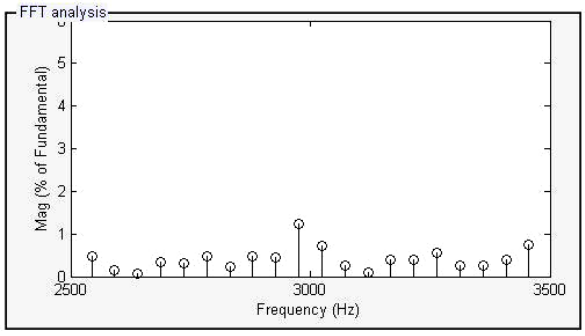


Fig. 36 RMPWM: Zoomed Portions at and around 3 kHz

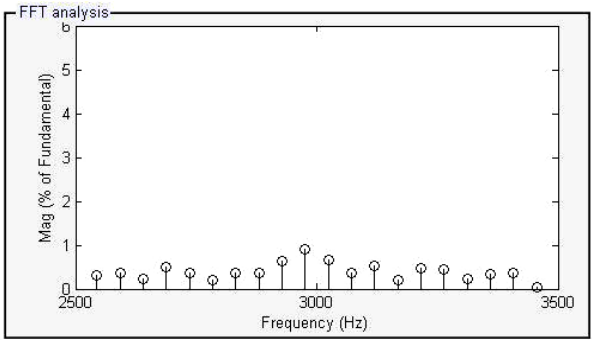


Fig. 37 RCPWM: Zoomed Portions at and around 3 kHz

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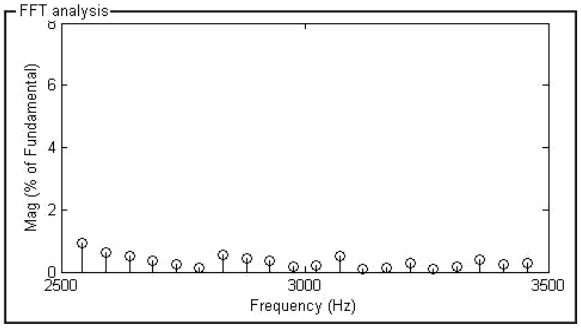


Fig. 38 RMCPWM: Zoomed Portions at and around 3 kHz

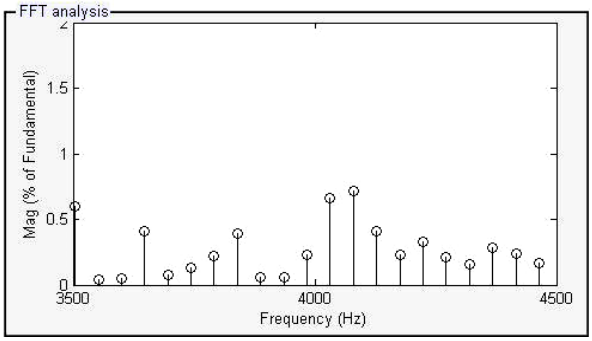


Fig. 39 SVPWM: Zoomed Portions at and around 4 kHz

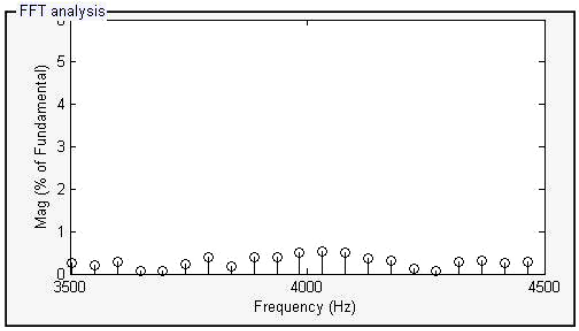


Fig. 40 RMPWM: Zoomed Portions at and around 4 kHz

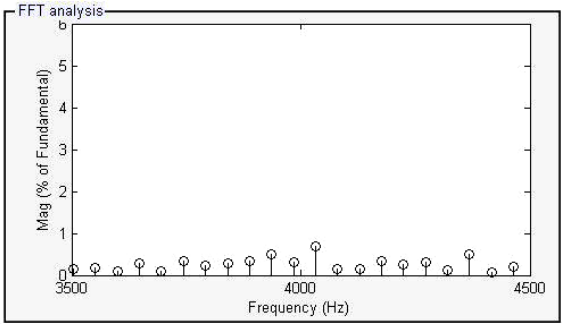


Fig. 41 RCPWM: Zoomed Portions at and around 4 kHz

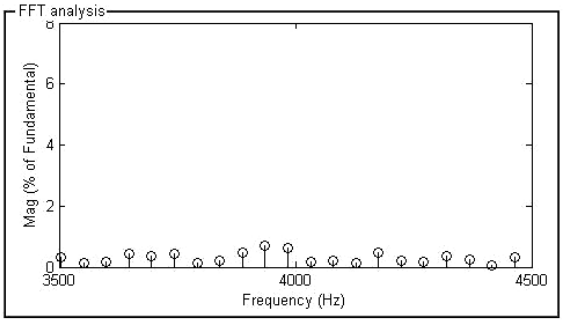


Fig. 42 RMCPWM: Zoomed Portions at and around 4 kHz

It is to be noted that the switching frequency is maintained constant at 1 kHz for all PWM algorithms, it is observed from the zoomed portion of the harmonic spectrum shown in Figs. 27-42 that lot of energy is concentrated at harmonics (multiples) of switching frequency (around 1 kHz, 2 Khz, 3 kHz and 4 kHz), but with the proposed RPWM algorithm the harmonic around the switching frequency are reduced. Voltage levels in phase voltage plots with all the RPWM are the same but, because of the randomization pulse, position may be changed. Hence, harmonic magnitude may increase or decrease. So, THD values of voltage and current plots with RPWM techniques may deviate (increment or decrement) from that of CPWM technique. Moreover, it is observed that there is a reduction in THD with RPWM. This reduction is because of a reduction in magnitude of the harmonics at and around harmonics of switching consequence in decreasing noise.

V. Conclusion

In this paper level shifted carrier signal based three scalar RPWM algorithms, namely RMPWM, RCPWM and RMCPWM for cascaded three level inverter fed v/f controlled induction motor drive are presented. The modulating signal can be achieved by adding a zero sequence signal to the sinusoidal reference signals. From the results it is concluded that the RPWM algorithms employed for AC drive give reduced harmonic distortion and also confirm the superiority when compared to SVPWM algorithm in the form of distributed spectra that results in reduced acoustic noise.

Appendix

- Induction Motor: 1Hp, 415 V, 1.8 A and 50 Hz
- DC-link converter: 3-phase, 9.3 kVA and 415 V, 13 A.
- Control board: dSPACE 1104 control board.
- Switching frequency: 1 kHz
- Applied effective input DC-voltage: 510 V
- Voltage sensor: LV-20P: 500 V - 6.3 V
- Current sensor: LA-55P: 50A - 6.3 V (used with six turns)

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Hardware Setup of the Drive

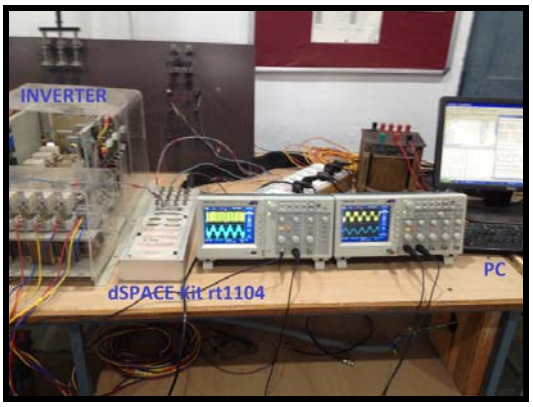


Fig. 43 Zoomed portion of Hardware Setup

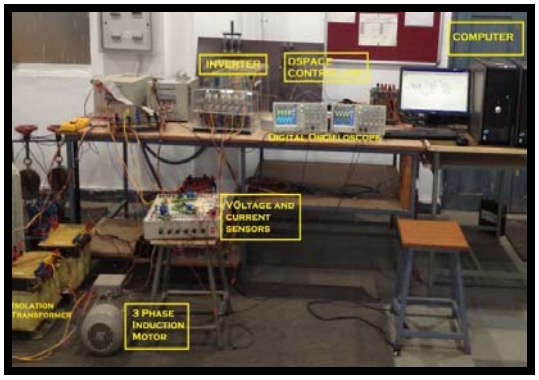


Fig. 44 Complete Hardware Setup

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Dr. Nayeemuddin.M had completed his B.Tech and M.Tech in 2005 and 2008 with first class in the department of Electrical and Electronics Engineering from J.N.T.University Hyderabad and Sri Krishna Devaraya, University Ananthapuramu respectively. He was Ph.D. in 2017. He is working as a Associate Professor in the Department of Electrical and Electronics Engineering at G. Pulla Reddy Engineering College, Kurnool, India. His scientific research is focusing on Power Electronics, and Motor Drive control.

Dr. T. Bramhananda Reddy had completed his B.Tech and M.E in 2001 and 2003 with first class in the department of Electrical and Electronics Engineering from Sri Krishna Devaraya University Ananthapuramu and Osmania University, Hyderabad respectively. He obtained doctoral degree from J.N.T. University, Ananthapuramu in 2009. He is working as a Professor and Head of the department of Electrical and Electronics Engineering in G.P.R Engineering College, Kurnool. He presented more than 120 research papers in various national and international conferences and journals. His research areas include PWM techniques, Power Electronics and control of electrical drives.

Dr. M. Vijaya Kumar graduated from NBKR Institute of Science and Technology, Vidyanagar, A.P, India in 1988. He obtained M.Tech degree from Regional Engineering College, Warangal, India in 1990. He received Doctoral degree from JNT University, Hyderabad, India in 2000. Currently he is working as Professor in Electrical and Electronics Engineering Department, JNT University, Anantapur, A.P, India. He has published over 84 research papers. He received two research awards from the Institution of Engineers (India). His areas of interests include Electrical Machines, Electrical Drives, Microprocessors and Instrumentation.