World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:9, No:7, 2015

Ambipolar Effect Free Double Gate PN Diode Based Tunnel FET

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Open Science Index, Electronics and Communication Engineering Vol:9, No:7, 2015 publications.waset.org/10004862/pdf

***Abstract*—**In this paper, we present and investigate a double gate PN diode based tunnel field effect transistor (DGPNTFET). The importance of proposed structure is that the formation of different drain doping is not required and ambipolar effect in OFF state is completely removed for this structure. Validation of this structure to behave like a Tunnel Field Effect Transistor (TFET) is carried out through energy band diagrams and transfer characteristics. Simulated result shows point subthreshold slope (SS) of 19.14 mV/decade and ON to OFF current ratio (I_{ON} / I_{OFF}) of 2.66 × 10^{14} (I_{ON} at V_{GS}=1.5V, V_{DS}=1V and I_{OFF} at V_{GS}=0V, V_{DS}=1V) for gate length of 20nm and HfO_2 as gate oxide at room temperature. Which indicate that the DGPNTFET is a promising candidate for nano-scale, ambipolar free switch.

***Keywords*—**Ambipolar effect, double gate PN diode based tunnel field effect transistor, high-κ dielectric material, subthreshold slope, tunnel field effect transistor.

I. Introduction

THE CMOS scaling offers various challenges for nano-scale MOSFETs. To overcome the challenges faced by nano-scale MOSFETs, various advanced design structures like multi gate, triple gate, gate all around and finFET are proposed in literature [1]-[3]. SS for these structures is limited to 60mV/decade. Steep SS, low OFF-state leakage current and ultra-low power consumption made the p-i-n based tunnel FET (TFET) the most promising device to replace MOSFET. Because of band to band tunneling a double gate TFET (DGTFET) with high-κ gate dielectric shows I_{ON} / I_{OFF} of more than 2 × 10^{11} [4] and become suitable for low-standby-power switch. Carbon nanotube-based tunnel field-effect transistor [5], and impact-ionization MOS-based transistor [6], [7] have lower value of SS then TFET but at the cost of complexity in fabrication and a high operating voltage. However, the conduction mechanism of TFET is completely dependent on tunneling, different design structures to improve tunneling rate are proposed in literature [8]-[10]. Using hetrojunction at source side reduces the band gap of tunnel junction which causes a boost in ON current [8]. This hybrid topology to improve ON current uses different semiconducting materials, which increase cost and complexity of fabrication process. With different gate work function, junction less TFET (JLTFET) [9] gives advantage of both conventional TFET and JLTFET, which has lower value of I_{ON} / I_{OFF} and SS.

In this paper, a simple structure for TFET is presented, which uses single doped region at source side. As formation of drain doping is not required, with this structure, fabrication steps will reduce compared to p-i-n TFET structure. While connecting drain contact with silicon-pad, we analyze ambipolar effect near drain contact during OFF stage. This unwanted tunneling is removed by reducing gate length (L_G).

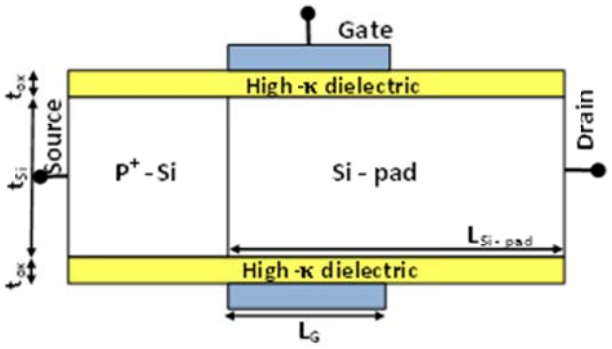


Fig. 1 Cross-sectional 2-D view of n-type Double gate PN diode based TFET (DGPNTFET) with high-κ gate dielectric: Width of the device is 1μm

II. Device Structure and Operation

The proposed n-type DGPNTFET structure is shown in Fig. 1. The parameters used in our simulation are: P^+ source doping (N_A) = 1×10^{21} cm^{-3} with length of 20nm, n-type silicon (Si-pad) with doping concentration N_D= 1×10^{17} cm^{-3}, length of Si-pad ($L_{Si\text{-}pad}$) = 50nm, gate length (L_G) = 20nm, oxide thickness (t_{ox}) = 2nm, silicon body thickness (t_{Si}) is limited to 10nm therefore we have not considered any quantum mechanical effects [11]. To get better control over device operation, double gate with gate work function = 4.5eV is considered in this work. Si-pad is directly connected with drain contact as reported in [16].

Silvaco Atlas 2-D device simulator is used to carry out all the simulations. To model the tunneling process more accurately, to consider spatial variation of energy bands and to take into account the generation or recombination of opposite carriers we used non-local Band-to-Band tunneling (BBT non-local) model. Because of high doping concentration at source side Klassen's Band-Gap Narrowing (KBGN) and Shockley-Read-Hall (SRH) recombination model is used [12].

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TABLE I
DEVICE STRUCTURE PARAMETERS FOR DGPNTFET

Parameter	Value
Gate length (L_G)	20nm
Oxide Thickness(t_{ox})	2nm
Gate oxide and permittivity(ε)	HfO2,22
Silicon body thickness(t_{Si})	10nm
P^+ Source doping (N_A)	1×10^{21} cm^{-3}
Si-pad doping	1×10^{17} cm^{-3}
Si-pad length($L_{Si\text{-}pad}$)	50nm

TABLE II
SIMULATION RESULTS OF DGPNTFET WITH DIFFERENT DONOR CONCENTRATION

N_D (cm^{-3})	I_{OFF}(ATV_{DS}=1, V_{GS}=0V)	I_{ON}(atV_{DS}=1V,V_{GS}=1.5V)	I_{ON}/I_{OFF}	SS
1×10^{15}	3.28×10^{-17}	8.96×10^{-5}	2.73×10^{12}	22.56
1×10^{16}	3.32×10^{-18}	9.27×10^{-5}	2.79×10^{13}	21.64
1×10^{17}	3.64×10^{-19}	9.70×10^{-5}	2.66×10^{14}	19.14

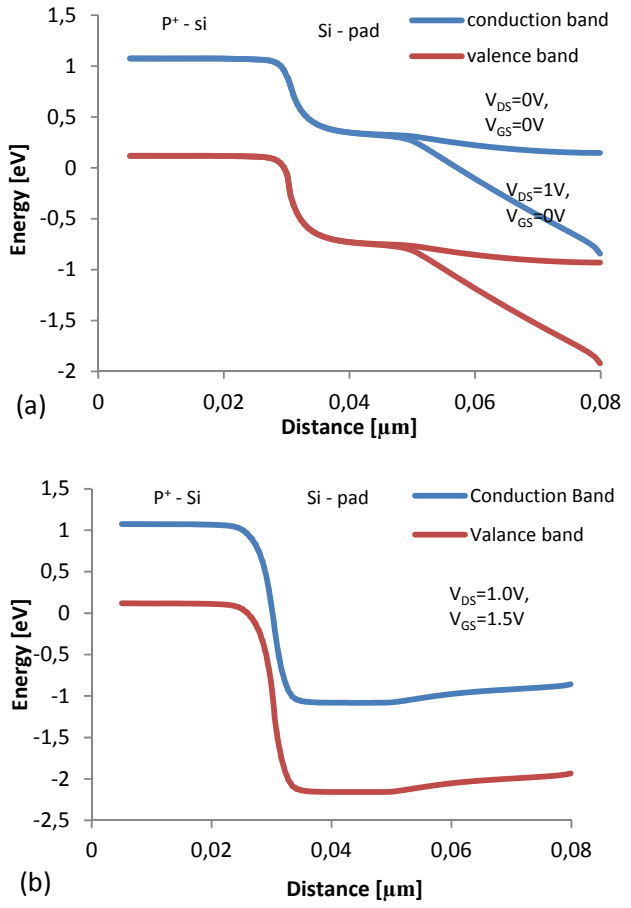


Fig. 2 (a) Energy band diagram for OFF – state (V_{GS} =0V, V_{DS}=0V and V_{DS}=1V). (b) Energy band diagram for ON – state (V_{GS}=1V, V_{DS}=1V) of DGPNTFET

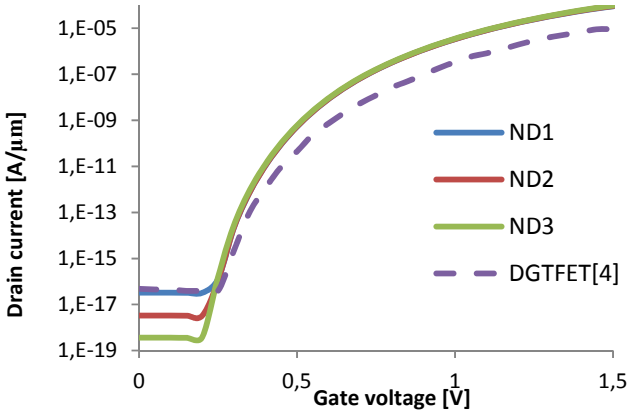


Fig. 3 Transfer characteristics of DGPNTFET and DGTFET [4] as a function of gate voltage. Here Si-pad donor doping (N_D) ($N_{D1}=1\times10^{15}$ cm^{-3}, $N_{D2}=1\times10^{16}$ cm^{-3}, $N_{D3}=1\times10^{17}$ cm^{-3})

In this basic gated PN diode design shown in Fig. 1, tunneling takes place between reverse biased p^+- n interface. Probability of tunneling T(E) is minimum for grounded source and zero gate bias which has been derived in the study[15] as,

$$T(E) \propto exp\left(-\frac{4\sqrt{2m^*E_g^{\frac{3}{2}}}}{3|e|\hbar(E_g+\Delta\Phi)}\sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}}t_{ox}t_{Si}}\right)\Delta\Phi \quad (1)$$

Here E_g is the bandgap, m^* is the effective carrier mass, $\Delta\Phi$ is the energy range over which tunneling can take place, t_{ox}, t_{Si}, ε_{ox}, ε_{Si} are the oxide and silicon film thickness and dielectric constants, respectively. By applying drain voltage, the energy bands near drain contact moves down. As gate bias is not applied, Device remains in OFF-state and draws no tunneling current as shown as energy band diagram in Fig. 2 (a), with drain to source voltage V_{DS} = 0V and V_{DS} = 1V. As increasing positive gate voltage, energy bands under the gate controlled region are pushed down, narrowing the width of tunnel junction and allow tunneling current to flow. Corresponding energy band diagram for applied V_{GS} = 1V and V_{DS} = 1V is shown in Fig. 2 (b).

III. RESULTS AND DISCUSSIONS

Simulation results are carried out for proposed structure on the bases of the different donor concentration, gate length, temperature and gate dielectric and corresponding transfer characteristics and energy band diagrams are presented here.

A. Donor Concentration

The transfer characteristics of DGPNTFET with function of gate voltage and different Si- pad doping N_D ($N_D=1\times10^{15}$ cm^{-3}, $N_D=1\times10^{16}$ cm^{-3} and $N_D=1\times10^{17}$ cm^{-3}) is presented in Fig. 3. Here the crucial parameter for device operation is n-type doping which shows a wide variation in OFF state leakage current (I_{OFF}). Simulated results for ON-to-OFF current ratio (I_{ON}/I_{OFF}) and minimum point SS for different donor profile is presented in Table II (I_{ON} at 1.5V, I_{OFF} at 0V). Thus, Si-pad

works as a channel and drain region making device free from extra drain doping.

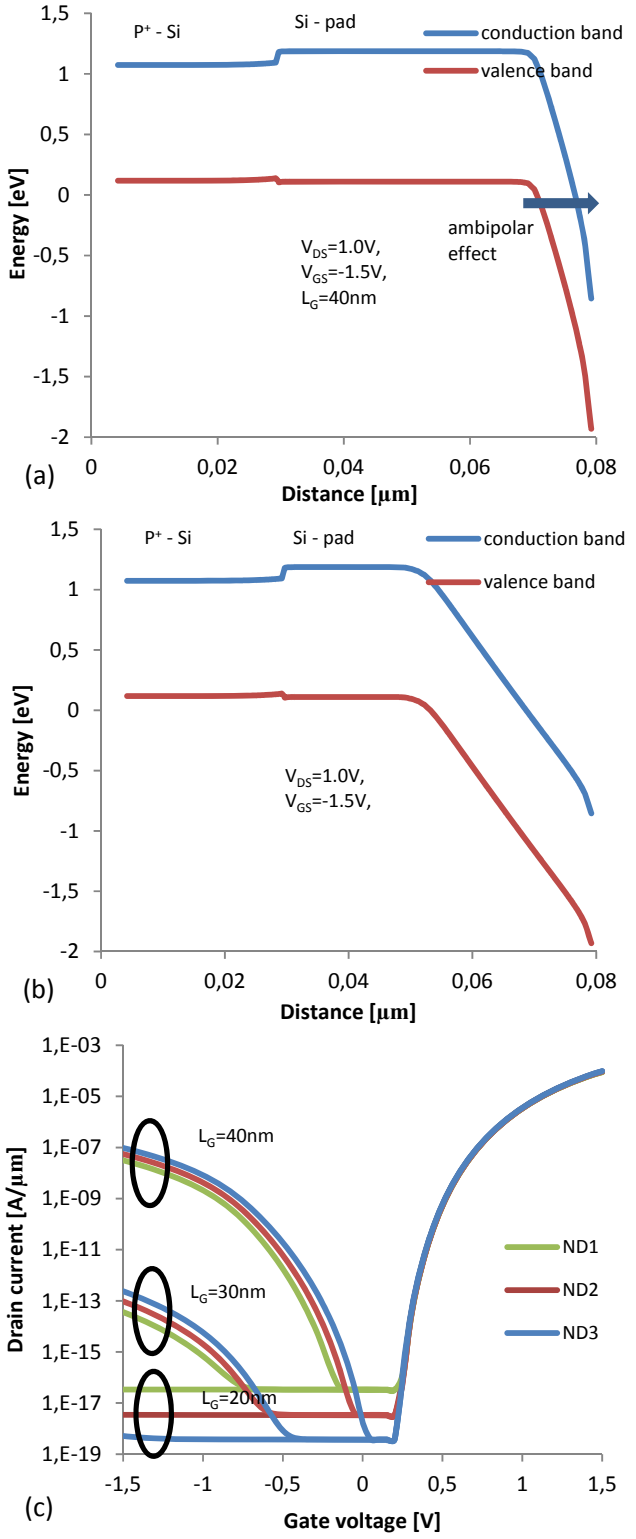


Fig. 4 (a) Band profile of DGPNTFET for gate length (L_G) = 40nm at V_{DS}=1v, V_{GS}= -1.5V (b) Band profile of DGPNTFET for L_G = 20nm at V_{DS}=1v, V_{GS}= -1.5V. (c) Transfer characteristics of DGPNTFET for different gate length (L_G) (where $N_{D1}=1\times10^{15}$ cm^{-3}, $N_{D2}=1\times10^{16}$ cm^{-3}, $N_{D3}=1\times10^{17}$ cm^{-3})

For the validation of our proposed device structure, well calibrated transfer characteristics with conventional double gate TFET (DGTFET) [4] is shown in Fig. 3. Considered device parameters for simulation are: HfO_2 (ε = 22) as gate oxide with thickness (t_{ox}) = 2nm, silicon body thickness (t_{Si}) =10nm, gate length (L_G) = 20nm, p^+ source doping (N_A) = 1×10^{21} cm^{-3}.

B. Gate Length (L_G)

The study of gate overlapping over drain doping [15] says that the OFF-state current at negative gate bias has major impact of gate overlapping. For DGPNTFET as shown in Fig. 4, this ambipolar effect is presented with the help of energy band diagram and transfer characteristics. While having more gate overlapping on Si-pad (L_G=40 nm), as negative gate voltage increases, the energy bands under gate controlled region are pulled up, which create a suitable situation for tunneling near drain. This tunneling or ambipolar effect is shown in Fig. 4 (a), with the help of energy band profile. Decreasing gate length, widened the tunnel junction, decreasing the probability of tunneling T(E) leads to lowering the OFF-state leakage current. The energy band diagram for a case with L_G=20 nm is presented in Fig. 4 (b) at V_{DS}=1V and V_{GS}=- 1.5V. For L_G=20 nm energy bands under gate controlled region moves up. But due to wider width of tunnel junction, probability of tunneling in negative gate bias is minimum.

Ambipolar effect of conventional TFET for negative gate bias is useful for sensing biomolecules [13] whereas, for CMOS technology, where device is operated at both the positive and negative gate bias, tunneling during negative gate bias gives leakage current, which is a major drawback in circuit applications. In DGPNTFET, ambipolar effect not only depends on gate length or gate overlapping but also depends on Si-pad doping profile. Effect of Si-pad doping on ambipolarity is presented in Fig. 4 (c) with the help of transfer characteristics as a function of gate voltage and donor concentration. With similar gate length, and with different donor concentration in Si-pad, DGPNTFET gives different performance characteristics which are marked together and presented in Fig. 4 (c).

C. High-κ Dielectric

Careful choice of gate dielectric can give an even higher device performance in terms of higher ON-current and reduced SS. Transfer characteristics of our proposed structure with different gate dielectric are presented in Fig. 5 (b). Simulation is carried out for gate dielectric like SiO_2 (ε=3.9), Si_3N_4 (ε=7.5), HfO_2 (ε=22), TiO_2 (ε=80) and corresponding variation in characteristic curve is shown in Fig. 5 (b). For TFETs, the improved coupling between the gate and the tunneling barrier has an exponential effect [14]. Similar to conventional TFET for DGPNTFET also this coupling is exponential in nature rather than linear one. Fig. 5 (b) shows that different gate oxide has no impact on device OFF-current. Improved ON-current and reduced SS is pure influence of higher control of gate over tunneling with high-κ gate

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dielectric. Simulated transfer characteristics are carried out for 2 nm of oxide thickness and gate work function of 4.5 eV. Corresponding value of I_{ON} (at V_{DS}=1v, V_{GS}=1.5V), I_{OFF} (at V_{DS}=1v, V_{GS}=0V) and point SS is given in Table III.

TABLE III
SIMULATION RESULTS OF DGPNTFET WITH GATE OXIDES

Gate oxide	I_{OFF}(AT V_{DS}=1, V_{GS}=0V)	I_{ON}(atV_{DS}=1V, V_{GS}=1.5V)	I_{ON}/I_{OFF}
SiO_2(ε=3.9)	3.72×10^{-19}	3.47×10^{-7}	0.93×10^{12}
Si_3N_4(ε=7.5)	3.63×10^{-19}	5.89×10^{-6}	1.62×10^{13}
HfO_2(ε=22)	3.52×10^{-19}	9.70×10^{-5}	2.75×10^{14}
TiO_2(ε=80)	3.46×10^{-19}	2.50×10^{-4}	0.72×10^{15}

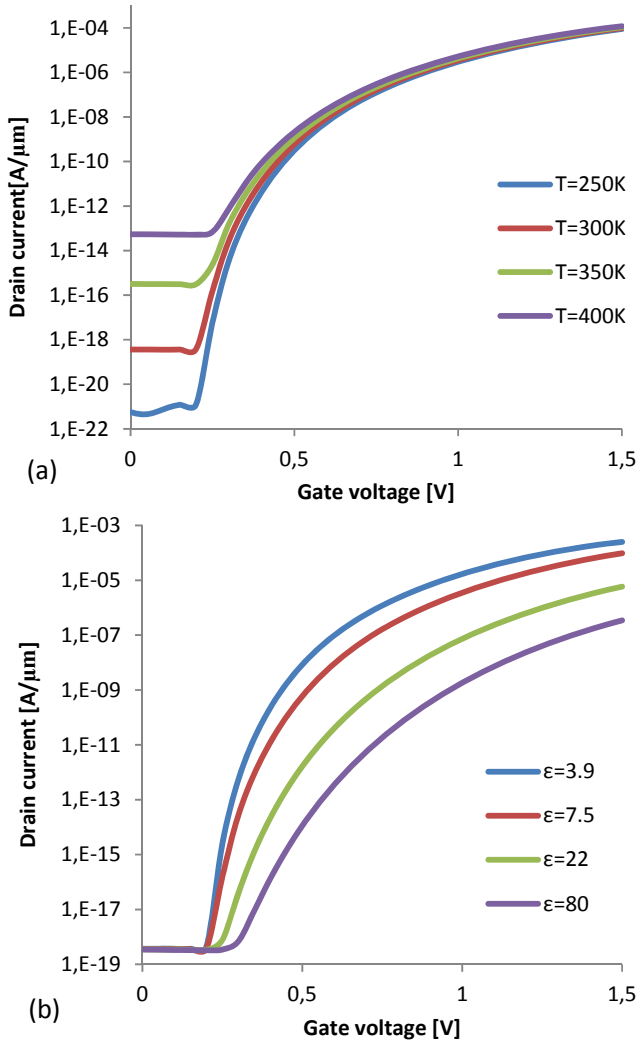


Fig. 5 Transfer characteristics of DGPNTFET for different parameters variations (a) temperature (b) Gate oxide dielectrics.

D. Temperature

Low OFF current in TFET is due to reverse biased junction. The generation of charge carriers increases with temperature, as a result the OFF state current increases. Furthermore, ON current in DGPNTFET is only dependent on tunneling at p^+ - n interface, which has no impact of temperature as temperature study of TFET [8].

In this work, we carried out transfer characteristics for temperature T =250 K, T=300 K, T=350 K, and T= 400 K for DGPNTFET. Fig. 5(a) shows the OFF and ON state current variations with gate voltage as variable parameter and different temperature.

IV. CONCLUSION

This paper demonstrates the new design concept of DGTFET called DGPNTFET and confirmed through simulation. The novelty of this structure lies with the fact that it does not require any additional drain doping. This gated PN diode device is advantageous in case of typical fabrication process as additional drain doping is not required. The simulated result shows SS of 19.14 mV/decade and I_{ON} / I_{OFF} of 2.66×10^{14} (at V_{DS} = 1V, V_{GS} = 1.5V). Moreover ambipolar effect in OFF-state is completely removed for gate length of 20nm in DGPNTFET. However, currently studied techniques to improve ON-state current and SS could also be employed to DGPNTFET. This paper provides a guideline to explore new features and in depth analysis.

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